# AS7620 Evaluation Board

## 500mA Hysteretic High Voltage Step-Down Converter with Dual Power Monitor

## 1 General Description

A demonstration board is available to test AS7620 functionalities and performance in a standard application.

Default conditions are $V_{IN}$=24V and $V_{OUT}$=5V, but in principle the input voltage can range from 5V to 32V.

While the AS7620 output voltage can range from 1.2V to $V_{IN}$, the demonstration board upper output voltage limitation is 15V.

The output voltage can be easily adjusted using the 0805-sized output resistor divider pads on the back of the evaluation board.

## 2 Key Features

- Convenient test point loops for input, output, shutdown and power monitor flags
- High Voltage ceramic capacitor for output voltages of up to 15V
- Micro-power LDO generates 3.3V for flag outputs, supplies up to 250mA
- Single-sided assembly allows convenient backside access for modification
- Large-size 0805 parallel pads for all configuration resistors
- Alternate landing pads for output inductor and capacitor
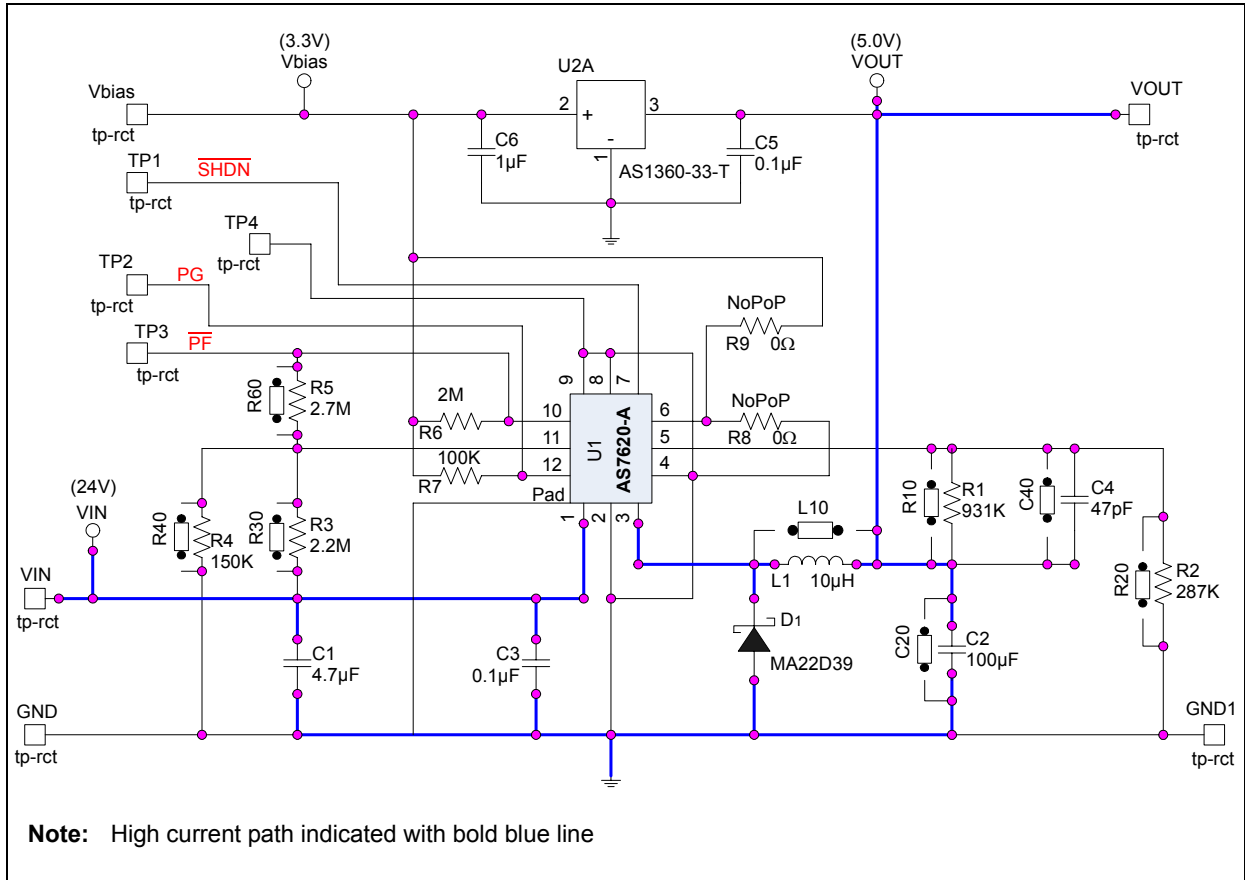- Quiet GND probe point minimizes GND loop area and noise

*Figure 1.  Demo Board Photograph*

# 3  Schematic & BOM

In Figure 2, the bold lines indicate high current paths. Components placed on both TOP and BOTTOM side are highlighted in the schematic.

*Figure 2.  Schematic and BOM*



**Note:**  High current path indicated with bold blue line

# 4 Layout & Component Placement

The layout must be drawn properly in order to minimize the noise, which can affect the behaviour of the converter itself and/or other electronic stages located nearby. The following high current path can be identified:

1. Input Power
2. Output Power
3. GND
4. Switching node (LX)

In order to maximize the efficiency and minimize the noise generated by pulsed currents, the above traces must be as wide and short as possible. Special attention must be paid when positioning the FB trace, which will carry the output voltage information into the device. The FB trace must be away from the switching node and, possibly, shielded by a GND trace in between.
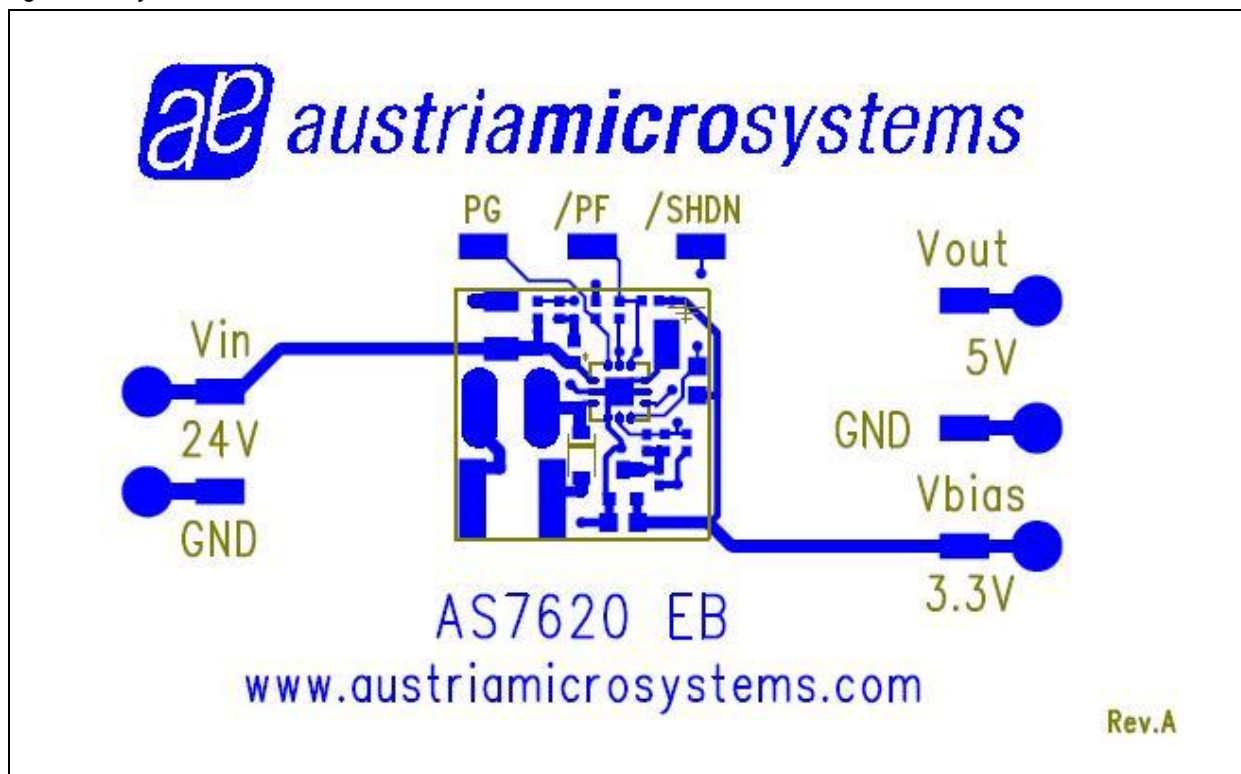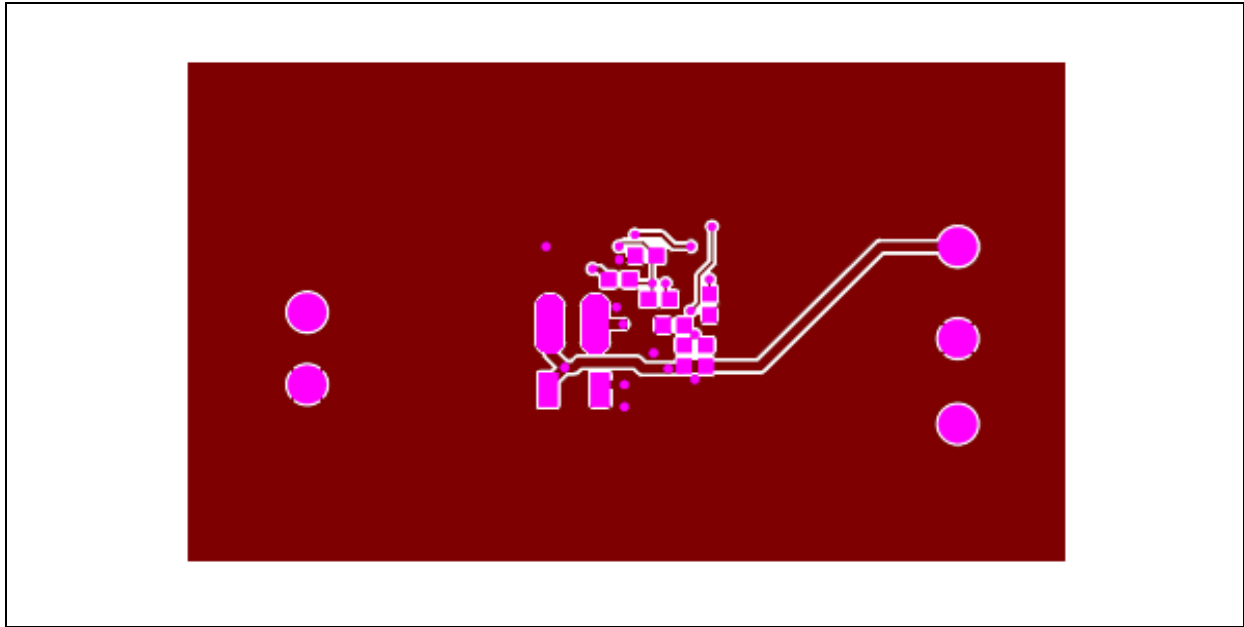
*Figure 3. Layout TOP Side*
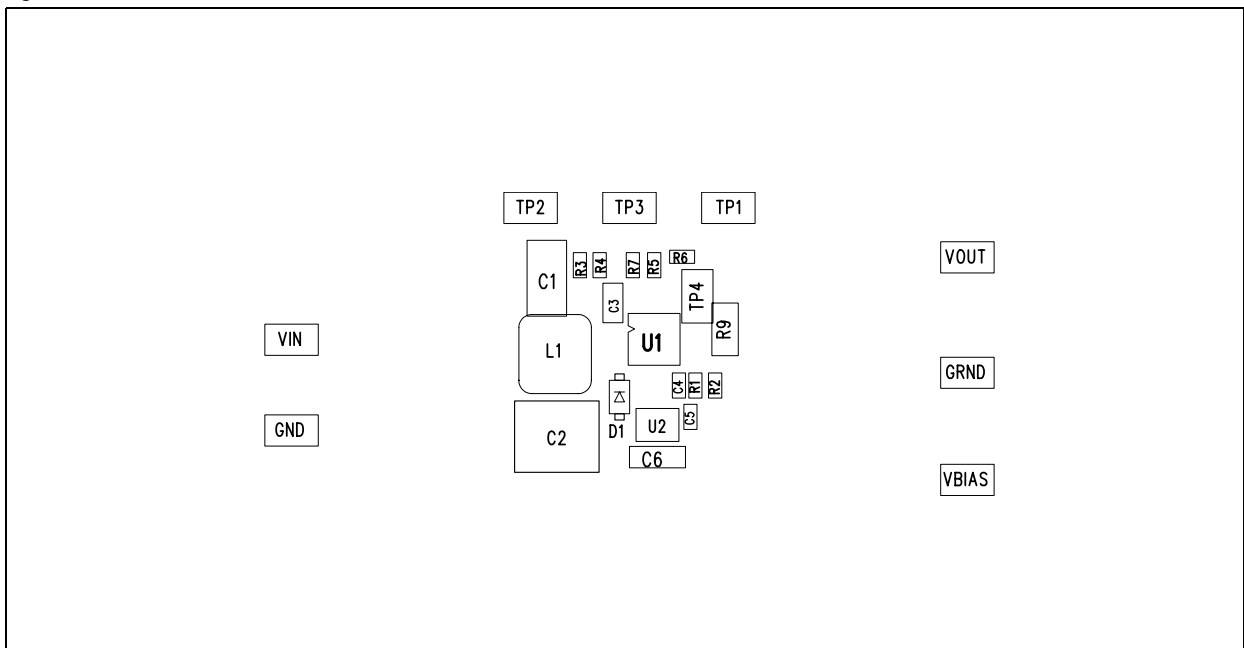
*Figure 4.  Layout BOTTOM Side*



All components that are changing the operating characteristics of the AS7620 have optional parallel access pads on the back-side. Larger size 0805 surface mount resistors and capacitors can be soldered in parallel to the default components. Output capacitor and inductor also have mirrored pads to more conveniently change the component value. With the default resistor still in place, the effective resistor value is calculated as follows:

$$(1/R\_eff = \frac{1}{R} + \frac{1}{R^1} ) \text{ or } R\_eff = \frac{R*R^1}{R + R^1} \qquad \text{(EQ 1)}$$
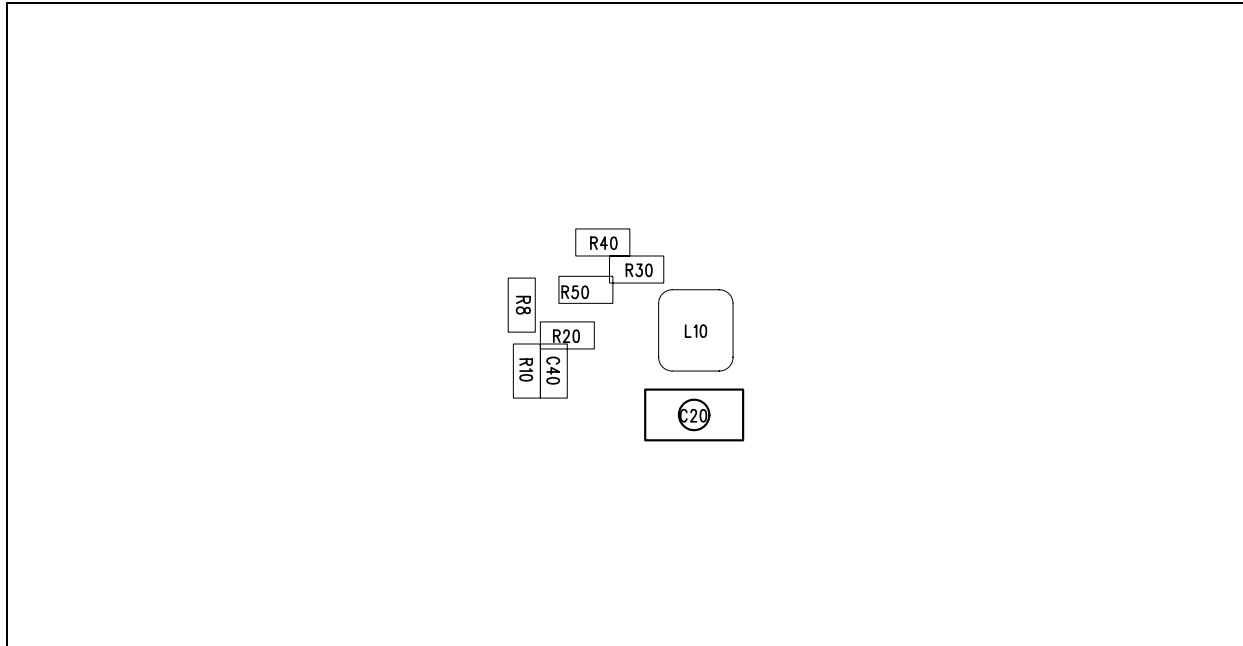
The schematic identifies optional parallel components with a 'zero' added to the component index, for example R10 is in parallel to R1. Additionally, the access pads may be used to probe certain nodes in the circuit that are not already connected to a test point.

*Figure 5.  Placement TOP*

Testing switch-mode converters requires attention to probe placement, in particular GND connections. It is best practice to use the most sensitive GND connection as a single point GND reference. Pin 4 of the AS7620 is the recommended GND connection and TP4 has been located very close to it to minimize GND loop currents. Because of high-frequency content of the switching frequencies, it is best to use a short GND strap connected closely to the probe pin and connect it to TP4, which is labelled with a GND symbol on the front.

*Figure 6.  Placement BOTTOM*



## Bias Voltage

A stable 3.3V derived from $V_{OUT}$ by the 'austriamicrosystems' ultra-low power linear regulator (AS1360) is available on board to pull up the PGOOD, PF and ILIM pin. In general those pins can accept a pull up voltage up to 3.6V. Vbias is accessible by the related terminal on the board. The AS1360 delivers up to 250mA and therefore can also be used to post-regulate the output voltage of the AS7620, effectively removing ripple voltage and hysteretic switching artefacts. Please consult the AS1360 datasheet for optimizing the output voltage of the AS7620 to accommodate the drop-out voltage of the AS1360 for most efficient power conversion performance.

## Power Good

The PG output comes outside with a dedicated terminal on the board. If the output voltage is not lower than 93% (typ) of the set point, the internal open drain will be off.

## Early Power Fail

The input voltage is monitored by the $V_{EPF}$ pin and a dedicated flag (PF active low) is provided outside. The status of PF depends on the programmed threshold and hysteresis. Table 1 provides the resistors values covering all the standard input BUS. The resistors values are 1% commercial values. It is mandatory to use the correct resistors values to guarantee the respect of maximum absolute voltages at EPF and PF pin. $V_{DD}$ has been considered 3.3V.

Terminology:

VRST: Reset voltage for the EPF. It is 90% of the Input BUS voltage.

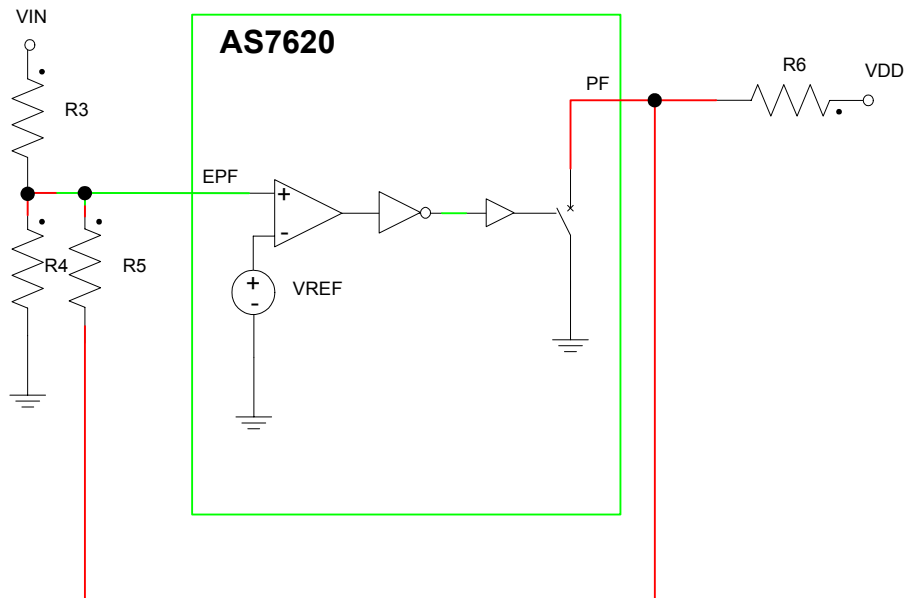VTRIP: Trip voltage for the EPF. It is 80% of the Input BUS voltage.

*Table 1. EPF Network Selection with Different Input BUS*

| V$_{IN}$ (V) | VRST (V) | VTRIP (V) | R3 (K$\Omega$) | R4 (K$\Omega$) | R5 (K$\Omega$) | R6 (K$\Omega$) |
|---|---|---|---|---|---|---|
| 5 | 4.5 | 4 | 365 | 143 | 1740 | 1370 |
| 6 | 5.4 | 4.8 | 464 | 143 | 1870 | 1430 |
| 9 | 8.1 | 7.2 | 768 | 140 | 2050 | 1580 |
| 12 | 10.8 | 9.6 | 1070 | 140 | 2100 | 1650 |
| 15 | 13.5 | 12 | 1370 | 140 | 2150 | 1690 |
| 20 | 18 | 16 | 1870 | 140 | 2210 | 1740 |
| 24 | 21.6 | 19.2 | 2260 | 140 | 2260 | 1740 |
| 28 | 25.3 | 22.5 | 2670 | 140 | 2260 | 1740 |

## Shut Down

This terminal is connected directly to the related pin of the device. Shorting it to GND shuts down the converter. The shutdown pin is internally pulled up and it is recommended to not use any external pull up to avoid conflict and prevent damage to the device.

## Output Voltage Selection

To change the output voltage, R1 and/or R2 have to be changed. The output voltage will be set according to the following formula:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right)$$

*(EQ 2)*

Setting V$_{OUT}$ higher than 15V requires replacement of the output capacitor with the one that is rated above the desired output voltage maximum. Presently a 100µF 16V ceramic capacitor is employed.

## Current Limit

The current is sensed during the on time of the internal PMOS. Three different current limit thresholds can be selected by the ILIM pin:

- 240mA (typ.) ILIM shorted to GND
- 720mA (typ.) ILIM shorted to V$_{OUT}$ (from 1.5V to 3.6V)
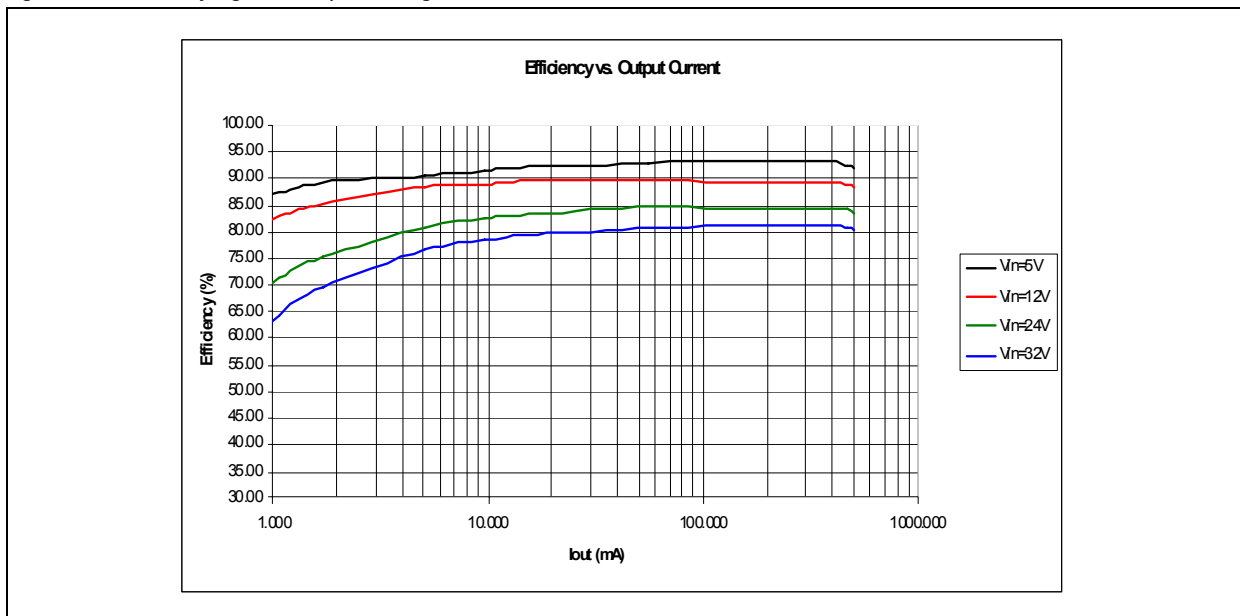- 1000mA (typ.) ILIM Floating

This threshold is intended as peak current limit. If the current reaches the threshold during the on time, the PMOS is turned off. The PMOS will be turned on again only when the current approaches 0A and the feedback voltage is equal or lower than V$_{REF}$. The maximum output current is ILIM/2. Note that the second setting (720mA) has a significant input voltage dependency. Input voltages significantly lower than 24V will reduce the peak current limit. It ranges from 360mA (typ.) at 5V input to 940mA (typ.) at 32V input. Maximum and minimum current limit settings have lesser input voltage sensitivity. Please refer to the product datasheet for Figure 7-Current Limit Threshold vs. V$_{IN}$.

Using the minimum current limit that allows the maximum desired output current, reduces inductor size and cost. Inductors lose their inductance on exceeding their saturation current. Hence, always employ inductors with a higher saturation current rating than the AS7620 current limit setting and not the average output current.

## Efficiency

The hysteretic control loop allows to achieve extremely high efficiency even at very light load.

*Figure 7. Efficiency figure. Output voltage 5V.*

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