BUFFER GATE DRIVER INTEGRATED CIRCUIT

Features

- High peak output current
- Negative turn-off bias
- Separate Ron / Roff resistors
- Low supply current
- Under-voltage lockout
- Full time ON capability
- Low propagation delay time
- Gate clamping when no supply
- Automotive qualified

Applications

- High power inverters
- EV/HEV power trains

Product Summary

Outputs Current:	+/- 10A
Operating Voltage:	13V to 25V
Negative Gate Bias:	0 to -10V

Package

SOIC8

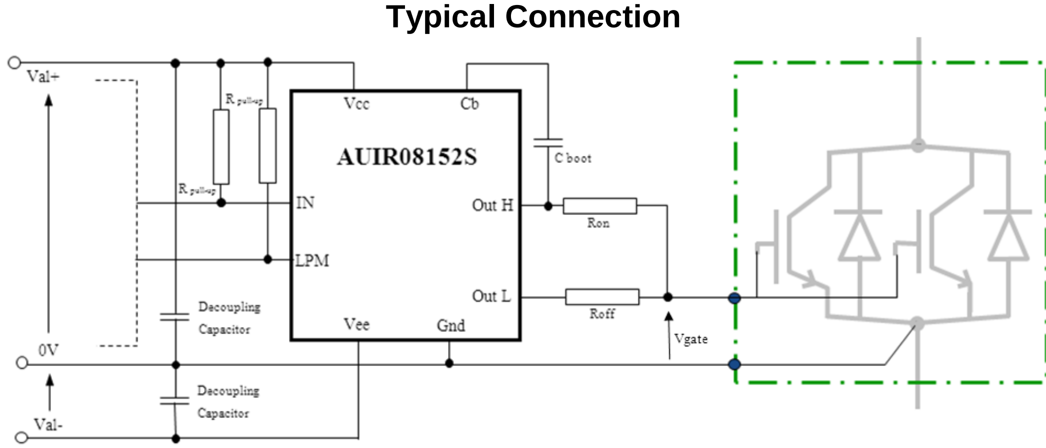
Description

The AUIR08152 buffer brings high power gate drive capability to all pre-driver stages. It is the output extension of the wide I.R gate driver families. It features a negative Gate bias for applications requiring high levels of dv/dt immunity, a low power consumption mode as well as the full time ON gate drive ability. Shoot-through prevention is extended even when the AUIR08152S supplies are absent by mean of a Gate to Emitter self-clamping impedance.

Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIR08152S	SOIC8	Tube	95	AUIR08152S
		Tape and reel	2500	AUIR08152STR

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured mounted on board in free air condition.

Symbol	Definition	Min	Max	Units
Vcc-Gnd	Vcc to Gnd maximum voltage	-0.3	+37	V
Vcc-Vee	Vcc to Vee maximum voltage	-0.3	+37	
Vcc-VIN	Vcc to Vin maximum voltage	-0.3	+37	
Vcc-Vlpm	Vcc to V_{LPM} maximum voltage	-0.3	+37	
VCB	CB to OUTH max voltage	-0.3	+5.5	
I_{LPM}	LPM pin maximum current	-10	+10	mA
Iin	IN pin maximum current	-10	+10	
VOUTH	OUTH pin maximum voltage, DC operation	Vcc - 37	V_{CC} + 0.3	V
VOUTL	OUTL pin maximum voltage, DC operation	V_{EE} - 0.2	V_{CC} + 0.3	
IOUTH	Maximum input transient current to OUTH pin (t < 1us,Ron = 2Ω)	---	2	A
IOUTL	Maximum output transient current from OUTL pin (t < 1us, Roff = 2Ω)	---	1.5	
PD	Package power dissipation @ T_A ≤ 25 °C	—	1	W
RthJA	Thermal resistance, junction to ambient	—	80	K/W
TJ	Junction temperature	-40	150	°C
TS	Storage temperature	-55	150	
TL	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The recommended conditions represent the AUIR08152 optimum performances for the typical application

Symbol	Definition	Min.	Max.	Units
VCC-GND	Gate driver positive supply voltage	15	25	V
GND-VEE	Recommended negative gate bias	0	-10	
VCC-VEE	Total supply voltage	15	35	
VOUTH	OUTH Output voltage	Vcc - 35	Vcc	
VIN,lpm	IN and LPM pins voltage range	Vcc-35	V_{CC}	
Cboot	Recommended bootstrap ceramic capacitor	10	47	nF
Cload	Maximum recommended equivalent gate capacitor	—	240	
Cdec	Recommended Vcc & Vee decoupling capacitors*	22	33	µF
Ron	OUTH series resistor to gate	1.5	20	Ω
Roff	OUTL series resistor to gate	1.5	20	
R pull-up	Recommended pull-up resistor for IN and LPM pins	10	100	kΩ
PWoff	Minimum recommended OFF time on the IN pin	1	—	µs
PWon	Minimum recommended ON time on the IN pin	1	—	

* Due to the high current application a good quality low ESR capacitor has to be used.
Numbers are indicative, a value about 40 times the load capacitance seen at the OutH and OutL pins is suggested.

Static Electrical Characteristics

V_{CC} – Gnd = 15V, V_{EE} – Gnd = -5V, C_{boot} = 15nF, Ron = Roff = 3Ω, -40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC}-GND under-voltage rising edge	—	11.7	12.8	V	LPM = X, IN = Vcc, Vee = Gnd;
V_{CCUV-}	V_{CC}-GND under-voltage falling edge	9.6	10.5	—	V	LPM = X, IN = Vcc, Vee = Gnd;
V_{CCUVH}	V_{CC}-GND under-voltage hysteresis	0.5	1.2	—	V	LPM = X, IN = Vcc, Vee = Gnd;
VCB_{UV} (*)	VCB under-voltage lockout	2.8	4	5.7	V	LPM = X, IN = Vcc, Vee = Gnd;
I_{QGG}	Current out of the Gnd pin	—	20	60	µA	IN = X, LPM = X
I_{QOUTL1}	Current flowing into the OUTL pin	—	0	1.5	µA	IN = Vcc,LPM = X, OUTH = NC, V_{OUTL}–Gnd = 15V
I_{QEESW}	V_{EE} pin current, IN cycling	—	3	8	mA	IN = 10kHz - 50% duty cycle LPM = Vcc, C_{LOAD} = 0nF
I_{QEE0}	V_{EE} pin current – output OFF – normal mode	—	1.5	4	mA	IN = Gnd, LPM = Vcc
I_{QEE1}	V_{EE} pin current – output ON – normal mode	—	0.8	1.6	mA	IN = Vcc, LPM = Vcc
I_{QEELQ0}	V_{EE} pin current – output OFF – low power mode	—	0.6	2.0	mA	IN = Gnd, LPM = Gnd
I_{QEELQ1}	V_{EE} pin current – output ON – low power mode	—	0.8	1.6	mA	IN = Vcc, LPM = Gnd
I_{QEEUV}	V_{EE} pin current at low Vcc supply	—	0.6	1.6	mA	IN = X, LPM = X, V_{CC}<V_{CCUV-}
I_{QB}	CB pin sink current	—	0.5	1	mA	IN = Vcc, LPM = Vcc, V_{CB}-V_{OUTH} = 5.5V
I_{QOUTH0}	OUTH pin sourced current – normal mode	—	1	3.5	mA	IN = Gnd, LPM = Vcc OUTH = V_{EE}, OUTL = NC
$I_{QOUTH0LQ}$	OUTH pin sourced current – low power mode	—	0.2	0.5	mA	IN = Gnd, LPM = Gnd OUTH = V_{EE}, OUTL = NC
I_{BOUTH}	CB pin sourced current – normal mode	30	90	—	mA	IN = Gnd, LPM = Vcc, OUTL = NC, CB = OUTH = Vee
I_{BOUTH_pl}	CB pin pulsed sourced current – normal mode	90	200	—	mA	Min pulse length 2us guaranteed by design
$I_{BOUTHLQ}$	CB pin sourced current – low power mode	0.5	5	23	mA	IN = Gnd, LPM = Gnd, OUTL = NC, CB = OUTH = Vee
I_{OUTH+} /I_{OUTL-}	OUTH /OUTL pins output current capability	10	—	—	A	LPM = X VOUTL-: t < 100us, VOUTH+: CB charged
Vcc-VinH	IN pin – output ON voltage	1.5	2.5	—	V	Vcc-Gnd > Vccuv+
Vcc-VinL	IN pin – output OFF voltage	—	4.5	5.5	V	Vcc-Gnd > Vccuv+
V_{INhys}	IN pin voltage hysteresis	1	2	—	V	Vcc-Gnd > Vccuv+
Vcc-VLPMH	LPM pin normal mode voltage	1.4	2	—	V	Vcc-Gnd > Vccuv+
Vcc-VLPML	LPM pin low power mode voltage	—	3.2	3.8	V	Vcc-Gnd > Vccuv+
V_{LPMhys}	LPM pin voltage hysteresis	0.3	1.1	—	V	Vcc-Gnd > Vccuv+
I_{IN15}	IN pin sourced current	40	90	180	µA	IN = Gnd
I_{LPM15}	LPM pin sourced current	10	25	50	µA	LPM = Gnd
$R_{dson\ OUTH}$	OUTH transistor Rdson	—	100	200	mΩ	IN = Vcc, Iout 10A, t < 100us, Gnd = Vee, V_{CB} = V_{OUTH} + 5.5V
$R_{dson\ OUTL}$	OUTL transistor Rdson	—	200	400	mΩ	-IN = Gnd, Iout = 10A, t < 100us, Gnd = Vee
I_{PMOS} (*)	OUTH Pulling- up current source	15	30	120	mA	IN = Vcc, LPM = X, Vcc – V_{OUTH} = 1.5V

(*)When V_{CB} – V_{OUTH} < VCB_{UV}, OUTH pin remaining pulled-up to Vcc is guaranteed for at least 3usec with low impedance (=Ron) via Vdmos then continuously with larger impedance via Pmos (= Ipmos, see block diagram).

Switching Electrical Characteristics

V_{CC} – Gnd = 15V, Vee – Gnd = -9V, Cboot = 15nF, Ron= Roff = 3Ω , C_{LOAD} = 220nF, -40 °C < T_A < 125 °C unless otherwise specified.

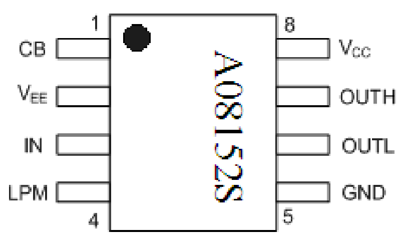
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	OUTH turn on propagation delay	—	150	350	ns	See parameters definitions LPM = X
t_{off}	OUTL turn off propagation delay	—	230	350		
t_{off_VCBuv}	OUTL turn off prop. delay when V_{CB} < VCBuv *	—	90	350		
t_r	OUTH rise time	—	50	150		
t_f	OUTL fall time	—	50	150		
t_{rLQ}	OUTH rise time (IN=1, Vcc ramping up, LPM = Gnd)	—	50	250		V_{EE} = LPM = Gnd, IN = Vcc
t_{fLQ}	OUTL fall time (IN=1, Vcc ramping down, LPM = Gnd)	—	50	250		V_{EE} = LPM = Gnd, IN = Vcc
Min Out-ON	ON time for 0.5µs IN pulse	200	600	900		Cload = open
Min Out-OFF cb discharged	OFF time for 0.5µs IN pulse, CB discharged	200	500	900		Cload = open, CB = 15 nF
Min Out-OFF cb charged	OFF time for 0.5µs IN pulse, CB charged	200	400	900		Cload = open, CB = 15 nF
t_{onLPM}	LPM activation time (from LPM edge to I_{CB} < IBOUTH/2)	—	0.6	3	µs	by design
t_{offLPM}	LPM deactivation time (from LPM edge to I_{CB} > IBOUTH/2)	—	0.6	3		

* See also Fig. 5

Truth Table

IN	LPM	VCC	OUTH	OUTL	Status
X	X	< Vccuv	Open	Vee	IGBT or MOSFET = OFF – Low power mode
Gnd	Gnd	> Vccuv	Open	Vee	IGBT or MOSFET = OFF – Low power mode
Gnd	Vcc	> Vccuv	Open	Vee	IGBT or MOSFET = OFF – Normal mode
Vcc	Gnd	> Vccuv	Vcc	Open	IGBT or MOSFET = ON – Low power mode
Vcc	Vcc	> Vccuv	Vcc	Open	IGBT or MOSFET = ON – Normal mode

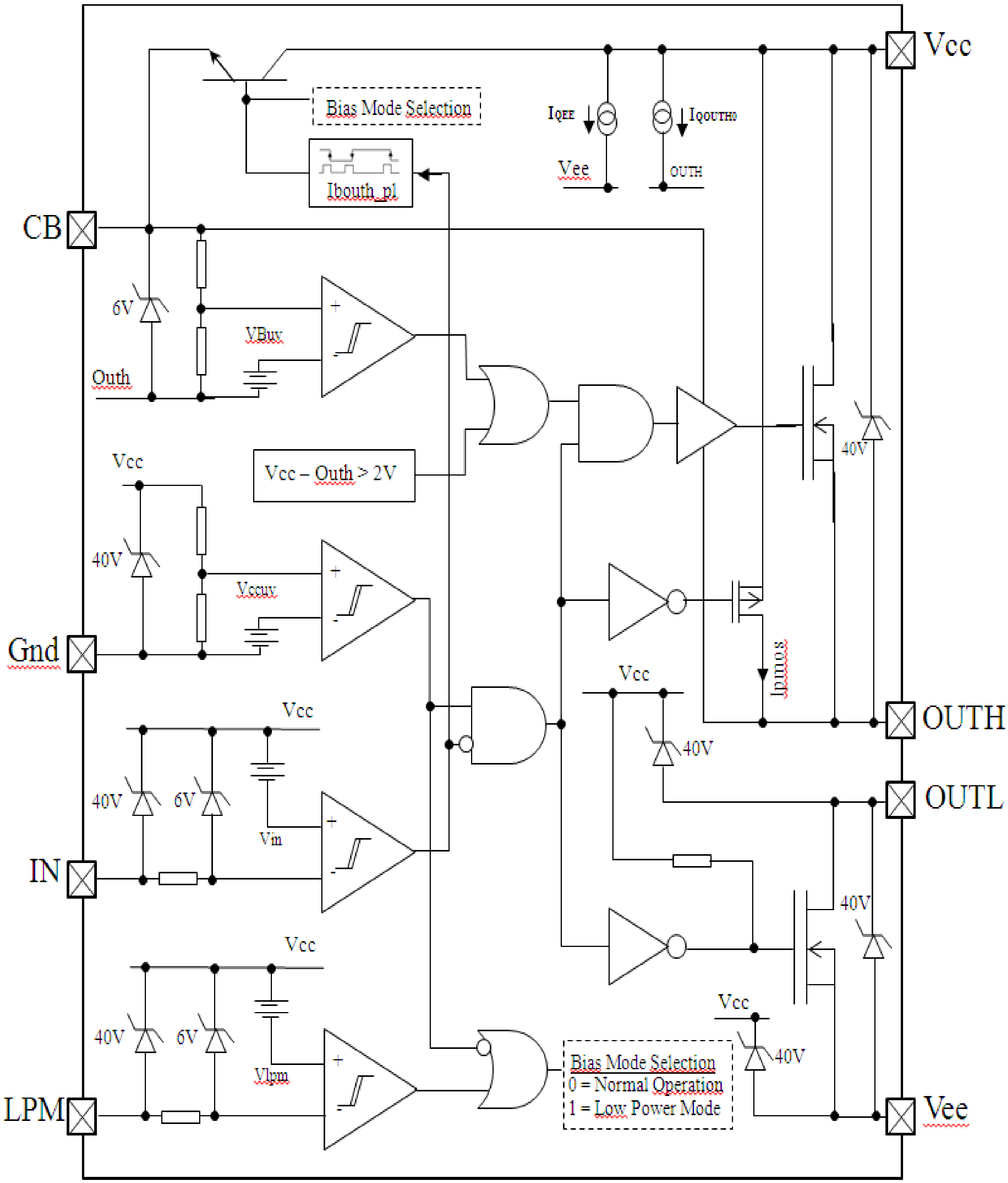
Lead Assignments



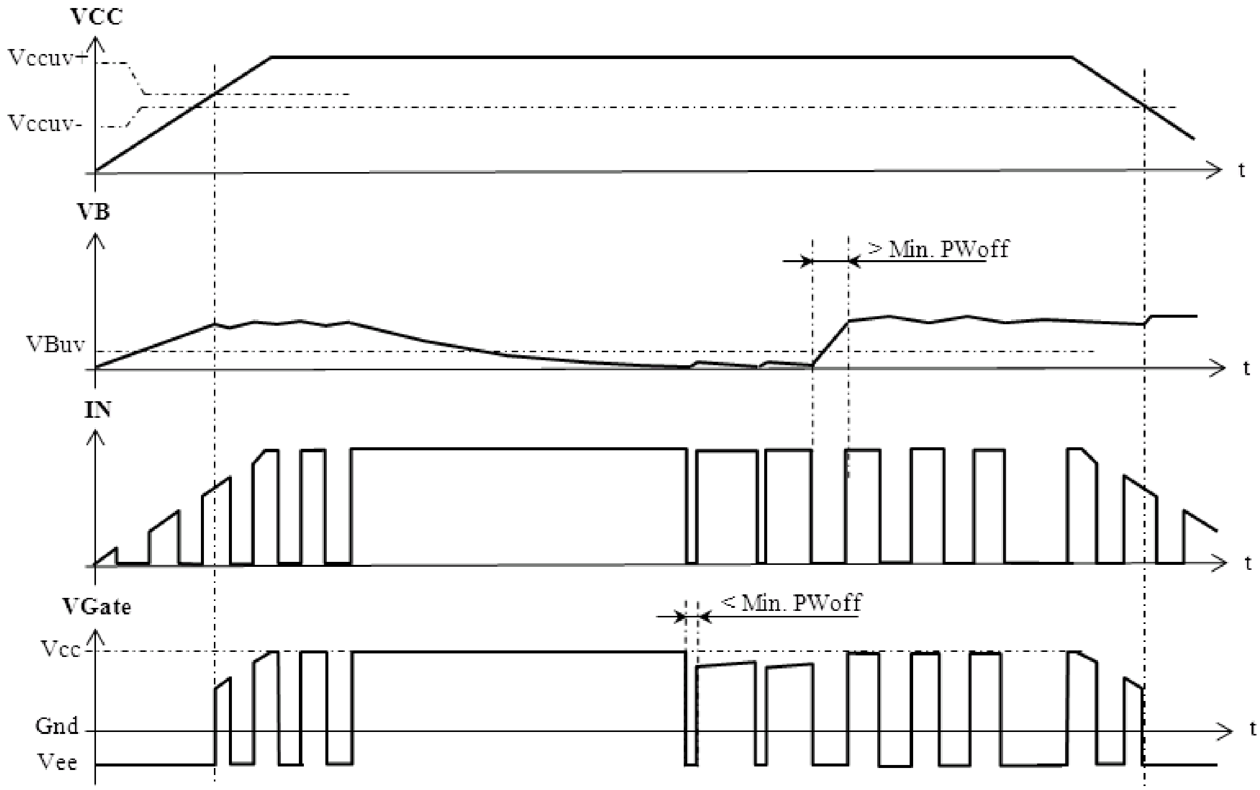
Lead Definitions

Symbol	Description	Pin
CB	External Bootstrap capacitor (cf. typical connection schematic)	1
Vee	Negative Supply Pin	2
IN	Gate Drive Input, (IN= Vcc forces OutH = high)	3
LPM	Low Power Mode Input, LPM= GND activates the Low Power Mode	4
GND	0V – IGBT Emitter or MOSFET Source Connection (cf. typical connection schematic)	5
OUTL	Gate Drive Output Pull down	6
OUTH	Gate Drive Output Pull up	7
Vcc	Positive Supply Pin	8

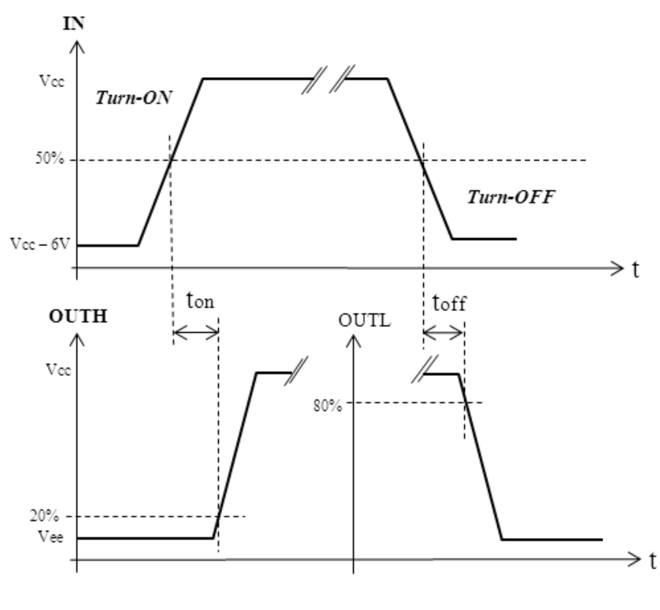
Functional Block Diagram



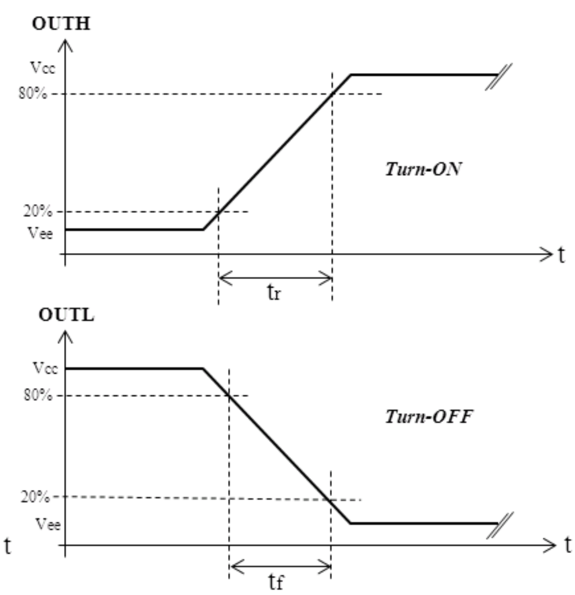
Timing Diagram



Parameters Definitions



Propagation delay definitions



Rise and fall time definitions

Parameters

Figures are given for typical value @ Tj=25°C otherwise specified

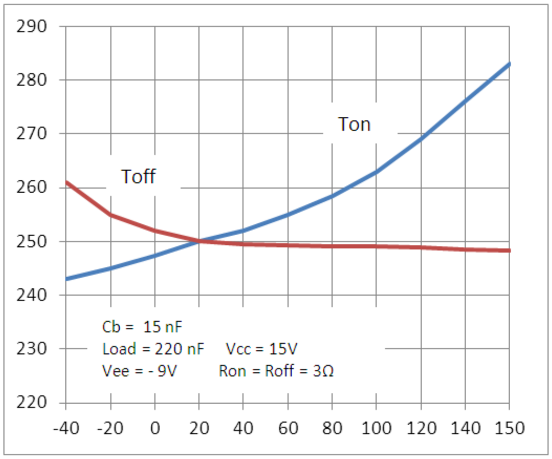


Figure 1: Ton and Toff (ns) Vs Temperature (°C)

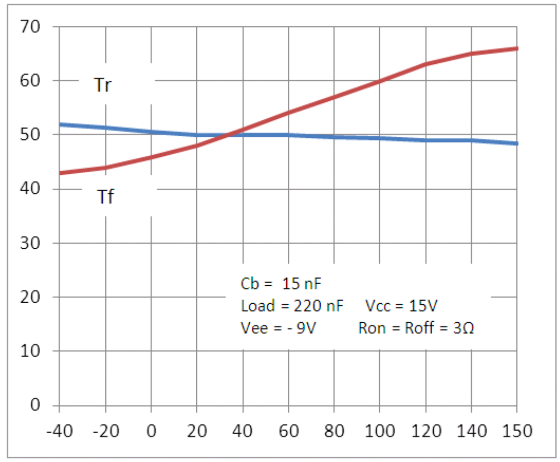


Figure 2: Tr and Tf (ns) Vs Temperature (°C)

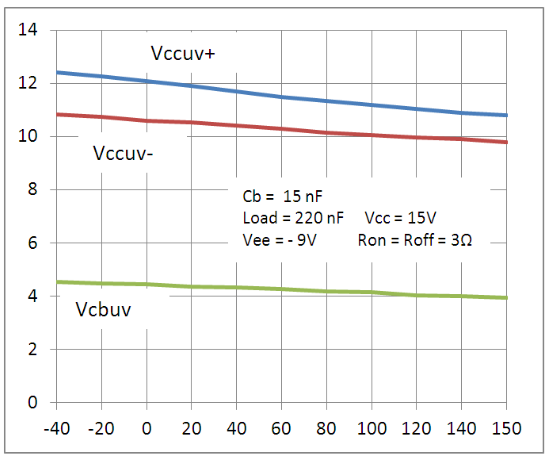


Figure 3: Vccuv+, Vccuv- and Vcbuv (V) Vs Temperature (°C)

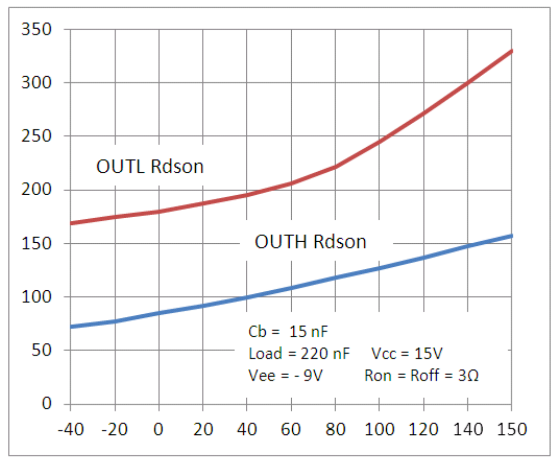


Figure 4: OUTH & OUTL Rdson's Vs Temperature (°C)

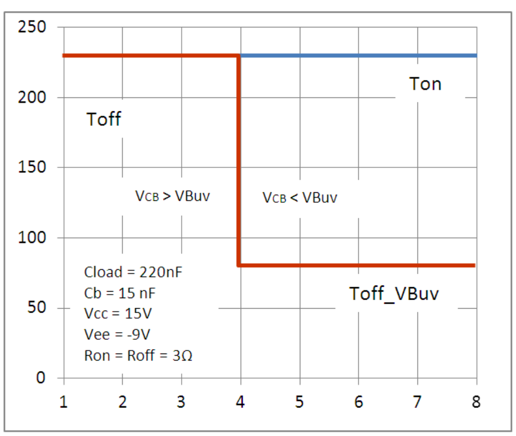


Figure 5: Ton, Toff (ns) Vs IN pulse duration (µs)

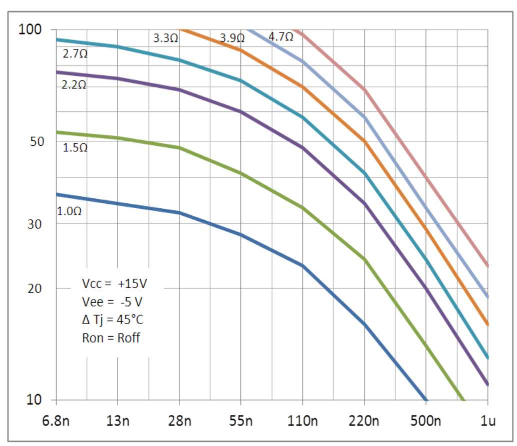


Figure 6: Max PWM Frequency (kHz) Vs Gate Capacitance (F) & Rg (Ω)

Examples of system schematics with HVIC

This section shows how the AUIR08152S can be driven by IR High Voltage IC (HVIC).
All the examples refer to an inverter leg; floating voltage sources to supply the high side AUIR08152S are named Vcch and Veeh, while voltage sources to supply the low side AUIR08152S are named Vccl and Veel.
In the examples, a 7V negative Veeh(l) is shown; this is usually enough to keep even big die size IGBT firmly clamped in their OFF state during dV/dt transients; in case the IGBTs do not require a negative gate voltage, Veeh(l) sources can simply be shorted to their relevant IC GND (h or l).
It is straightforward to say that, when multiple legs are considered, floating supplies must have galvanic isolation between each other (and w.r.to low side); low side supplies could be shared between the different legs but the choice if using multiple or shared low side supplies mostly depend upon the system layout.
Especially important in the emitter impedance Zl, as shown in the figures. Non negligible value of the emitter inductance creates imbalance between the emitter returns and may suggest using separate supplies also for the low side gate drivers.

Example1 : IGBT gate driving by AUIRS2181S and two AUIR08152S buffer ICs.

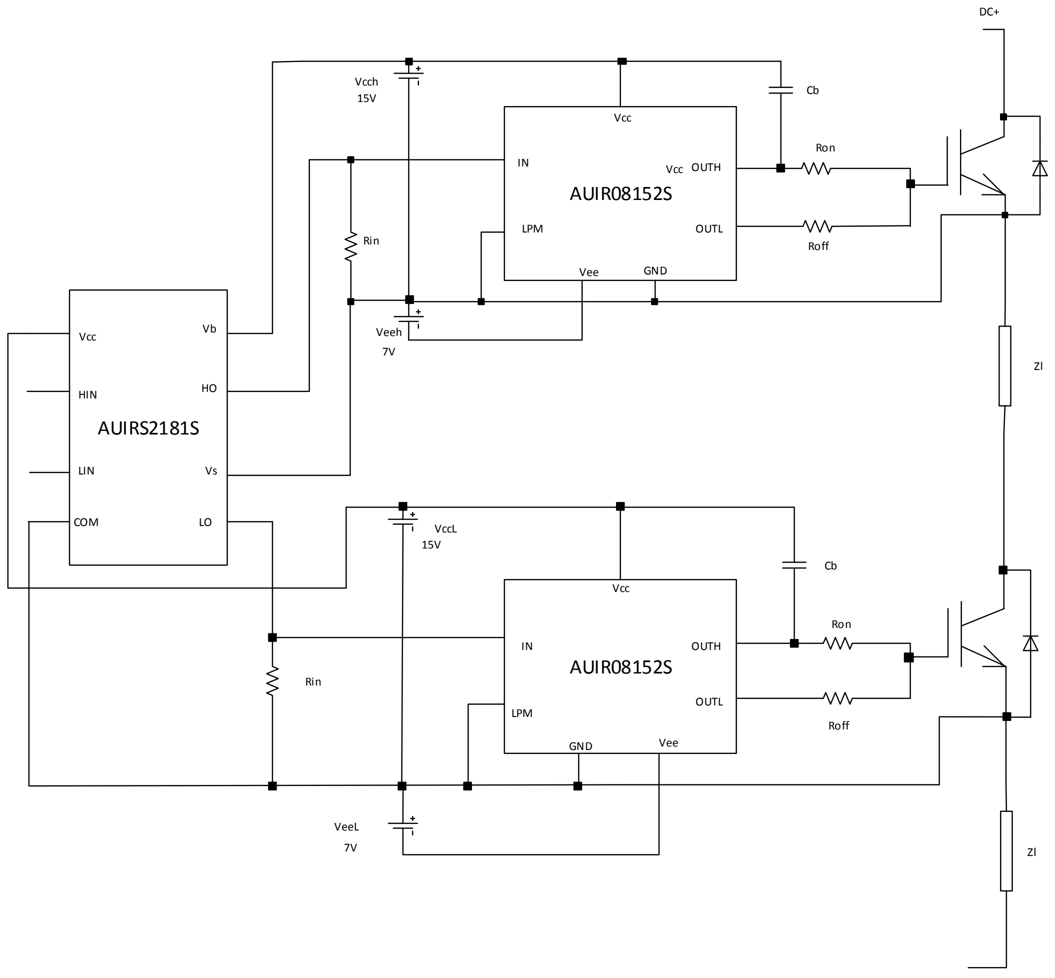


Figure A-1

The AUIRS2181S is a 8 pin SOIC and does not have separate COM (power GND) and Vss (signal GND) pins. Therefore, COM is directly connected to the GND of the low side buffer IC but special care has to be taken when layouting power and control section.

Example 2: IGBT gate driving by AUIRS21814S (or AUIRS2191S) and two AUIR08152S buffer ICs.

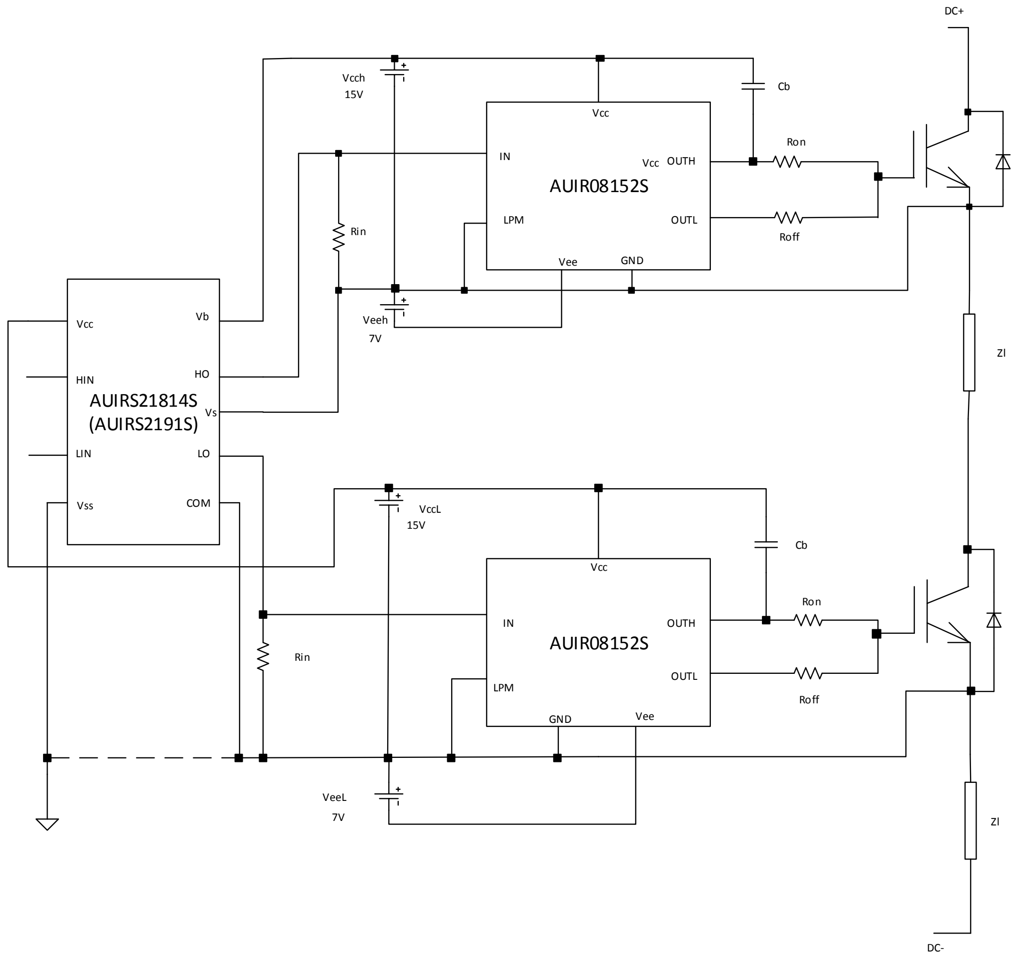


Figure A-2

The AUIRS21814S (and the AUIRS2191S) have separate Vss and COM pins. They can be simply connected together or, better, connected to separate logic and power GND.
In any case, the low side AUIR08152S GND pin has to be connected to the low side IGBT emitter, and layouting care has to be taken that, in case of separate Vss and COM grounding, the imbalance between these two points doesn't exceed the data sheet value (usually +/-5V).

Example 3: IGBT gate driving by two AUIRS2117(8)S and two AUIR08152S buffer ICs.

Here, the situation is partially better in term of separation between logic and power GND, in that even the low side power GND can float -5V to +600V with respect to COM, which is connected to signal GND.
Actually, because the negative Vs transient capability of the AUIRS2117(8) , much more room is allowed for both positive and negative transients of the IGBT emitters w.r.to COM.

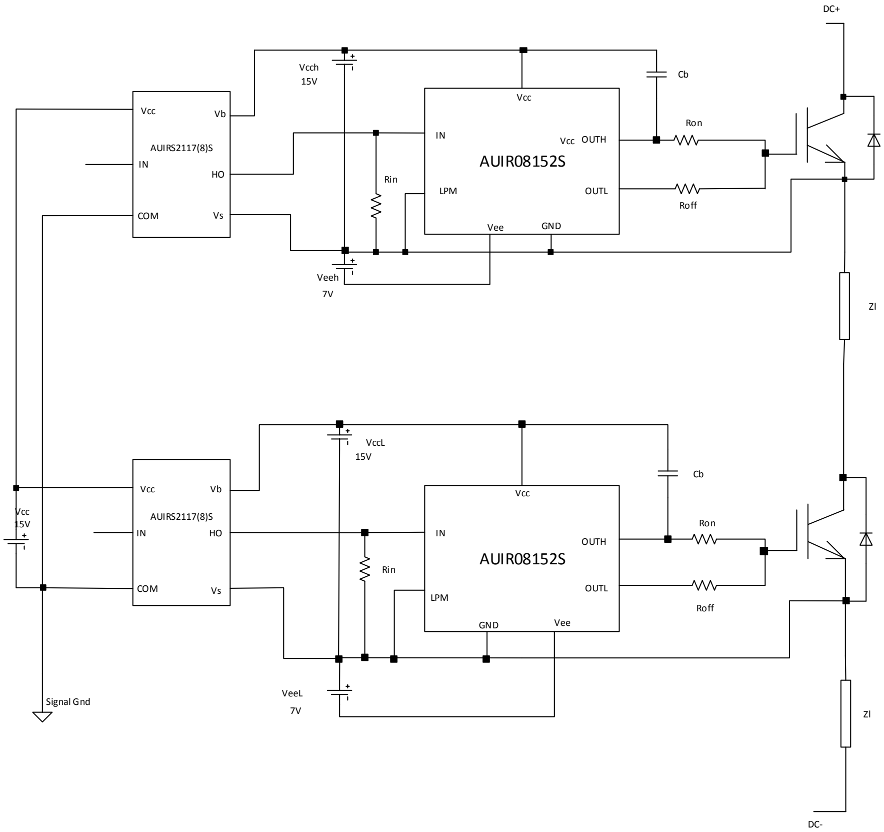


Figure A-3

Examples of system schematics with Opto

The example in Figure A-4 is, again, a leg gate driver where the AUIR08152 are driven by optocouplers.
The optocoupler only needs to drive a logic signal (the input of the buffer) so there is no need for high current capability. Its speed mostly depends upon system switching frequency and control aspects. The propagation delays and rise and fall times of the opto’s stage must preferably be well below the buffer IC ones, to avoid introducing further delays which affect both the system control loop stability and the modulation depth.
Figure A-4 shows the schematic of one of the leg sections (high or low) while Figure A-5 shows the layout.

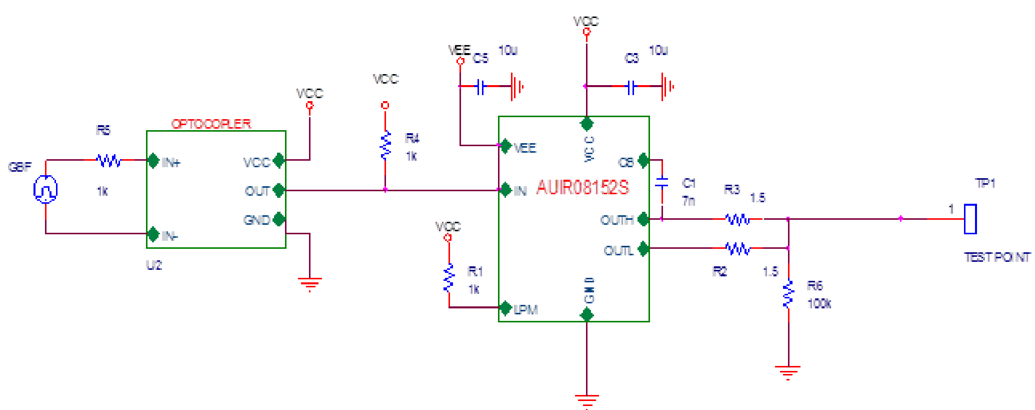


Figure A-4


HI
HG2
HE2
HC
T1
T2
LG1
LI
LE1
I2
C2
VCC2
GND2
VEE2
I1
C1
VCC1
GND1
VEE1
International Rectifier
IOR
AUIR08152S
TP19 TP22 TP20
ROFF2
RON2
TP18
C24
R41
TP21
C25
R15
R05
R32
U3
R34
D12
Q5
R42
C6
J9
CBOOT2
TP2 TP5 TP3
TP4
R1
C23
R9
C22
R5
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J8
U1
C10
R4
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ROFF1
D13
Q1
CBOOT1
TP1
RON1
3R0

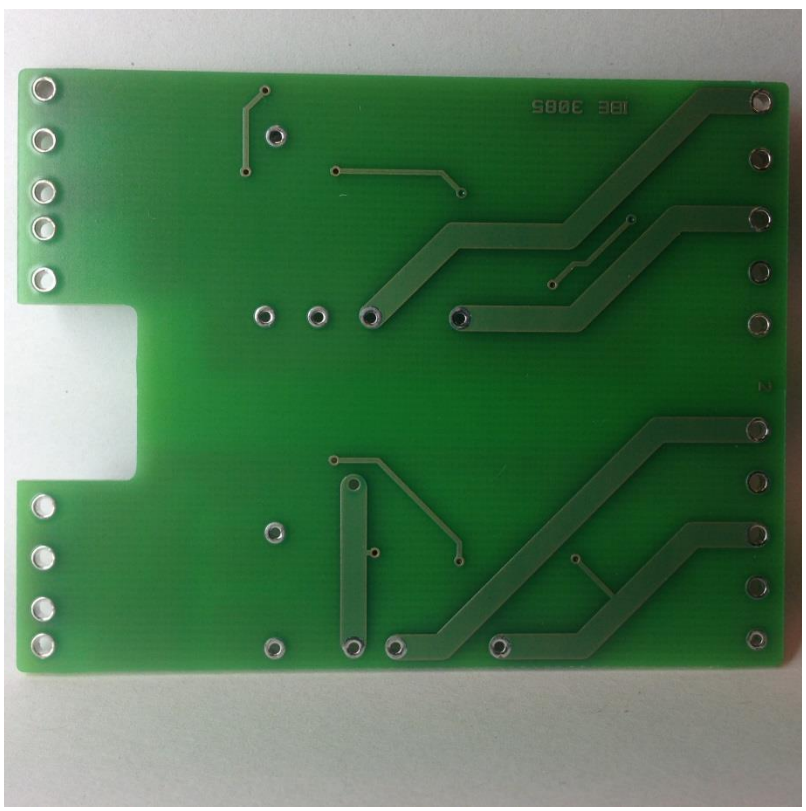


Figure A-5

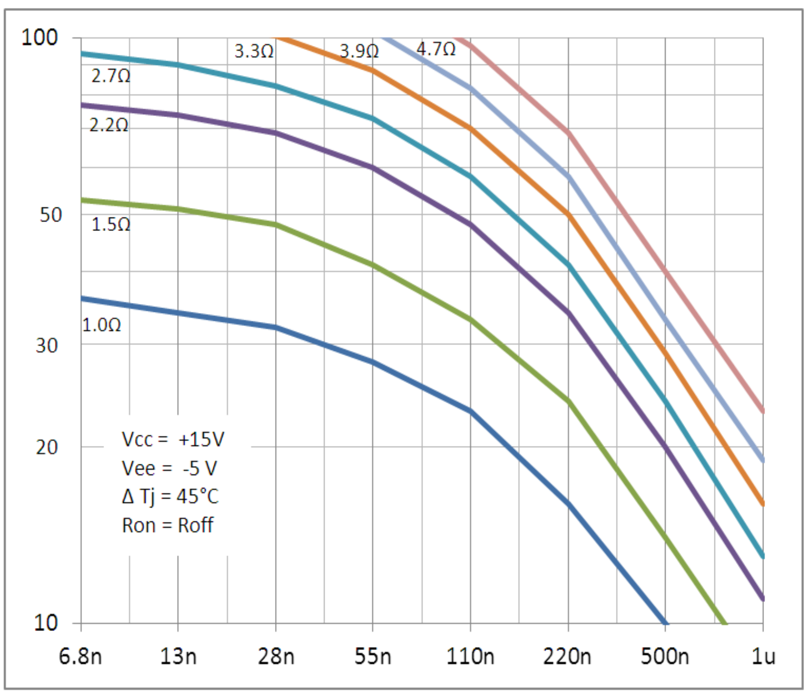
General Application Hints

IN & LPM interface

IN and LPM have a current capability of 10mA max (source and sink); these limits only apply in case the stage driving these signals may go above Vcc or below Vcc-40V.
In the majority of cases, when the driving stage is only an open collector, referenced at GND or –Vee, when looking at the functional block diagram, it appears the internal comparators have 6V zener clamp diodes, whose current is limited to much lower current by internal limiting resistors. These currents are I_{IN15} and I_{LPM15} and are reported in the static electrical characteristics for Vcc=15V and IN and LPM being pulled down at GND level.
In any case, when driving IN and LPM via open collector outputs, a pull-up resistor is needed, to guarantee clean rise times (fall time are uniquely determined by the speed the open collectors turns-on).
Rise time is determined by the pull-up resistor and the equivalent pin capacitance to Vcc. Typically few hundred Ohm to few kOhm are placed here.
If a push pull, and not an open collector, stage is used to drive IN and LPM, no pull-up resistor is needed but pay attention the push pull stage is fed between Vcc and GND or Vcc and –Vee.
A pull down resistor (few hundred kOhm) is suggested instead, especially if long traces or cables connect the predriver to the buffer IC.

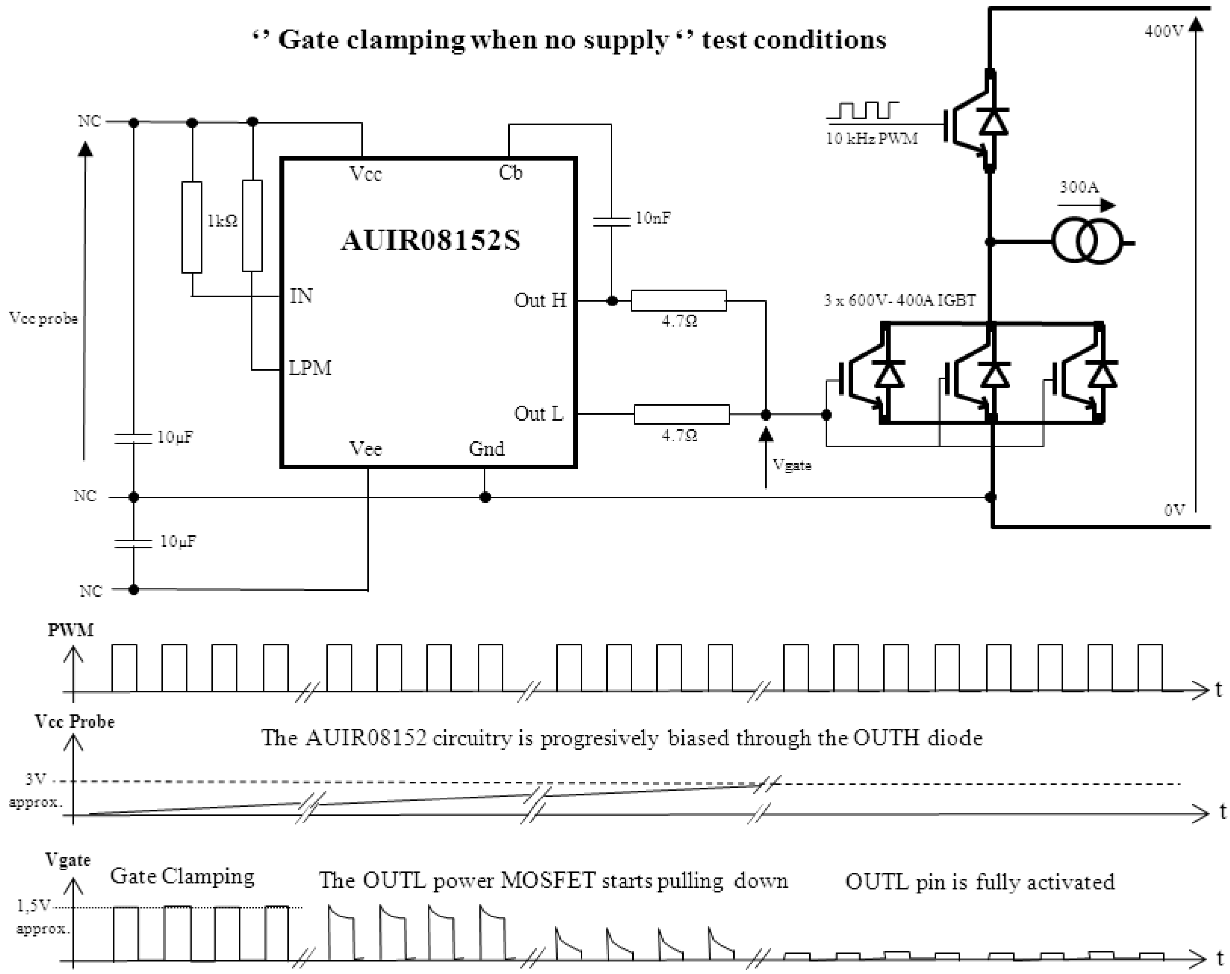
IC power dissipation

This figure is mostly related to the switching frequency, the value of external gate resistances, and the equivalent load capacitance (the IGBT gate Ciss).
A complete characterization of the IC capabilities is given in figure 6, and shown here again for sake of clarity.



Max PWM Frequency (kHz) Vs Gate Capacitance (F) & Rg (Ω)

The AUIR08152S features a self-clamping gate protection in case of the auxiliary power supply disappears. A resistor is pulling up the gate of the OUTL internal power MOSFET to keep OutL pulled down until a minimum Vcc is applied, when Vcc disappears (< about 3V) then the Vgate is clamped via the OUTH ESD diode.
In this situation forcing OutL high injects current into the pin that charges the Vcc decoupling capacitor and reactivates the internal OUTL output power MOSFET (for more info see the Functional Block Diagram).



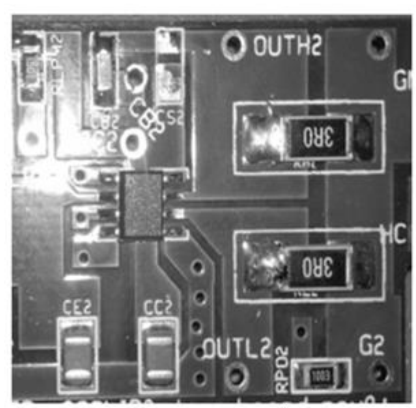
a) If no negative bias is used, Vee shall be connected to Gnd

b) OUTH and OUTL pins shall never be shorted together

c) Decoupling capacitors shall be ceramic types and implemented as close as possible of the AUIR08152S supply pins

d) The decoupling capacitors shall be at least 40 times bigger than the max. Cload and of low ESR type, in order to avoid any Vccuv oscillations

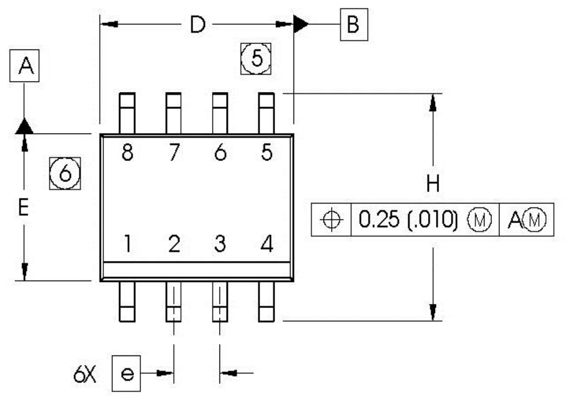
e) IN and LPM pins shall never be left open



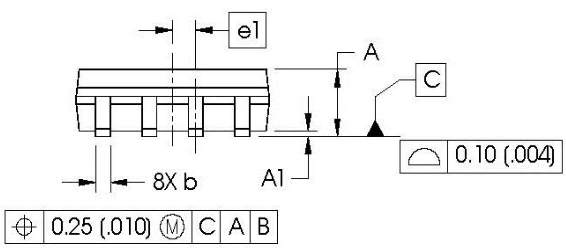
PCB Layout Example

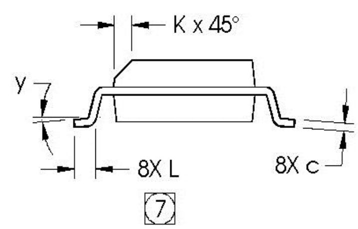
Case Outline – SO8

Dimensions are shown in millimeters (inches)



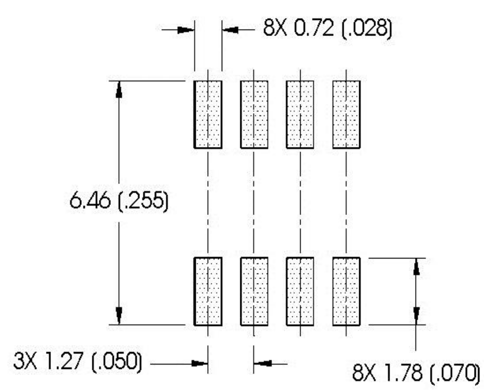
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



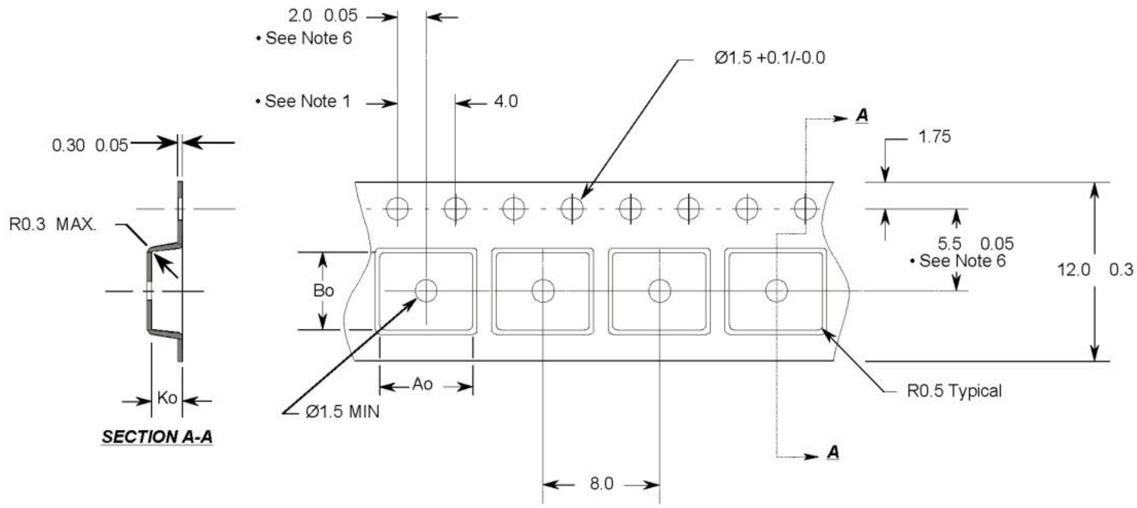


NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



Tape & Reel SO8



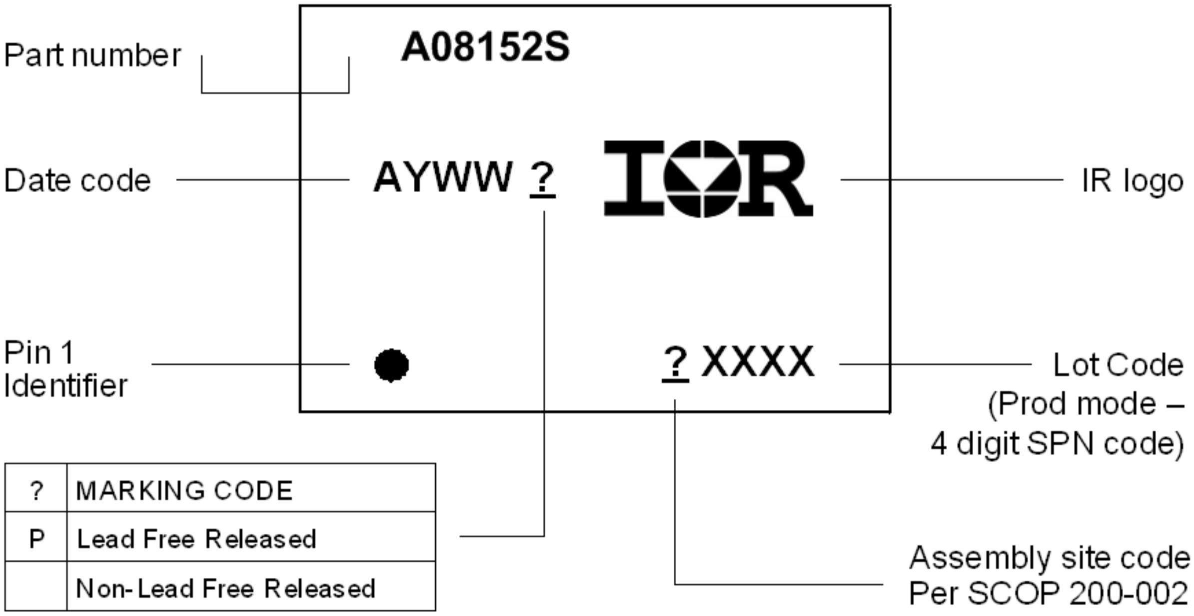
Notes:

1. 10 sprocket hole pitch cumulative tolerance 0.2
2. Camber not to exceed 1mm in 100mm
3. Material: Black Conductive Advantek Polystyrene
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 6.4 mm
Bo = 5.2 mm
Ko = 2.1 mm

- All Dimensions in Millimeters -

Part Marking Information



Qualification Information†

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL2†† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (+/-200V) (per AEC-Q100-003)	
	Human Body Model	Class H2 (+/-2500V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher MSL ratings may be available for the specific package types listed here.
Please contact your International Rectifier sales representative for further information.

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Revision History

Revision	Date	Notes/Changes
A1	August 5th , 2013	Preliminary Datasheet AUIR08152S
A2	August 23rd 2013	Advanced datasheet
A3	August 26th 2013	Advanced datasheet
A4	September 2nd 2013	Final datasheet, updated Iout+ and Iout- definition
A5	Dec. 5th, 2013	Updated cosmetic for production
A6	Aug. 27th, 2014	Updated note * on page 3, updated footprint
A7	Sept 25, 2015	Application section totally updated
A8	Nov. 09th, 2015	Few minor mistyping errors corrected.