DEMO MANUAL DC140

DESIGN-READY SWITCHERS

LTC1436-PLL 2-Output Synchronous Buck Converter with Versatile Frequency Controller

DESCRIPTION

Demonstration circuit DC140 is a 2-output, general purpose evaluation platform intended to demonstrate the many functions of the LTC®1436-PLL and to make it easy to implement circuit changes. The switching frequency of the LTC1436-PLL can be synchronized to an external clock frequency or modulated to reduce EMI by decreasing the average power of the switching harmonics. The high efficiency, constant-frequency advantages of the Adaptive Power™ output stage can be observed under light load conditions. The enable and soft start features of the LTC1436-PLL can also be observed, along with a power-on reset (POR) signal for the main output.

DC140 is intended for users with noise-sensitive applications where conducted and radiated emissions are important design considerations. These applications include radio, cell-phone and other wireless communication products. Two versions of DC140 are available; they differ only in the magnitude of the second output voltage. Both versions provide 5V at 3A on the main output. The second output is derived from the main 5V output and postregulated by an internal auxiliary linear regulator. Version A provides a second output voltage of 3.3V at 0.1A, whereas version B provides a second output of 12V at 0.1A.

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Adaptive Power is a trademark of Linear Technology Corporation.

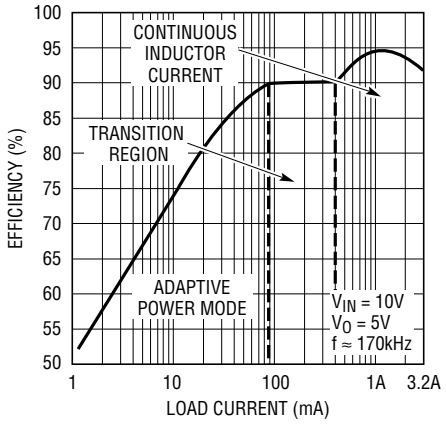
PERFORMANCE SUMMARY

Operating Temperature Range 0°C to 50°C

PARAMETER	CONDITIONS	VALUE
Input Voltage Range	Maximum Input Voltage (Limited by External MOSFETs)	5.5V to 28V
Output Voltage	Main Output, 5V 3.3V Output (Version A) 12V Output (Version B)	4.9V to 5.1V 3.13V to 3.47V 11.4V to 12.6V

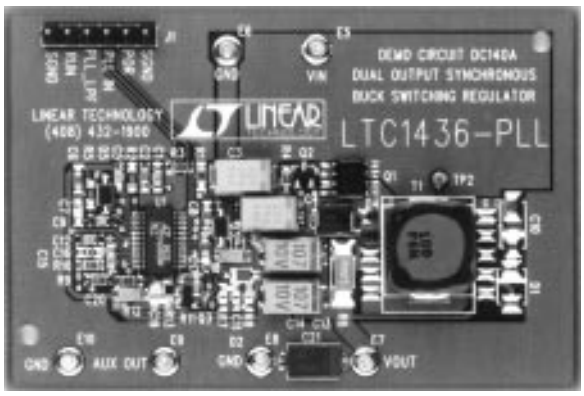
TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Efficiency



DC140 TA01

Component Side

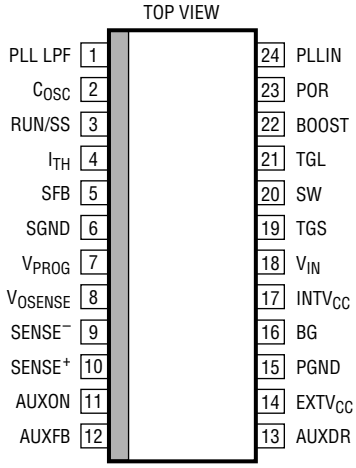


PERFORMANCE SUMMARY

Operating Temperature Range 0°C to 50°C

PARAMETER	CONDITIONS	VALUE
Output Voltage Ripple	5V Output, 3A Load, 10MHz Bandwidth Limited 3.3V Output, 0.1A Load, 10MHz Bandwidth Limited 12V Output, 0.1A Load, 10MHz Bandwidth Limited	$60mV_{P-P}$ $20mV_{P-P}$ $20mV_{P-P}$
Line Regulation	V_{IN} = 6V to 20V, 5V Output	±5mV
Load Regulation	I_O = 0A to 3A, 5V Output	40mV
Frequency	Typical Free-Running Frequency, C_{OSC} = 68pF	170kHz
Supply Current	Typical, V_{IN} = 15V, Both Outputs On (No Load)	320µA
Shutdown Current	Typical, V_{IN}= 15V, RUN/SS = 0V	16µA

PACKAGE DIAGRAM



GN PACKAGE
24-LEAD PLASTIC SSOP
(150 MIL SSOP)

LTC1436CGN-PLL

SCHEMATIC DIAGRAMS

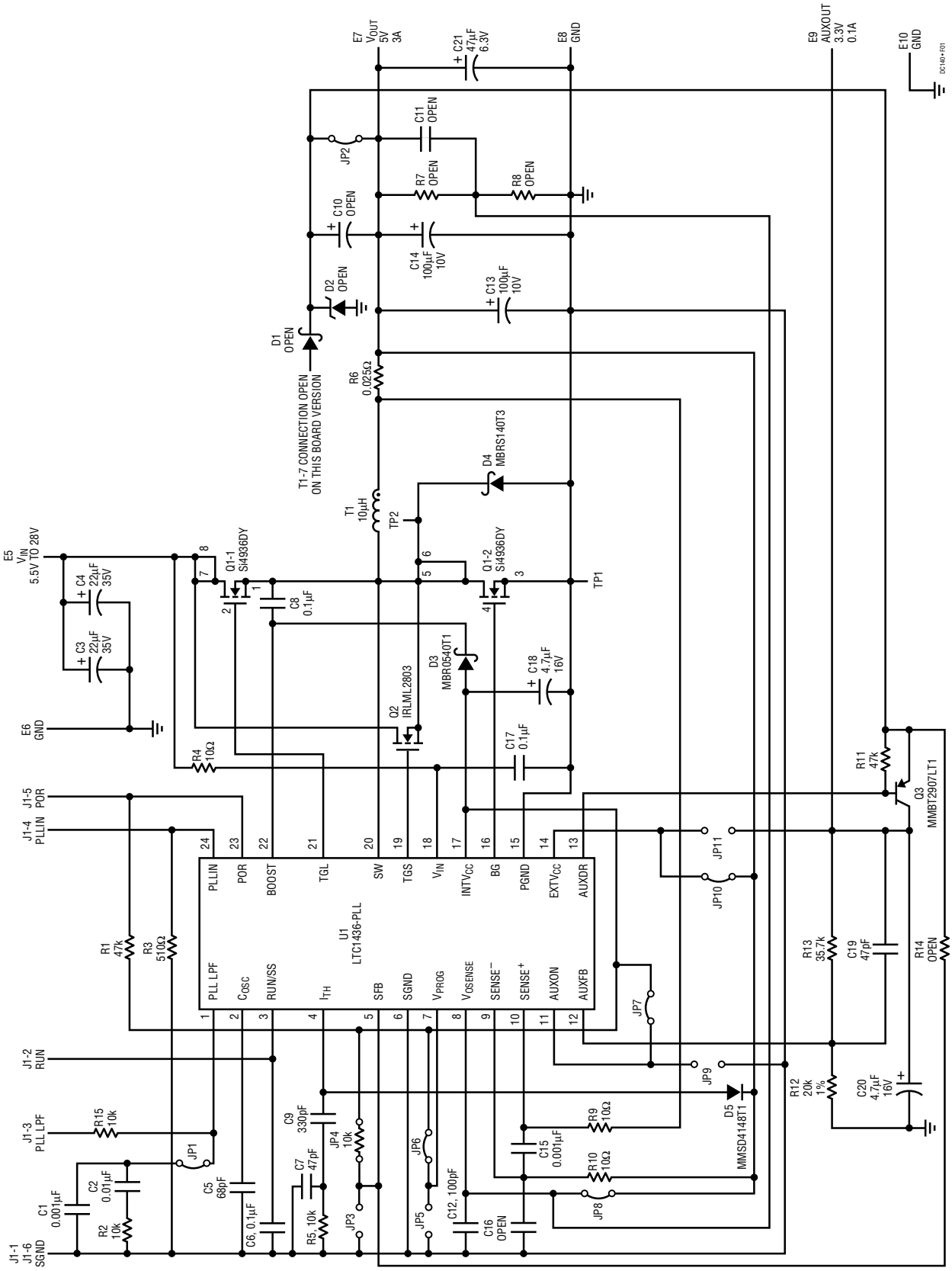


Figure 1. DC140A-A, 5V, 3A and 3.3V, 0.1A Outputs

SCHEMATIC DIAGRAMS

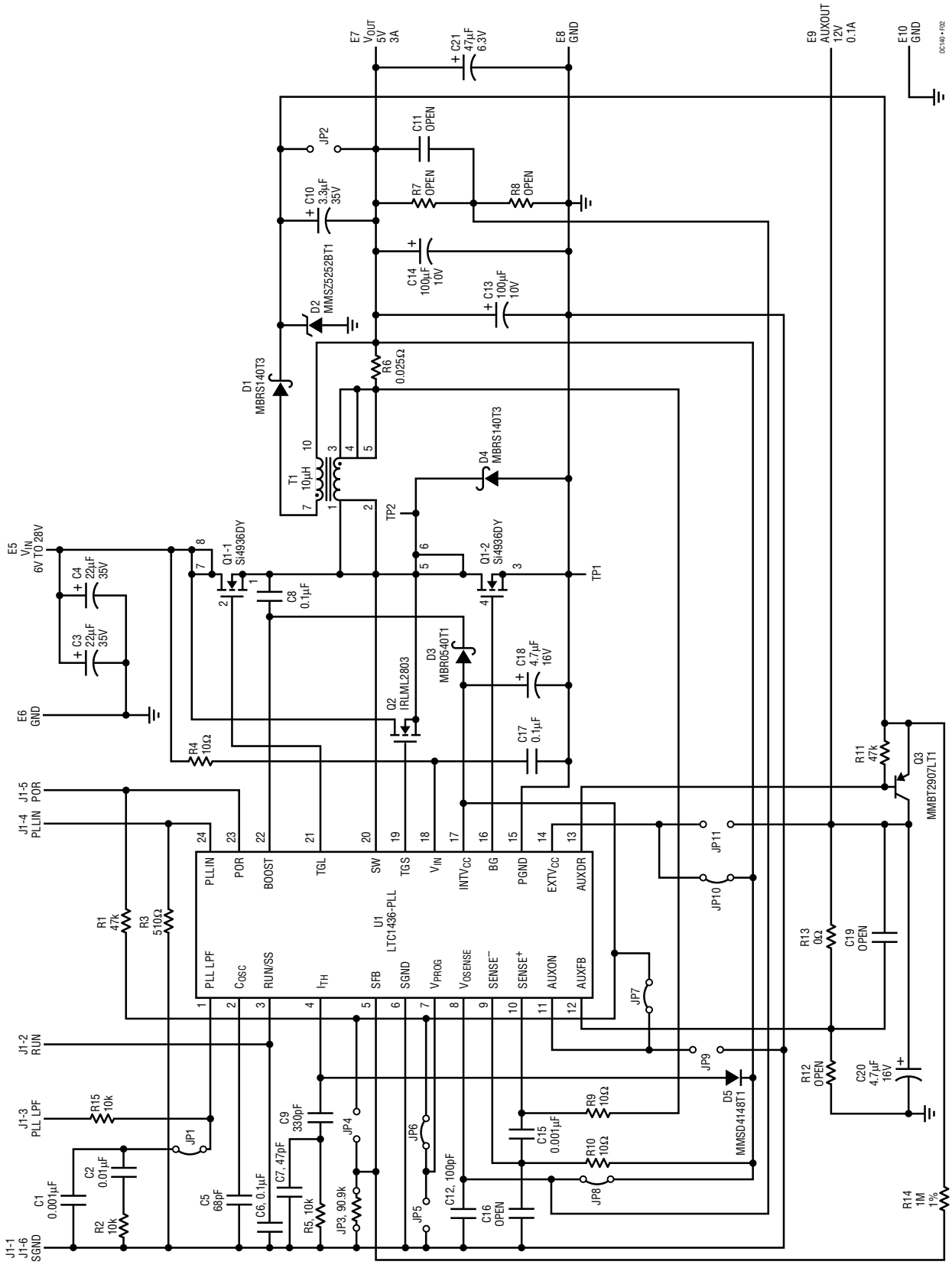


Figure 2. DC140A-B, 5V, 3A and 12V, 0.1A Outputs

PARTS LIST DC140A-A

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C15	2	08055C102KAT1A	0.001µF 50V 10% X7R Chip Capacitor	AVX	(843) 946-0362
C2	1	08055C103KAT1A	0.01µF 50V 10% X7R Chip Capacitor	AVX	(843) 946-0362
C3, C4	2	T495X226M035AS	22µF 35V 20% Tantalum Capacitor	KEMET	(408) 986-0424
C5	1	08055A680KAT1A	68pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C6, C8, C17	3	08055G104ZAT1A	0.1µF 50V –20% 80% Chip Capacitor	AVX	(843) 946-0362
C7, C19	2	08055A470KAT1A	47pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C9	1	08055A331KAT1A	330pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C12	1	08055A101KAT1A	100pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C13, C14	2	TPSD107M010R0065	100µF 10V 20% Tantalum Capacitor	AVX	(843) 946-0690
C18, C20	2	T494A475M016AS	4.7µF 16V 20% Tantalum Capacitor	KEMET	(408) 986-0424
C21	1	EEFCDOJ470R	47µF 6.3V Polymer Capacitor	Panasonic	(201) 348-7522
D3	1	MBR0540T1	Schottky Diode	Motorola	(800) 441-2447
D4	1	MBRS140T3	Schottky Diode	Motorola	(800) 441-2447
D5	1	MMSD4148T1	Diode	Motorola	(800) 441-2447
E5 to E10	6	2501-2	Terminal Turret	Mill-Max	(516) 922-6000
J1	1	3801-06G2	Pin Header 0.100 (1x6) Connector	COMM CON	(626) 301-4200
JP1, JP2, JP6 to JP8, JP10	6	CJ21-000J-T	Shunt Chip 0805	AVX	(843) 946-0362
Q1	1	Si4936DY	Dual N-Channel MOSFET	Siliconix	(800) 554-5565
Q2	1	IRLML2803	N-Channel MOSFET	IR	(310) 322-3331
Q3	1	MMBT2907LT1	Transistor PNP	Motorola	(800) 441-2447
R1, R11	2	CR21-473J-T	47k 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R2, R5, R15, JP4	4	CR21-103J-T	10k 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R3	1	CR21-511J-T	510Ω 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R4, R9, R10	3	CR21-100J-T	10Ω 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R6	1	LR2010-01-R025F	0.025Ω 0.5W 1% Chip Resistor	IRC	(512) 992-7900
R12	1	CR21-2002F-T	20k 0.1W 1% Chip Resistor	AVX	(843) 946-0524
R13	1	CR21-3572F-T	35.7k 0.1W 1% Chip Resistor	AVX	(843) 946-0524
T1	1	CDRH125-100	10µH Inductor	Sumida	(847) 956-0666
TP1, TP2	2	1425-2	Micro Pin Terminal	Keystone	(718) 956-8900
U1	1	LTC1436CGN-PLL	I.C. LTC1436-PLL	LTC	(408) 432-1900

Note: Part locations for C10, C11, C16, D1, D2, JP3, JP5, JP9, JP11, R7, R8 and R14 are not used on this assembly.

PARTS LIST DC140A-B

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C15	2	08055C102KAT1A	0.001µF 50V 10% X7R Chip Capacitor	AVX	(843) 946-0362
C2	1	08055C103KAT1A	0.01µF 50V 10% X7R Chip Capacitor	AVX	(843) 946-0362
C3, C4	2	T495X226M035AS	22µF 35V 20% Tantalum Capacitor	KEMET	(408) 986-0424
C5	1	08055A680KAT1A	68pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C6, C8, C17	3	08055G104ZAT1A	0.1µF 50V –20% 80% Chip Capacitor	AVX	(843) 946-0362
C7	1	08055A470KAT1A	47pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C9	1	08055A331KAT1A	330pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C10	1	TAJC335M035	3.3µF 35V 20% Tantalum Capacitor	AVX	(843) 946-0362
C12	1	08055A101KAT1A	100pF 50V 10% NPO Chip Capacitor	AVX	(843) 946-0362
C13, C14	2	TPSD107M010R0065	100µF 10V 20% Tantalum Capacitor	AVX	(843) 946-0690
C18, C20	2	T494A475M016AS	4.7µF 16V 20% Tantalum Capacitor	KEMET	(408) 986-0424
C21	1	EEFCDOJ470R	47µF 6.3V Polymer Capacitor	Panasonic	(201) 348-7522
D1, D4	2	MBRS140T3	Schottky Diode	Motorola	(800) 441-2447
D2	1	MMSZ5252BT1	24V Zener Diode	Motorola	(800) 441-2447
D3	1	MBR0540T1	Schottky Diode	Motorola	(800) 441-2447
D5	1	MMSD4148T1	Diode	Motorola	(800) 441-2447
E5 to E10	6	2501-2	Terminal Turret	Mill-Max	(516) 922-6000
J1	1	3801-06G2	Pin Header 0.100 (1x6) Connector	COMM CON	(626) 301-4200
JP1, JP6 to JP8, JP10, R13	6	CJ21-000J-T	Shunt Chip 0805	AVX	(843) 946-0362
JP3	1	CR21-9092F-T	90.9k 0.1W 1% Chip Resistor	AVX	(843) 946-0362
Q1	1	Si4936DY	Dual N-Channel MOSFET	Siliconix	(800) 554-5565
Q2	1	IRLML2803	N-Channel MOSFET	IR	(310) 322-3331
Q3	1	MMBT2907LT1	Transistor PNP	Motorola	(800) 441-2447
R1, R11	2	CR21-473J-T	47k 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R2, R5, R15	4	CR21-103J-T	10k 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R3	1	CR21-511J-T	510Ω 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R4, R9, R10	3	CR21-100J-T	10Ω 0.1W 5% Chip Resistor	AVX	(843) 946-0524
R6	1	LR2010-01-R025F	0.025Ω 0.5W 1% Chip Resistor	IRC	(512) 992-7900
R14	1	CRCW08051004F	1M 0.1W 1% Chip Resistor	Dale	(605) 665-9301
T1	1	LPE-6562-A262	Transformer	Dale	(605) 665-9301
TP1, TP2	2	1425-2	Micro Pin Terminal	Keystone	(718) 956-8900
U1	1	LTC1436CGN-PLL	I.C. LTC1436-PLL	LTC	(408) 432-1900

Note: Part locations for C11, C16, C19, JP2, JP4, JP5, JP9, JP11, R7, R8 and R12 are not used on this assembly.

QUICK START GUIDE

DC140 is easily set up for evaluating the LTC1436-PLL. Follow the procedure outlined below for proper operation.

1. Connect the input voltage power supply, output loads and meters as shown in Figure 3. For best accuracy, it is important to connect true RMS reading voltmeters directly to the PCB terminals where the input and output voltages are to be measured. True RMS reading ammeters should also be used for current measurements.
2. Increase the input voltage from 0V to 28V and observe both outputs increase to their regulated voltages. Set the 5V load current to about 0.5A. Note that since the 5V output features a foldback current-limiting circuit, constant-current electronic loads set to 3A will limit the output voltage to a low value when the input voltage is first applied. Reducing the electronic load current setting to about 0.5A or using a resistive load will allow the 5V output to start normally. When the output voltage is greater than 1.5V, the electronic load current can be readjusted to 3A. This is not a problem during normal operation, since most electronic circuits do not require full load current under low input voltage conditions.
3. Connect a pulse generator and oscilloscope between SGND and PLLIN, as shown in Figure 3. Adjust the pulse-generator output for a peak voltage of 2V to 9V, adjust the frequency to about 250kHz and set the duty cycle to about 50%. Note, the circuit will not be damaged if the pulse generator is turned on or off, regardless of whether the input voltage to the DC140 is turned on or turned off.
4. With the pulse generator set for 250kHz and the input voltage applied to DC140, the rising edge of V_{SW}, seen at TP2, will be synchronized to the rising edge of the pulse generator for a wide range of pulse-generator frequencies and duty cycles. Note that the pulse generator duty cycle is not important, provided that the period of the high voltage is 0.2µs or longer and the minimum period for the low voltage is greater than 0.2µs.
5. As an alternate method of controlling the V_{SW} frequency, turn off the pulse generator and connect an adjustable bias supply between SGND and PLL LPF, as shown in Figure 3. Set the oscilloscope to trigger on channel 2 and observe the frequency change as the bias supply voltage is adjusted from 0V to 2.2V. Caution: the **absolute maximum** voltage rating of the PLL LPF pin is 2.7V. Although the DC140 has a 10k protection resistor between the IC and the PLL LPF terminal, the bias supply voltage should never be greater than 2.7V.

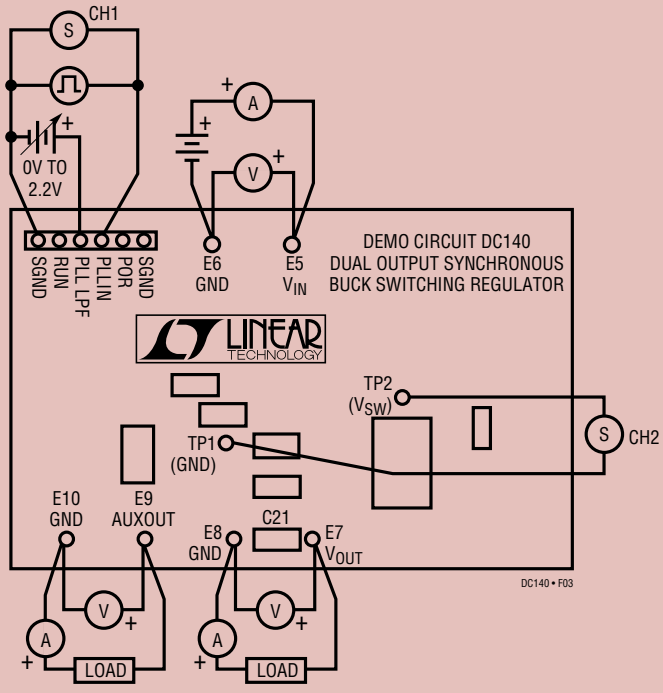


Figure 3. Proper Measurement Setup

OPERATION

The operation of DC140 is best understood by first reading the LTC1436-PLL data sheet.

High Current Switching Circuit

Figures 1 and 2 show the LTC1436-PLL in a synchronous buck configuration that provides a main output voltage of 5V at 3A from an input of 5.5V to 28V. The dual N-channel MOSFET package (Q1) contains the top MOSFET (Q1-1) and bottom MOSFET (Q1-2). A double-package layout configuration is used for the 10µH switch inductor (T1). Version A uses a standard 10µH inductor, since the second output voltage is less than the main output voltage, whereas version B uses the primary of a transformer (also called an overwound inductor) because the second output voltage is greater than the main output voltage. The current sense resistor is R6 and the output capacitors are C13 and C14. Capacitor C21 provides high frequency decoupling across the output terminals.

A short dead time exists before the conduction of each power MOSFET. Diode D4 improves circuit efficiency by ensuring that the internal substrate diode in the bottom MOSFET remains off during this dead time. Since D4 is a Schottky diode, its forward voltage drop is less than the 0.6V required to forward bias the MOSFET's bipolar body diode. Significant shoot-through current occurs if the bottom MOSFET body diode is forward biased when the top MOSFET turns on.

The input-voltage filter capacitors are C3 and C4; R4 and C17 provide local input voltage decoupling near the IC. Capacitor C18 filters the $INTV_{CC}$ bias voltage and provides the energy source for the C8/D3 charge pump, which supplies a boosted voltage that allows the gate drive of the N-channel top MOSFET to be higher than the input voltage.

Low Current Operating Modes

The LTC1436-PLL is a current mode controller that has three low current operating modes: Burst Mode™ operation for highest efficiency under light load current conditions, the Adaptive Power mode for high efficiency and constant switch frequency under light load conditions and the continuous inductor current mode for fast transient response over widely varying load conditions. In the continuous inductor current mode, both the top and bottom power MOSFETs continue to switch at the normal frequency, even when the output current goes to zero. This means that the large gate input capacitances of both power MOSFETs are charged and discharged at the switching frequency even though the output current is zero. This gate-drive power loss significantly decreases circuit efficiency under light load conditions. The highest circuit efficiency is obtained with Burst Mode operation because the power MOSFETs are pulsed in bursts just often enough to maintain the output voltage.

The Adaptive Power mode of operation maintains the normal switching frequency down to less than 1% of maximum load current, with good circuit efficiency. The Adaptive Power mode changes the circuit configuration to a basic buck regulator by turning off both power MOSFETs and using the small SOT-23 size MOSFET (Q2) in place of the top MOSFET (Q1-1) and the diode D4 in place of the bottom MOSFET (Q1-2). Circuit efficiency remains high, since the on-state losses of Q2 and D4 are low due to the light load condition.

The LTC1436-PLL recognizes a light load condition when the peak-to-peak inductor ripple current develops a voltage across R6 that changes from zero to less than 20mV. These voltage levels indicate that the maximum peak inductor ripple current is less than 20% of the nominal DC output current and the minimum peak inductor ripple current is zero. These conditions cause a shift to the low current operating mode when the SFB pin is high. If Q2 is installed, the LTC1436-PLL will operate in the Adaptive Power mode; otherwise it will default to Burst Mode operation.

The SFB pin allows the circuit designer to disable the Adaptive Power and Burst Mode functions. The regulator will operate in the continuous inductor-current mode when the SFB pin voltage is below 1.19V. Pulling the SFB pin above 1.19V will allow the regulator to operate in either the Burst Mode or the Adaptive Power mode under light load conditions. Jumper JP3 allows the SFB pin to be forced low and JP4 allows the SFB pin to be tied high. The SFB pin should always be terminated.

Burst Mode is a trademark of Linear Technology Corporation

OPERATION

Output Voltage Programming

The LTC1436-PLL can be programmed to regulate the main output voltage at 5V or 3.3V without using external feedback resistors. The V_{PROG} pin is a programming pin with a three-state input. A high on the V_{PROG} pin sets the output to 5V and a low sets the output to 3.3V; when the V_{PROG} pin is not connected, the output can be programmed from 1.5V to 9V with external feedback resistors. Jumpers JP5 and JP6 allow either 5V or 3.3V outputs to be programmed. Not installing JP5, JP6 and JP8 allows other output voltages to be programmed using feedback resistor locations R7 and R8. C11 can be used if phase lead is required to improve transient response or loop stability. For output voltages of 5V or more, JP10 should be used to connect the output voltage to $EXTV_{CC}$. For output voltages greater than 6.3V, C21 should be removed or replaced with a higher voltage capacitor.

Control Loop

The LTC1436-PLL uses a transconductance-type error amplifier with a g_m of about 1mS. The output of the error amplifier is brought out on the I_{TH} pin, where most of the loop compensation components are connected. A fraction of the I_{TH} pin voltage is level shifted and used as the current-comparator threshold to which the inductor current is compared. The $SENSE^+$ and $SENSE^-$ pins connect the current comparator to the sense resistor, R6. When the voltage across R6 equals the current comparator threshold voltage, the top MOSFET is turned off. R9, R10 and C15 attenuate any PCB-generated noise in the traces connecting the SENSE pins to R6.

Diode D5 provides foldback current limiting so the output current decreases under short-circuit conditions. Since the error amplifier output ultimately controls load current, the I_{TH} pin voltage can be used to provide additional load current control. When the output voltage is zero, D5 is forward biased, limiting the I_{TH} pin voltage to 0.6V and reducing the output current to about 1A. Full load current will be available before the output reaches 1.5V. Circuits powered by the LTC1436-PLL are not affected by the foldback current limiting feature because they do not require 3A of input current when their input voltage is below 1.5V.

Switching Frequency

The free-running switch frequency of DC140 is about 170kHz and is determined by the value of the capacitance connected to the C_{OSC} pin. Capacitance values from 120pF to 22pF will produce switching frequencies from about 100kHz to about 400kHz. The maximum switching frequency allowed for a given application is the highest frequency that ensures a minimum top MOSFET on-time of greater than 500ns at the highest input voltage. When the LTC1436-PLL senses a top MOSFET on-time less than 500ns, the regulator will start skipping gate-drive pulses, which ultimately cuts the switching frequency in half while continuing to maintain output voltage regulation.

Frequency Synchronization

The switching frequency will synchronize to an external clock applied to the PLLIN pin, provided that the applied clock frequency is within the capture range of the internal phase-locked loop. This capture range is set by the capacitance connected to the C_{OSC} pin and can be determined by measuring the highest switching frequency with 2.4V applied to the PLL LPF pin and the lowest frequency by grounding the PLL LPF pin to SGND.

The PLL LPF pin is the output of the phase detector and the input of the voltage controlled oscillator. The center frequency (f_O) is defined as the frequency that causes a PLL LPF pin voltage of 1.2V. The specified capture range of the phase-locked loop is ±30% of f_O. For applications requiring external frequency synchronization, the C_{OSC} pin capacitor should be selected for a PLL LPF pin voltage close to 1.2V at the synchronizing frequency. For synchronizing to a single frequency, a 10kΩ/0.01μF lowpass filter should be connected between the PLL LPF pin and SGND to smooth the phase-detector output. The values of lowpass filter components are not critical unless the synchronizing frequency changes rapidly and the phase-locked loop tracking rate is important, in which case the values of C1, C2 and R2 can be optimized.

OPERATION

The external clock signal applied to the PLLIN pin should have a low voltage below 0.4V and a high voltage between 2V and 9V. The duty cycle of the external clock signal is not important as long as the minimum pulse width is more than 200ns. The PLLIN pin should be connected to SGND if not used. Resistor R3 biases the PLLIN pin low, so an external SGND connection is not required on DC140 when an external clock signal is not present.

Frequency Modulation

Since the PLL LPF pin is the input of the voltage-controlled oscillator, the switching frequency can be varied from f_O by ±30% by changing the PLL LPF pin voltage from 1.2V by ±0.7V. The frequency extremes are determined by the capacitor connected to the C_{OSC} pin. The frequency deviation can be small or large, as determined by the peak-to-peak modulating voltage. By centering a ramp voltage around 1.2V, the switching frequency can be swept from minimum to maximum at a rate determined by the ramp frequency. The resulting frequency modulation significantly reduces the average conducted and radiated power levels at any fundamental frequency and all harmonic frequencies. Although the peak conducted and radiated EMI levels are the same, the average power at any one frequency is significantly reduced. The reduced average EMI levels decrease the risk of interference with nearby circuits and make it easier to get EMI certification. To experiment with switching frequency modulation, remove JP1 and be careful not to exceed the 2.7V absolute maximum voltage rating of the PLL LPF pin.

RUN/SS

The dual-function RUN/SS pin provides on/off control of both outputs and enables the designer to control the main output current ramp when power is first applied. Using an open-collector or open-drain device to pull the RUN/SS voltage below 0.8V will turn off all IC functions. With this pin open, the IC will start normally with an internal 3μA current source charging the soft start capacitor (C6) to about 6V. The full-load output current ramp is approximately 0.5s/μF, so the soft start current can be adjusted by changing the value of C6. The main output voltage remains zero until the C6 voltage is greater than about 1.3V, so a combination of delay and soft start ramp can be used for output voltage sequencing. If output voltage sequencing and soft start are not required, removing C6 will allow the output voltage to increase almost as fast as the input voltage.

Power-On Reset

The POR pin provides a power-on reset function with an open-drain output. Resistor R1 provides a pull-up to $INTV_{CC}$. The POR voltage is low whenever the output is less than 92.5% of the regulated value or when the RUN/SS pin is low. At startup, the POR pin stays low for an additional 65,536 switching cycles before going high.

Auxiliary Output

The LTC1436-PLL features an additional PNP regulator for a second output. The primary use of this output is for voltages between 2.5V and 12V with current levels up to 0.5A. The AUXON pin of the LTC1436-PLL allows the second output to be enabled with JP7 or disabled with JP9. The AUXON pin should always be terminated. The AUXDR pin provides the base current control of the external PNP pass transistor (Q3), which regulates the output voltage. C20 is the output capacitor. Internal feedback resistors are provided for 12V applications, so the output voltage is connected directly to the AUXFB pin. For output voltages other than 12V, the AUXDR pin voltage must be kept in the range of 2.5V to 8.5V and the AUXFB pin voltage equals 1.19V when the output is in regulation. When used, R12 and R13 are the feedback resistors that step the output voltage down to 1.19V at the AUXFB pin. Capacitor C19 can provide phase lead to the control loop if required.

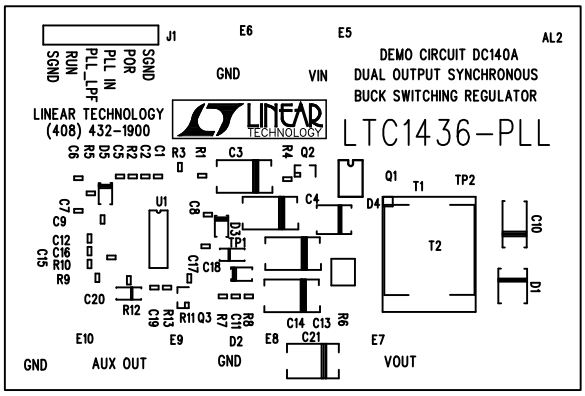
DC140 version A steps down the main output voltage to 3.3V using the auxiliary regulator. Jumper JP2 connects the main output to the input of the pass transistor, Q3. Version B uses a transformer to generate a voltage higher than the main output voltage for a 12V regulated output from the auxiliary regulator. Diode D1 rectifies the transformer secondary current and capacitor C10 filters the secondary voltage that is added to the main output voltage. A trace connects the secondary output to the pass transistor (Q3), so a jumper is not required. Caution: the second output does not have output current limiting.

OPERATION

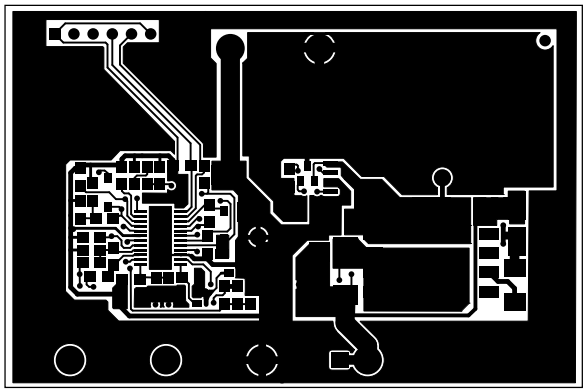
Shorting this output will normally result in a damaged PNP transistor.

Although cost effective, there are limitations to using a transformer to generate secondary output voltages higher than the main output voltage. It is best to keep the regulator duty cycle between 20% and 80% and both output currents should be above 20% of maximum for best regulation. Energy is transferred from the primary inductance to the secondary output only when the top MOSFET is turned off and primary inductor current flows. Discontinuous inductor current stops current flow to the secondary and may cause the 12V output to decrease. R14 and the resistor stuffed at JP3 force continuous inductor-current operation by pulling the SFB pin below 1.19V when the input to the 12V regulator drops too low for regulation. The SFB pin provides optimum circuit efficiency by allowing the regulator to operate in Burst Mode operation or the Adaptive Power mode until the 12V output voltage is in danger. The maximum duty cycle is determined by the 12V load current and varies from about 5.5V to 6V input.

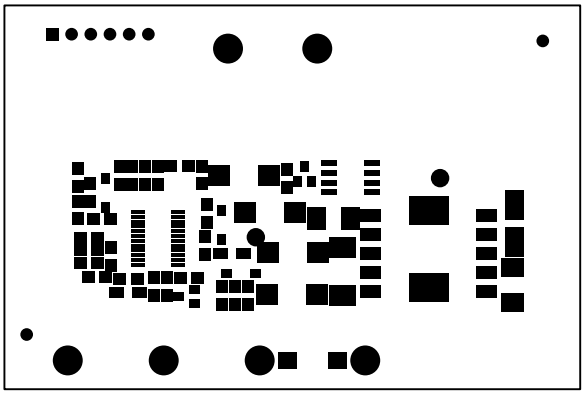
PCB LAYOUT AND FILM



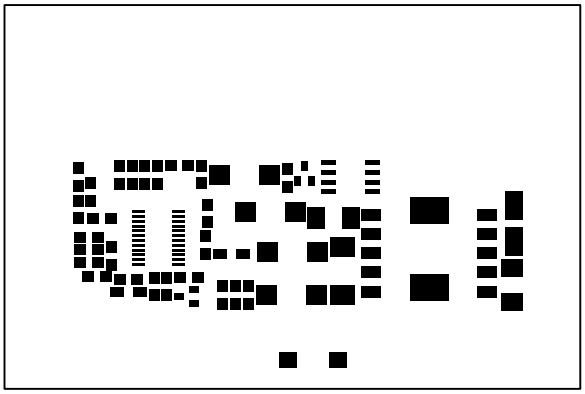
Component Side Silkscreen



Component Side



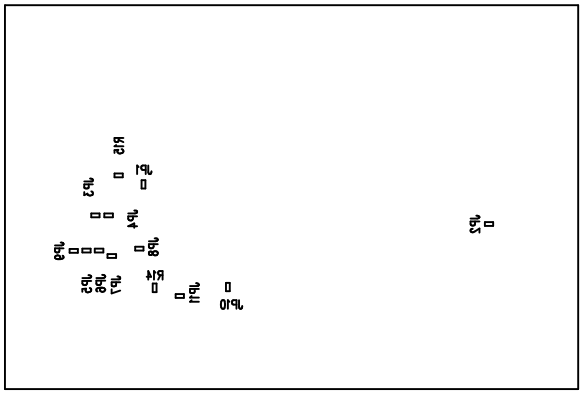
Component Side Solder Mask



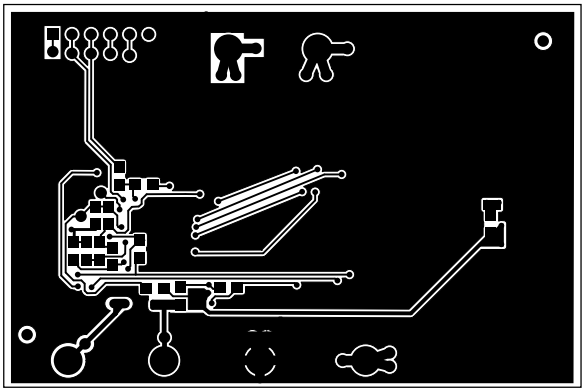
Component Side Paste Mask

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

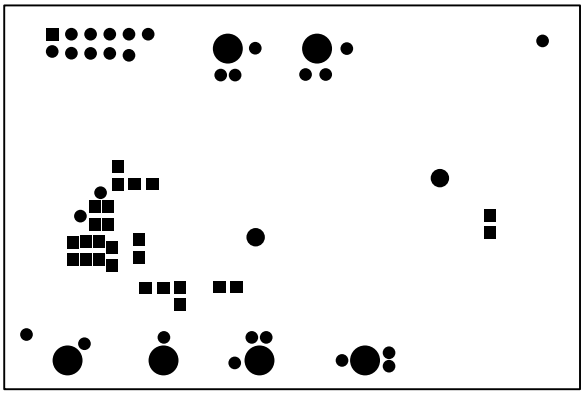
PCB LAYOUT AND FILM



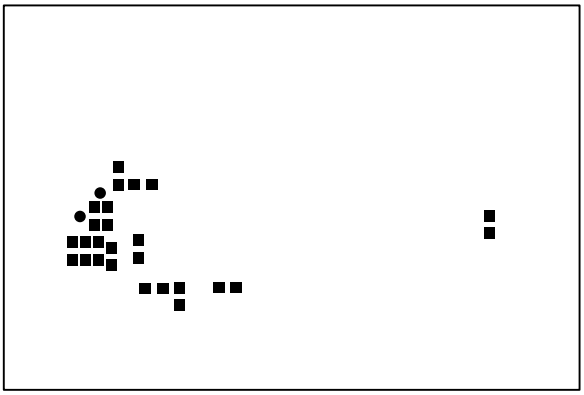
Solder Side Silkscreen



Solder Side

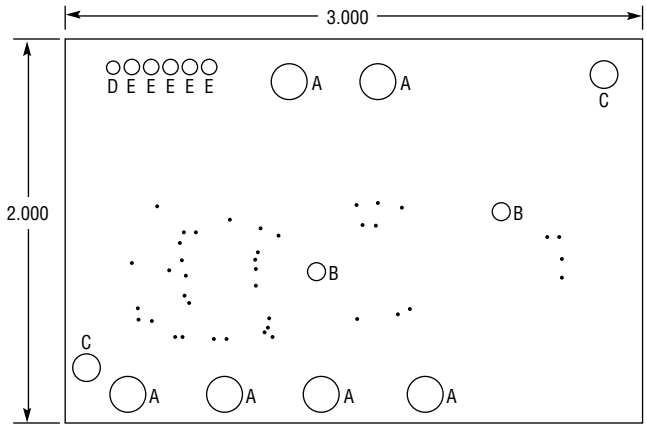


Solder Side Solder Mask



Solder Side Paste Mask

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIAL: FR4, 0.062" THICK WITH 2 OZ COPPER
2. PCB WILL BE DOUBLE SIDED WITH PLATED THROUGH HOLES
3. HOLE SIZES ARE AFTER PLATING. PLATED THROUGH HOLE HOLE WALL THICKNESS MIN 0.0014" (1 OZ)
4. USE SOLDER MASK OVER BARE COPPER PROCESS
5. SOLDER MASK BOTH SIDES WITH LPI GREEN USING FILM PROVIDED
6. SILKSCREEN COMPONENT SIDE USING FILM PROVIDED. USE WHITE, NONCONDUCTIVE INK
7. ALL DIMENSIONS ARE IN INCHES

SYMBOL	DIAMETER	NUMBER OF HOLES
A	0.094	6
B	0.043	2
C	0.070	2 NOT PLATED
D	0.035	1
E	0.040	5
UNMARKED	0.010	40
TOTAL HOLES		56

DC140 • FAB DWG

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
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