



#### DEMO MANUAL DC2419A

## LTC3372EUK

# 4-Channel 8A Configurable Buck Plus Low IQ High Voltage Buck Supply

#### DESCRIPTION

Demonstration circuit 2419A features the LTC®3372 in a multi-output step-down converter. The controller portion of the LTC3372 drives a high output voltage (HV) buck converter which has an input voltage range of 6V to 60V. Its output voltage ( $V_{OUT\_HV}$ ) is nominally 5V but can be configured for either 5V or 3.3V with the  $V_{OUTPRG}$  pin.  $V_{OUT\_HV}$  supplies power to the configurable buck regulator. This regulator provides four low voltage (LV) outputs labelled  $V_{OUT1-4}$ . These outputs are 1.2V/2A, 1.8V/2A, 2.5V/2A and 3.3V/2A respectively. When  $V_{OUT\_HV}$  is configured for 5V, it can supply 6A to the external loads with full load on  $V_{OUT1-4}$ . With no load on  $V_{OUT1-4}$ ,  $V_{OUT\_HV}$  can supply 10A to the external loads. See Figure 3 for the Block Diagram.

The LV buck regulator consists of eight power stages that can be arranged in up to four channels. The LV regulator on the DC2419A is setup for four channels of two power stages each. With modifications, the LV buck regulator can be setup for eight different configurations. See the LV Regulator Configuration section for more details.

If  $V_{OUT\_HV}$  is programmed for 3.3V, then  $V_{OUT4}$  which provides 3.3V/2A will be in dropout. This rail will require an external input voltage to stay in regulation. See the LV Regulator Configuration section for more details.

The LV rails operate at 2MHz and the HV converter operates at one-sixth this frequency or 333kHz. The high frequency of the LV rails allows the use of 4mm  $\times$  4mm inductors. The power stage for the HV converter consists of 60V avalanche rated MOSFETs and a 2.2µH 10mm  $\times$  10mm inductor. A 4m $\Omega$  discrete sense resistor is used to sense current.

The low  $I_Q$  current of the LTC3372 provides high efficiency at light loads. When the  $V_{OUT\_HV}$  is supplying the nominal 5V, its Burst Mode® efficiency with 1mA load is 90.3% for a 12V input, see Figure 9. When the HV converter is off, it only draws 27µA from a 12V input.

Other features of the board include:

- Selectable light load operating modes of:
  - FCM
  - Pulse-skipping (HV) and Burst Mode operation (LV)
  - · Burst Mode operation
- PLLIN pin to synchronize the LV regulators over a 1MHz to 3MHz range (166kHz to 500kHz for the HV converter)
- Watch dog circuit
- TEMP pin to monitor the junction temperature of the LTC3372
- PGOOD pin for the HV converter and RST pin for the LV regulators

The LTC3372 data sheet provides a complete description of the IC operation and application information. The data sheet must be read in conjunction with the quick start quide.

Design files for this circuit board are available at http://www.analog.com/DC2419A

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#### **PERFORMANCE SUMMARY** Specifications are at T<sub>A</sub> = 25°C

Table 1. Performance Summary for the HV Converter ( $T_A = 25$ °C), No Airflow

PARAMETER	CONDITION	VALUE
Minimum Input Voltage (V <sub>IN</sub> )		6V
Maximum Input Voltage (V <sub>IN</sub> )		60V
Output Voltage (V <sub>OUT_HV</sub> )	I <sub>OUT_HV</sub> = 0A to 10A, No load on V <sub>OUT1-4</sub> V <sub>OUTPRG</sub> Tied High	5V ± 2%
Output Voltage (V <sub>OUT_HV</sub> )	$I_{OUT\_HV}$ = 0A to 10A, No load on $V_{OUT1-4}$ $V_{OUTPRG}$ Tied Low	3.3V ± 2%
I <sub>OUT(MAX)</sub> for V <sub>OUT_HV</sub>	$V_{IN}$ = 6V to 60V, $V_{OUT\_HV}$ = 5V or 3.3V No Load on $V_{OUT1-4}$	10A
Nominal Switching Frequency		333kHz
Efficiency See Figures 7 to 10	V <sub>OUT_HV</sub> = 5V, V <sub>IN</sub> = 12V, I <sub>OUT_HV</sub> = 10A V <sub>OUT_HV</sub> = 5V, V <sub>IN</sub> = 48V, I <sub>OUT_HV</sub> = 10A	94.6% Typical 90.6% Typical

Table 2. Performance Summary for the LV Regulators ( $T_A = 25$ °C), No Airflow

PARAMETER	CONDITION	VALUE
Minimum Input Voltage (V <sub>IN_LV</sub> )*		2.25V
Maximum Input Voltage (V <sub>IN_LV</sub> )*		5.5V
Output Voltage V <sub>OUT1</sub>	I <sub>OUT1</sub> = 0A to 2A, V <sub>IN_LV</sub> = 5V or 3.3V	1.2V ± 1%
Output Voltage V <sub>OUT2</sub>	$I_{OUT2} = 0A \text{ to } 2A, V_{IN\_LV} = 5V \text{ or } 3.3V$	1.8V ± 2%
Output Voltage V <sub>OUT3</sub>	I <sub>OUT3</sub> = 0A to 2A, V <sub>IN_LV</sub> = 5V or 3.3V	2.5V ± 3%
Output Voltage V <sub>OUT4</sub>	$I_{OUT4} = 0A$ to 2A, $V_{IN\_LV} = 5V$ Only	3.3V ± 3%
Nominal Switching Frequency		2MHz
Efficiency	$V_{OUT1} = 1.2V, I_{OUT1} = 2A, V_{IN\_LV} = 5V$	79.7% Typical
See Figures 11 to 14	$V_{OUT2} = 1.8V$ , $I_{OUT2} = 2A$ , $V_{IN\_LV} = 5V$	84.7% Typical
	$V_{OUT3} = 2.5V$ , $I_{OUT3} = 2A$ , $V_{IN\_LV} = 5V$	88.0% Typical
	$V_{OUT4} = 3.3V$ , $I_{OUT4} = 2A$ , $V_{IN\_LV} = 5V$	90.4% Typical

 $<sup>^*</sup>V_{IN\_LV}$  and  $V_{OUT\_HV}$  share the same net on the demo board.

#### **QUICK START PROCEDURE**

The evaluation setup for demonstration circuit 2419A is straight forward. Refer to the diagram shown in Figure 1.

Next, follow the procedure below:

- With power off, connect the input supply, load and meters as shown in Figure 1. Preset the loads to 0A and V<sub>IN</sub> supply to be 0V.
- 2) Place the RUN jumper in the ON position and EN1 to EN4 in the off position. Make sure  $V_{OUTPRG}$  is in the 5V position and the PULLUP PWR jumper is in the INTV<sub>CC</sub> position.

- 3) Set the input voltage to 12V.
- Check V<sub>OUT\_HV</sub>. The output voltage should be within the regulation limits shown in the performance summary table for the HV converter.
- 5) Apply 10A load and re-measure  $V_{OUT\_HV}$ . It should be within the same regulation limits.
- 6) Make sure the PULLUP PWR jumper is in the INTV<sub>CC</sub> position. This will ensure the EN pins for the LV regulators can be pulled high for the steps that follow.

- 7) Place EN1 in the ON position.
- 8) Measure V<sub>OUT1</sub>. It should be within the regulation limits shown in the performance summary table for the low voltage regulators.
- 9) Apply 2A load to V<sub>OUT1</sub>. It should be within the same regulation limits.
- 10) Repeat steps 7 to 9 for V<sub>OUT2-4</sub>.
- 11) With 2A load each on  $V_{OUT1-4}$  and 6A load on  $V_{OUT\_HV}$ , measure the input current flowing into  $V_{IN}$  at an input voltage of 12V. It should be less than 4.58A.
- 12) After the basic performance has been verified, the other aspects of performance can be measured and observed.

#### **OUTPUT RIPPLE MEASUREMENT**

When measuring the output voltage or input voltage ripple, be sure to place the probe directly across an output or input capacitor. Figure 2 shows one example. Leads are soldered to either side of the capacitor. The probe's ground ring makes contact with the return lead and the probe tip makes contact with the other lead.

#### **AIRFLOW REQUIREMENTS**

When V<sub>OUT\_HV</sub> is 5V, the demo board can operate with no airflow at room temperature ambient with full load on all outputs for input voltages up to 60V.

When V<sub>OUT\_HV</sub> is 3.3V, airflow will be required with full load on all outputs and high input voltages due to losses in the INTV<sub>CC</sub> LDO. Here are some guidelines to follow:

 $V_{IN}$  = 12V: no airflow

 $V_{IN} = 36V$ : 200 LFM airflow

 $V_{IN} = 48V$ : 400 LFM airflow

#### LV REGULATOR CONFIGURATION

The LV regulator section consists of eight power stages labeled A to H which can be arranged in up to four channels. Each stage consists of a PMOS top FET and NMOS bottom FET and can supply 1A each. The stages are paralleled by tying their input voltages together and SW nodes together. When paralleled, the combined stages can supply N x 1A, where N is the number of parallel stages. Up to four stages can be paralleled.

The LV regulators on the demo board are setup for the 2-2-2-2 configuration. 2-2-2-2 means four channels with two stages each. As indicated, the switch nodes are tied in pairs: SWA and B, SWC and D, SWE and F and SWG and H. Modifying the LV regulation section involves these steps:

- 1) Cutting and jumping the SW traces. The SW pairs mentioned above are all separable. A SW trace in one pair can be tied to a SW trace in another pair by making a cut and jump. Use 28 AWG or similar size wire. Make the cuts and jumps close to the SW pins. To facilitate this, openings in the solder mask were placed over the SW traces next to the SW pins.
- 2) Setting the configuration bits. Pins C1 to C3 are the configuration bits. By tying these pins high or low, different configurations can be programmed. Refer to Table 1 in the data sheet for the complete list of configurations.

#### LV REGULATOR CONFIGURATION

3) If a channel is not used, then tie its FB pin and EN pin to ground. Also remove the inductor.

The  $V_{IN}$  pin for each stage is tied to the output of the HV converter with  $0m\Omega$  jumpers.

Figure 4 and Figure 5 show how to setup the board for two different configurations.

Refer to the Applications Information section of the data sheet for guidance on selecting the output capacitors and inductors when adding or removing a power stage to or from a channel.

For a few cases an external supply may be required for the LV regulators. This could happen for the following reasons:

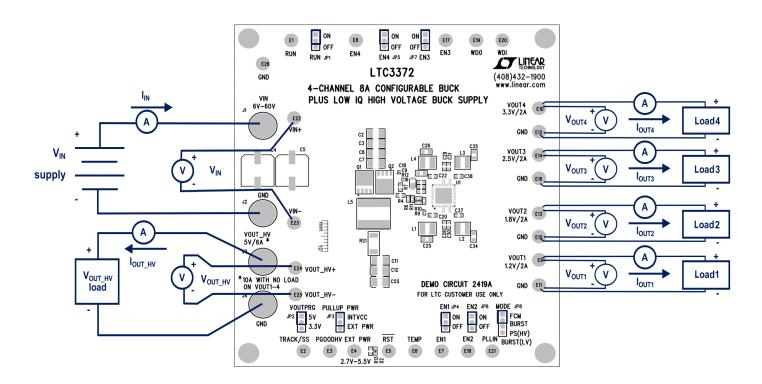
 The HV converter is fed from a supply which does not have sufficient power.

- An external load is drawing too much current from the HV converter.
- A LV regulator needs more headroom.

To supply a LV regulator channel with an external supply, follow these steps:

- Remove the 0mΩ copper jumper tying V<sub>IN\_LV</sub> to the channel's input pins. V<sub>IN\_LV</sub> and V<sub>OUT\_HV</sub> share the same net.
- Place a small bulk capacitor from the input to ground for damping.
- Connect the external supply across this capacitor.

See Figure 6 for more details



NOTE: FOR ACCURATE EFFICIENCY MEASUREMENTS OF THE LV RAILS, MONITOR THEIR OUTPUT VOLTAGE AND INPUT VOLTAGE AT THE FOLLOWING POINTS

CHANNEL #1: V<sub>OUT1</sub>: C25 V<sub>INAB</sub>: C20 OR C28 CHANNEL #2: V<sub>OUT2</sub>: C34 V<sub>INC</sub>, V<sub>IND</sub>: C30 OR C37 CHANNEL #3: V<sub>OUT3</sub>: C35 V<sub>INE</sub>, V<sub>INF</sub>: C38 OR C31 CHANNEL #4: V<sub>OUT4</sub>: C26 V<sub>ING</sub>, V<sub>INH</sub>: C29 AND C22

DC2419a F01

Figure 1. Proper Measurement Setup of the DC2419A

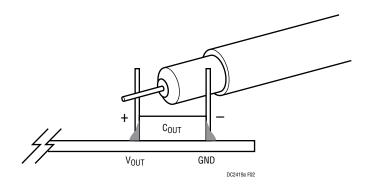


Figure 2. Measuring Output Voltage Ripple

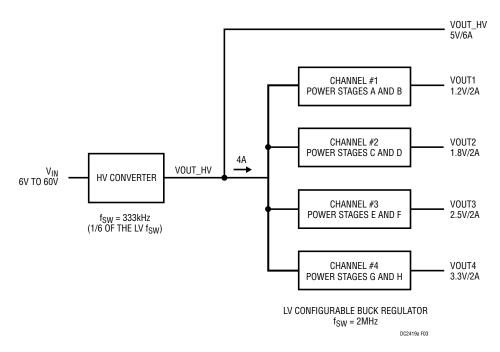
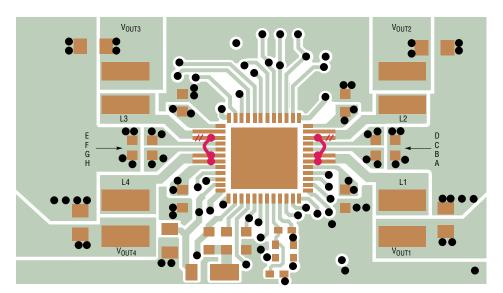
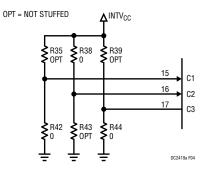


Figure 3. DC2419A Block Diagram

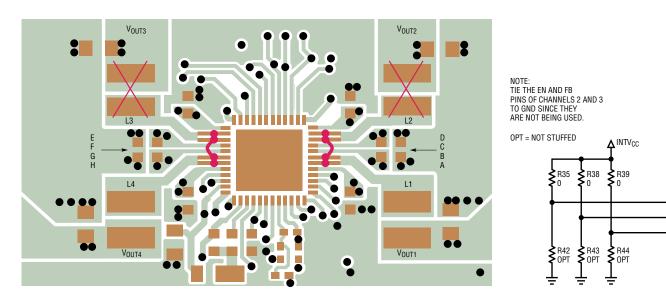




// = CUT

WITH THIS CONFIGURATION, CHANNELS 1 AND 4 PROVIDE 3A OUTPUTS WHILE CHANNELS 2 AND 3 PROVIDE 1A OUTPUTS. THE FOOTPRINTS OF L1 AND L4 CAN BE STUFFED WITH 5mm × 5mm INDUCTORS TO ALLOW HIGHER CURRENT DEVICES TO BE USED. ORIGINAL DESIGN USES 4mm × 4mm INDUCTORS.

Figure 4. DC2419A Setup for the ABC-D-E-FGH Configuration



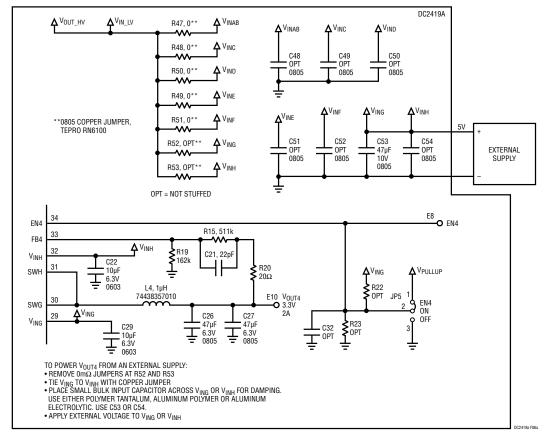
WITH THIS CONFIGURATION, BOTH CHANNELS 1 AND 4 PROVIDE 4A OUTPUTS. CHANNELS 2 AND 3 ARE NOT USED. THE FOOTPRINTS OF L1 AND L4 CAN BE STUFFED WITH 5mm  $\times$  5mm INDUCTORS TO ALLOW HIGHER CURRENT DEVICES TO BE USED. ORIGINAL DESIGN USES 4mm  $\times$  4mm INDUCTORS.

Figure 5. DC2419A Setup for the ABCD- EFGH Configuration

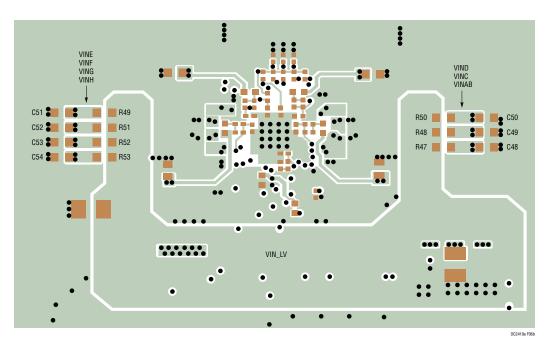
C1

C2 C3

16



(a) Example: Supplying the 3.3V, 2A Rail with an External Voltage



(b) Location of the  $V_{IN\ LV}$  Jumpers and the Optional LV Input Capacitors

Figure 6. How to Connect an External Supply to the Input of a LV Rail

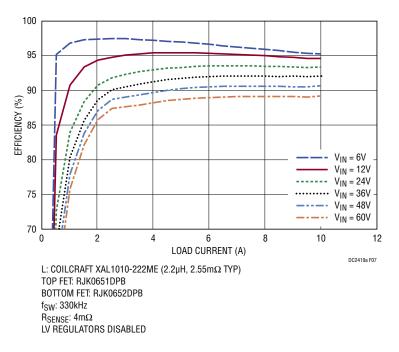


Figure 7. Efficiency of the HV Converter in FCM,  $V_{OUT\ HV} = 5V$ 

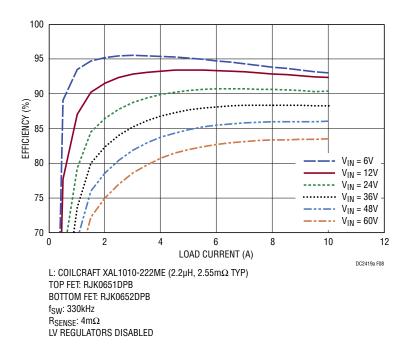


Figure 8. Efficiency of the HV Converter in FCM,  $V_{OUT\ HV} = 3.3V$ 

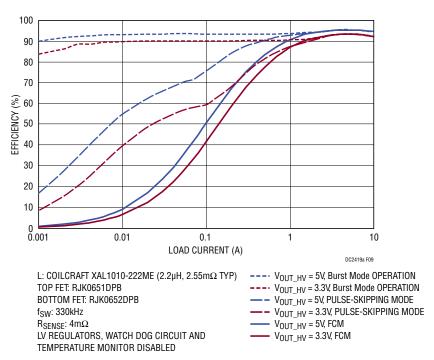


Figure 9. Efficiency of the HV Converter in FCM, Pulse-Skipping and Burst Mode Operation,  $V_{IN} = 12V$ 

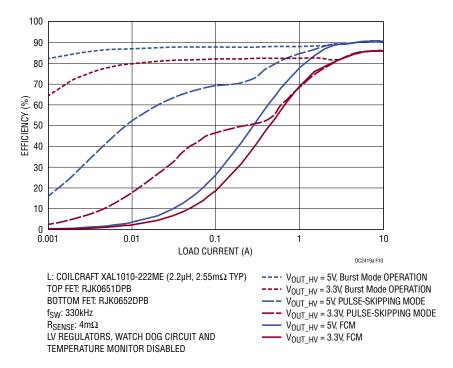


Figure 10. Efficiency of the HV Converter in FCM, Pulse-Skipping and Burst Mode Operation,  $V_{IN} = 48V$ 

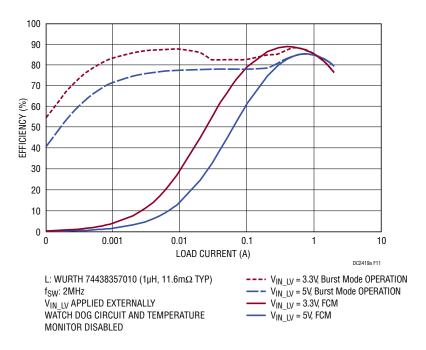


Figure 11. Efficiency of the 1.2V, 2A LV Rail (V<sub>OUT1</sub>)

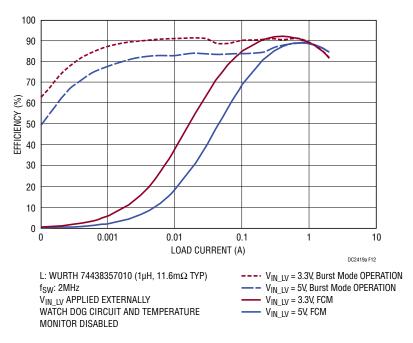


Figure 12. Efficiency of the 1.8V, 2A LV Rail (V<sub>OUT2</sub>)

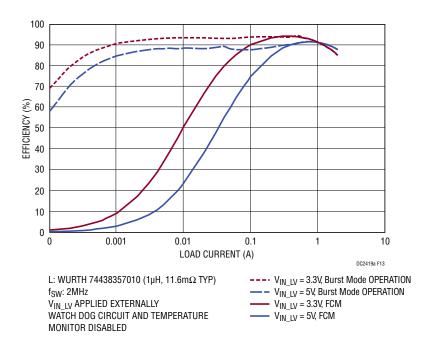


Figure 13. Efficiency of the 2.5V, 2A LV Rail (V<sub>OUT3</sub>)

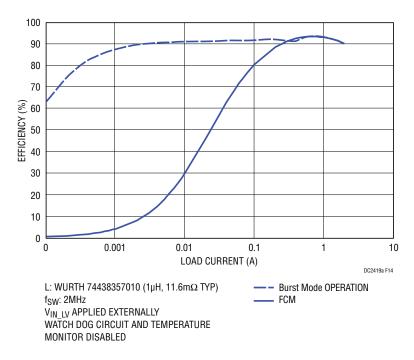
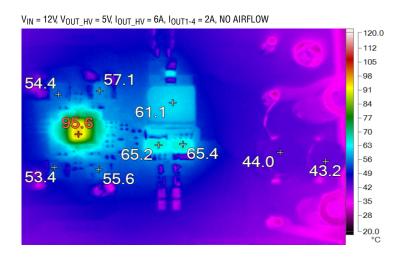
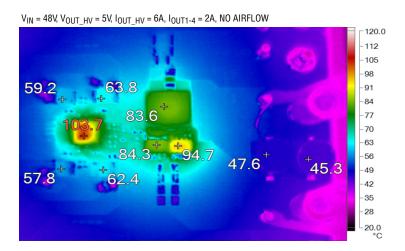


Figure 14. Efficiency of the 3.3V, 2A LV Rail ( $V_{OUT4}$ ),  $V_{IN\_LU}$  = 5V





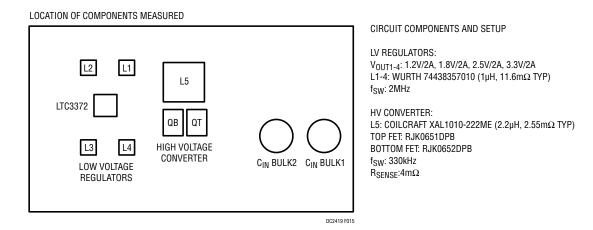
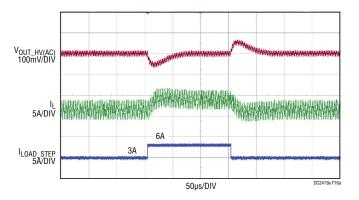
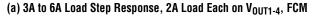
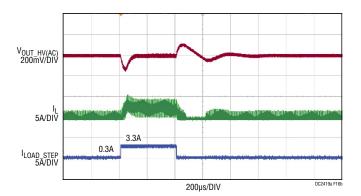


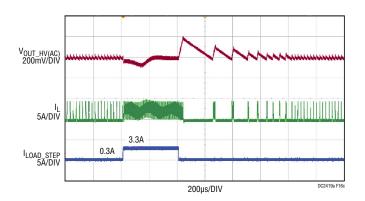
Figure 15. Thermal Image of the DC2419A Demo Board with Full Load on All Rails







(b) 0.3A to 3.3A Load Step Response, No Load on V<sub>OUT1-4</sub>, Pulse-Skipping Mode



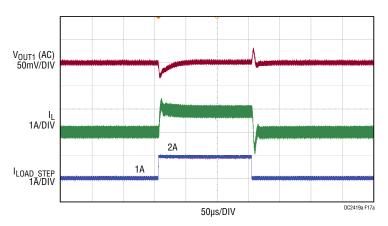
(c) 0.3A to 3.3A Load Step Response, No Load on  $V_{OUT1-4}$ , **Burst Mode Operation** 

 $C_{OUT(BULK)}\!\!: 2x\,T520B157M006ATE025 \\ (150\mu F,\,6.3V,\,25m\Omega)$ 

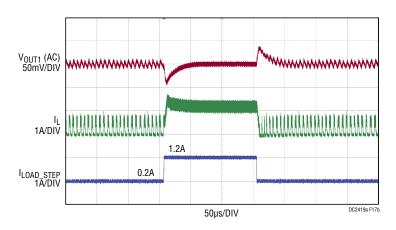
 $C_{OUT(CER)}$ : TMK325ABJ476MM-T (47 $\mu$ F, 25V, X5R, 1210)

f<sub>SW</sub>: 330kHz

Figure 16. Load Step Response of the HV Converter ( $V_{OUT\ HV}$ ),  $V_{OUT\ HV}$  = 5V,  $V_{IN}$  = 12V



(a) 1A to 2A Load Step Response, FCM



(b) 0.2A to 1.2A Load Step Response, Burst Mode Operation

 $C_{OUT}$ : 2× GRM21BR60J476ME15L (47 $\mu$ F, 6.3V, X5R, 0805)

f<sub>SW</sub>: 2MHz

Figure 17. Load Step Response of the LV 1.2V, 2A Regulator ( $V_{OUT1}$ ),  $V_{IN\_LV}$  = 5V

# **PARTS LIST**

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Require	d Circu	iit Components		
1	1	C10	CAP, 0.01µF 10% 25V X7R 0402	MURATA, GRM155R71E103KA01J
2	1	C39	CAP, 0.01µF 10% 50V X7R 0402	MURATA, GRM155R71H103KA88D
3	3	C9, C16, C46	CAP, 0.1µF 10% 100V X7R 0603	MURATA, GRM188R72A104KA35D
4	1	C17	CAP, 1000pF 5% 50V NP0 0402	MURATA, GRM1555C1H102JA01D
5	9	C20, C22, C28 TO C31, C37, C38, C47	CAP, 10µF 20% 16V X5R 0603	MURATA, GRM188R61C106MA73D
6	2	C7, C8	CAP, 2.2µF 10% 100V X7R 1210	MURATA, GRM32ER72A225KA35L
7	1	C15	CAP, 220pF 5% 25V NPO 0402	YAGEO, CC0402JRNP08BN221
8	3	C21, C40, C41	CAP, 22pF 5% 50V NPO 0402	MURATA, GRM1555C1H220JA01D
9	2	C12, C55	CAP, 3528 150µF 6.3V POLY TANT	KEMET, T520B157M006ATE025
10	1	C18	CAP, 4.7µF 10% 25V X5R 0805	MURATA, GRM21BR61E475KA12L
11	1	C19	CAP, 47pF 5% 50V NPO 0402	MURATA, GRM1555C1H470JA01D
12	1	C11	CAP, 47µF 20% 1210 25V X5R	TAIYO YUDEN, TMK325ABJ476MM-T
13	8	C24 TO C27, C33 TO C36	CAP, 47µF 20% 6.3V X5R 0805	MURATA, GRM21BR60J476ME15L
14	2	C4, C5	CAP, 47µF 63V, 30mW, 2.1A RMS	SUNCON ELEC, 63HVH47M
15	1	C14	CAP, 6800pF 10% 50V X7R 0402	YAGEO, AC0402KRX7R9BB682
16	1	D1	DIODE, SCHOTTKY 100V	DIODES INC, DFLS1100-7
17	1	U1	IC LTC3372EUK	ADI, LTC3372EUK#PBF
18	4	L1 T0 L4	IND, 1µH 7.4A 13.5mW	WURTH ELEKTRONIK, 74438357010
19	1	L5	IND, 2.2µH 32.0A 2.55mW	COILCRAFT, XAL1010-222MEB
20	6	R47 TO R53	JUMPER, 0mW 0805	TEPRO, RN61
21	1	Q1	MOSFET, N-CH 60V 25A LFPAK	RENESAS, RJK0651DPB-00#J5
22	1	Q2	MOSFET, N-CH 60V 35A LFPAK	RENESAS, RJK0652DPB-00#J5
23	4	R10, R42, R43, R44	RES, 0W, 0402	VISHAY, CRCW04020000Z0ED
24	1	R58	RES, 0W, 0603	VISHAY, CRCW06030000Z0EA
25	4	R54, R26, R45, R46	RES, 100k 1% 0603	VISHAY, CRCW0603100KFKEA
26	3	R3, R32, R41	RES, 10k 5% 0603	VISHAY, CRCW060310K0JNEA
27	1	R9	RES, 10W, 5% 0402	VISHAY, CRCW040210R0JNED
28	1	R19	RES, 162k 1% 0402	VISHAY, CRCW0402162KFKED
29	1	R7	RES, 2.2W 1% 0603	VISHAY, CRCW06032R20FKEA
30	1	RS1	RES, 2010 4mW 1% 1W	VISHAY, WSL20104L000FEA
31	4	R17, R28, R20, R25	RES, 20W 1% 0603	VISHAY, CRCW060320R0FKEA
32	1	R14	RES, 232k 1% 0402	VISHAY, CRCW0402232KFKED
33	1	R12	RES, 3.3W 1% 0603	VISHAY, CRCW06033R30FKEA
34	1	R27	RES, 309k 1% 0402	VISHAY, CRCW0402309KFKED
35	1	R8	RES, 4.02k, 1% 0402	VISHAY, CRCW04024K02FKED
36	1	R34	RES, 402k 1% 0402	VISHAY, CRCW0402402KFKED
37	1	R18	RES, 464k 1% 0402	VISHAY, CRCW0402464KFKED
38	1	R15	RES, 511k 1% 0402	VISHAY, CRCW0402511KFKED
39	1	R30	RES, 649k 1% 0402	VISHAY, CRCW0402649KFKED
40	1	R24	RES, 66k 1% 0402	VISHAY, CRCW0402665KFKED
41	1	R29	RES, 806K 1% 0402	VISHAY, CRCW0402806KFKED

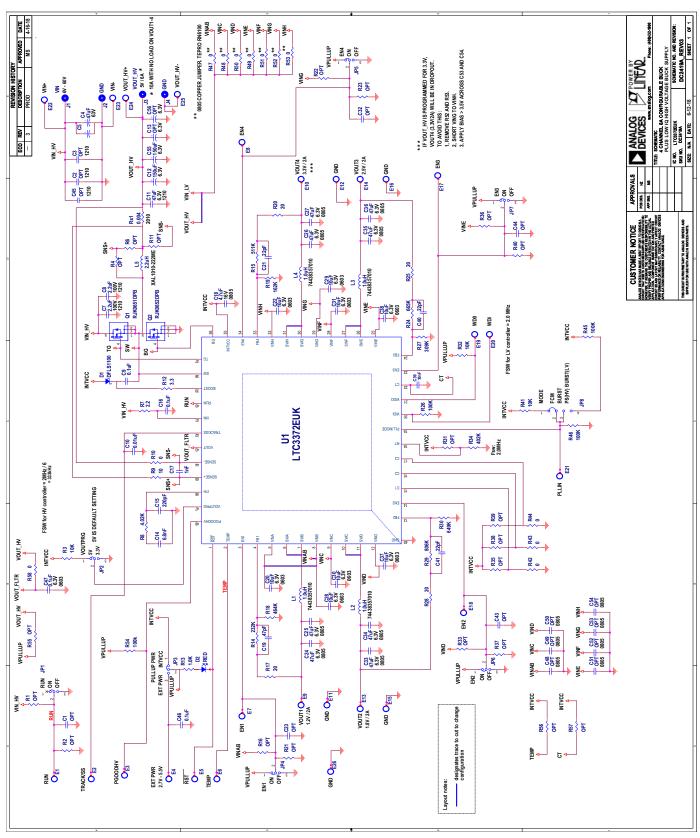
UG-1377 Rev 0

# DEMO MANUAL DC2419A

# **PARTS LIST**

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER		
Addition	Additional Demo Board Circuit Components					
1	0	C1, C23, C32, C43, C44	CAP, 0402 OPT			
2	0	C48 TO C54	CAP, 0805 OPT			
3	0	C2, C3	CAP, 1210 OPT			
4	0	C13, C56	CAP, 3528 OPT			
5	1	D2	LED, RED	WURTH ELEKTRONIK, 150060RS75000		
6	1	R13	RES, 1k 1% 0603	VISHAY, CRCW06031K00FKEA		
7	0	R1, R2, R4, R6, R11, R16, R21, R22, R23, R31, R33, R35 T0 R40, R55 T0 R57	RES, OPTIONAL			
Hardwa	Hardware: For Demo Board Only					
1	7	JP1 TO JP7	HEADER, SINGLE ROW 3PIN	WURTH ELEKTRONIK 62000311121		
2	1	JP8	HEADER, SINGLE ROW 4PIN	WURTH ELEKTRONIK 62000411121		
3	4	J1, J2, J3, J4	JACK, BANANA	KEYSTONE, 575-4		
4	8	XJP1 TO XJP8	SHUNT	WURTH ELEKTRONIK 60800213421		
5	4		STANDOFF, NYLON, SNAP-ON, 0.375"	WURTH ELEKTRONIK 702933000		
6	26	E1 TO E26	TURRET	MILL MAX 2501-2-00-80-00-00-07-0		

#### SCHEMATIC DIAGRAM



#### DEMO MANUAL DC2419A



#### **ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

#### **Legal Terms and Conditions**

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board shall signify your acceptance of the Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board For EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI. Customer, their employees, affiliates and in-house consultants. The Evaluation Board is considered the conflidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or re

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