56F803

Evaluation Module User Manual

56F800
16-bit Digital Signal Controllers

DSP56F803EVMUM
Rev. 5
07/2005

freescale.com

freescale™
semiconductor

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Preface

This reference manual describes in detail the hardware on the 56F803 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F803 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction -** provides an overview of the 56F803EVM and its features.
- **Chapter 2, Technical Summary -** describes in detail the 56F803EVM hardware.
- **Appendix A, 56F803EVM Schematics -** contains the schematics of the 56F803EVM.
- **Appendix B, 56F803EVM Bill of Material -** provides a list of the materials used on the 56F803EVM board.

Suggested Reading

More documentation on the 56F803 and the 56F803EVM kit may be found at the URL:

http://www.freescale.com

Notation Conventions

This document uses the following conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{WE}$ $\overline{OE}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a “$” symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter “b” attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Bold	Reference sources, paths, emphasis	...see: **www.freescale.com**...	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

A/D	Analog-to-Digital
CAN	Controller Area Network; serial communications peripheral and method
CiA	CAN in Automation, an international CAN user's group that coordinates standards for CAN communications protocols
EVM	Evaluation Module
GPIO	General Purpose Input and Output Port
IC	Integrated Circuit
JTAG	Joint Test Action Group, a bus protocol/interface used for test and debug
LQFP	Low-profile Quad Flat Pack
MPIO	Multi Purpose Input and Output Port; shares package pins with other peripherals on the chip and can function as a GPIO
OnCE™	On-Chip Emulation, a debug bus and port created by Freescale to enable designers to create a low-cost hardware interface for a professional quality debug environment
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface Port
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter

References

The following sources were referenced to produce this manual:

[1] *DSP56800 Family Manual*, Freescale Semiconductor, DSP56800FM

[2] *DSP56F801/803/805/807 User's Manual*, Freescale Semiconductor, DSP56F801-7UM

[3] *56F803 Technical Data*, Freescale Semiconductor, DSP56F803

[4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation

[5] CAN Specification 2.0B, BOSCH or CAN in Automation

Chapter 1
Introduction

The 56F803EVM is used to demonstrate the abilities of the 56F803 and to provide a hardware tool allowing the development of applications that use the 56F803.

The 56F803EVM is an evaluation module board that includes a 56F803 part, peripheral expansion connectors, external memory, RS-232 interface and a CAN interface. The expansion connectors are for signal monitoring and user feature expandability.

The 56F803EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the 56F803EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full-speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the controller's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the chip are available to the user.

1.1 56F803EVM Architecture

The 56F803EVM facilitates the evaluation of various features present in the 56F803 part. The 56F803EVM can be used to develop real-time software and hardware products based on the 56F803. The 56F803EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The 56F803EVM is flexible enough to allow a user to fully exploit the 56F803's features to optimize the performance of their product, as shown in **Figure 1-1**.

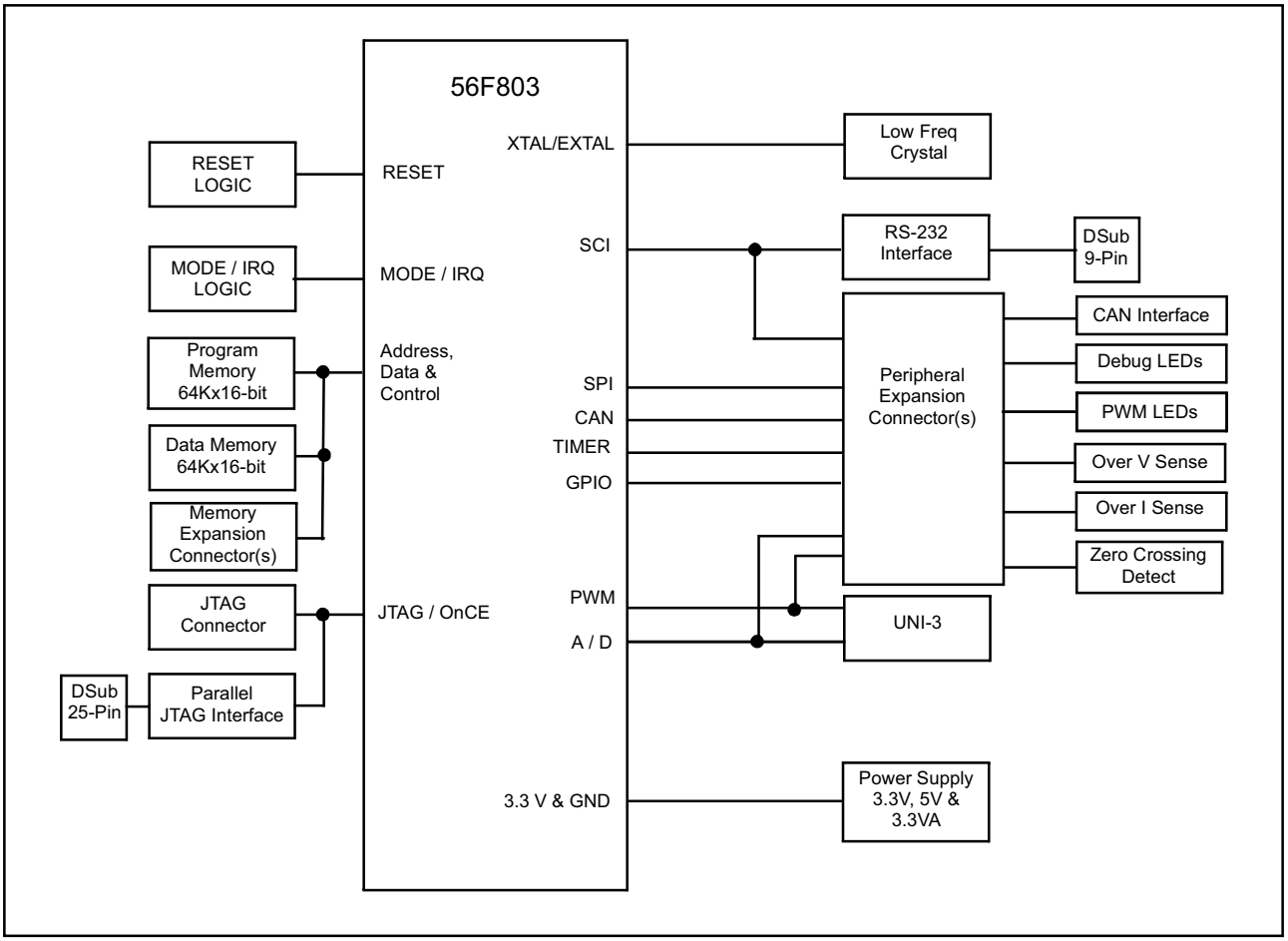

Figure 1-1. Block Diagram of the 56F803EVM

1.2 56F803EVM Configuration Jumpers

Ten jumper groups, (JG1-JG10), shown in **Figure 1-2**, are used to configure various features on the 56F803EVM board. **Table 1-1** describes the default jumper group settings.

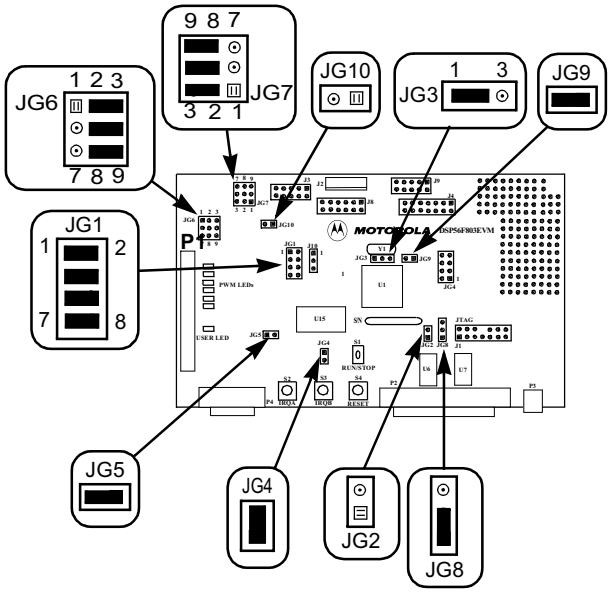

Figure 1-2. 56F803EVM Jumper Reference

Table 1-1. 56F803EVM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	UNI-3 serial selected	1–2, 3–4, 5–6 & 7–8
JG2	Enable on-board Parallel JTAG Command Converter Interface	NC
JG3	Use on-board crystal for oscillator input	1–2
JG4	Selects device's Mode 0, BOOT From FLASH, operation upon exit from reset	1–2
JG5	Enable external SRAM	1–2
JG6	UNI-3 3-Phase Current Source Selected	2–3, 5–6 & 8–9
JG7	Encoder Input Selected	2–3, 5–6 & 8–9
JG8	On-board Parallel JTAG Command Converter powered by Host System	1-2
JG9	Use on-board crystal for oscillator input	1–2
JG10	Leave CAN bus un-terminated	NC

1.3 56F803EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12V DC power supply to the 56F803EVM board.

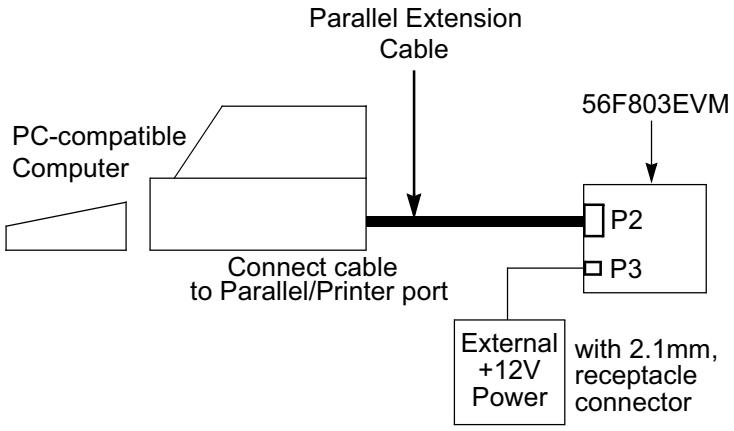

Figure 1-3. Connecting the 56F803EVM Cables

Perform the following steps to connect the 56F803EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer.
2. Connect the other end of the parallel extension cable to P2, shown in **Figure 1-3**, on the 56F803EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 4.0A power supply is not plugged into a +120V AC power source.
4. Connect the 2.1mm output power plug from the external power supply into P3, shown in **Figure 1-3**, on the 56F803EVM board.
5. Apply power to the external power supply. The green Power-On LED will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The 56F803EVM is designed as a versatile controller development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, servo and motor control, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F803 controller, combined with the on-board 64K × 16-bit external program Static RAM (SRAM), 64K × 16-bit external data SRAM, CAN interface, Hall-Effect/Quadrature Encoder interface, motor zero crossing logic, motor bus over-current logic, motor bus over-voltage logic and parallel JTAG interface, makes the 56F803EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F803 processor.

The main features of the 56F803EVM include:

- 56F803 16-bit +3.3V controller operating at 80MHz [U1]
- External fast Static RAM (FSRAM) memory [U2], configured as:
  - 64K×16-bit of Program memory with 0 wait states at 70MHz
  - 64K×16-bit of Data memory with 0 wait states at 70MHz
- 8.00MHz crystal oscillator for device frequency generation [Y1]
- Optional external oscillator frequency input connector [JG3 and JG9]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J1]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P2]
- RS-232 interface for easy connection to a host processor [U3 and P4]
- CAN interface for high speed, 1.0Mbps, communications [U15 and J3]
- CAN bypass and bus termination [J13 and JG10]
- Connector to allow the user to connect his own SCI / GPIO-compatible peripheral [J12]
- Connector to allow the user to connect his own SPI / MPIO-compatible peripheral [J6]
- Connector to allow the user to connect his own PWM / GPIO-compatible peripheral [J4]
- Connector to allow the user to connect his own CAN physical layer peripheral [J5]
- Connector to allow the user to connect his own Timer / MPIO-compatible peripheral [J10]

- Connector to allow the user to connect to the device's A/D Port [J9]
- 56F803's external memory expansion connectors [J7, J8 and J11]
- On-board power regulation from an external +12V DC-supplied power input [P3]
- Light Emitting Diode (LED) power indicator [LED1]
- Six on-board PWM monitoring LEDs [LED2-LED7]
- On-board real-time user debugging LED [LED8]
- UNI-3 Motor interface [P1]
  - Encoder/Hall-Effect interface
  - Over-Voltage sensing [U14]
  - Over-Current sensing [U14]
  - DC Bus Voltage sensing [U13]
  - DC Bus Current sensing [U13]
  - Back-EMF sensing
  - Temperature sensing
  - Zero Crossing detection
  - Pulse Width Modulation
  - Power Factor Correction (PFC) sensing
- Manual RESET push-button [S4]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push-button for $\overline{\text{IRQB}}$ [S3]
- General purpose toggle switch for RUN/STOP control(AN7) [S1]

2.1 56F803

The 56F803EVM uses a Freescale DSP56F803BU80 part, designated as U1 on the board and in the schematics. This part will operate at a maximum speed of 80MHz. A full description of the 56F803, including functionality and user information, is provided in the following documents:

- 56F803 *Technical Data*, (DSP56F803)**:** Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements and available packaging.

- *DSP56F801/803/805/807 User's Manual*, (DSP56F801-7UM): Provides an overview description of the controller and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control/status register descriptions for each subsystem.
- *DSP56800 Family Manual*, (DSP56800FM): Provides a detailed description of the core processor including internal status and control registers and a detailed description of the family instruction set.

These manuals contain detailed information about chip functionality and operation and can be found at this URL:

http://www.freescale.com

2.2 Program and Data Memory

The 56F803EVM uses one bank of 128K×16-bit Fast Static RAM (GSI GS72116, labeled U2) for external memory expansion; see the FSRAM schematic diagram in Figure 2-1. This physical memory bank is split into two logical memory banks of 64Kx16-bits: one for Program memory and the other for Data memory. By using the device's program strobe, $\overline{PS}$, signal line along with the memory chip's A0 signal line, half of the memory chip is selected when Program memory accesses are requested and the other half of the memory chip is selected when Data memory accesses are requested. This memory bank will operate with zero wait-state accesses while the 56F803 is running at 70MHz. However, when running at 80MHz, the memory bank operates with four wait-state accesses. This memory bank can be disabled by removing the jumper at JG5.

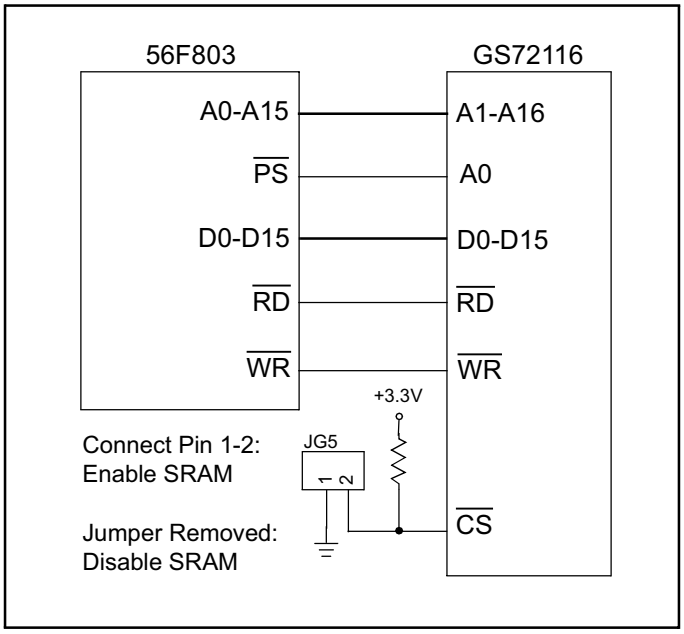

Figure 2-1. Schematic Diagram of the External Memory Interface

2.3 RS-232 Serial Communications

The 56F803EVM provides an RS-232 interface by the use of an RS-232 level converter, (Analog Devices ADM3311EARS, designated as U3); refer to the RS-232 schematic diagram in Figure 2-2. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232 compatible signal levels and connects to the host's serial port via connector P4. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The pin-out of connector P4 is listed in Table 2-1.

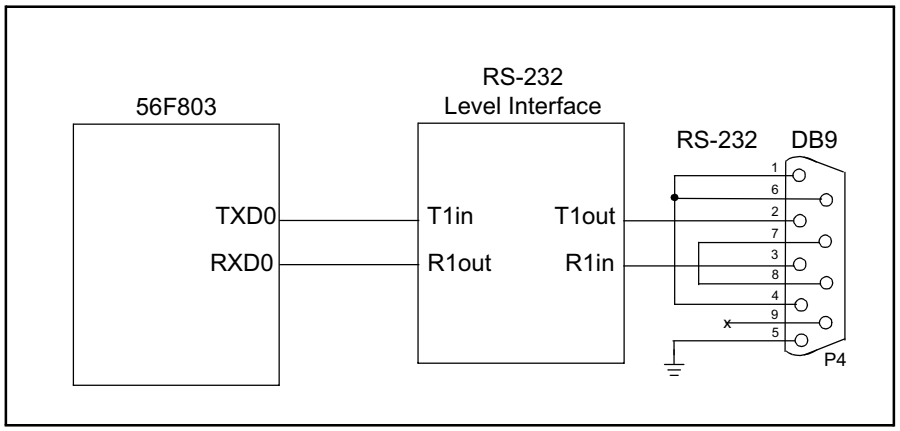

Figure 2-2. Schematic Diagram of the RS-232 Interface

Table 2-1. RS-232 Serial Connector Description

P4			
Pin #	**Signal**	**Pin #**	**Signal**
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD	7	Jumper to 8
3	RXD	8	Jumper to 7
4	Jumper to 1 & 6	9	N/C
5	GND		

2.4 Clock Source

The 56F803EVM uses an 8.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. The 56F803 uses its internal PLL to multiply the input frequency by 10 to achieve its 80MHz maximum operating frequency. An external oscillator source can be connected to the controller by using the oscillator bypass connectors, JG3 and JG9; see Figure 2-3.

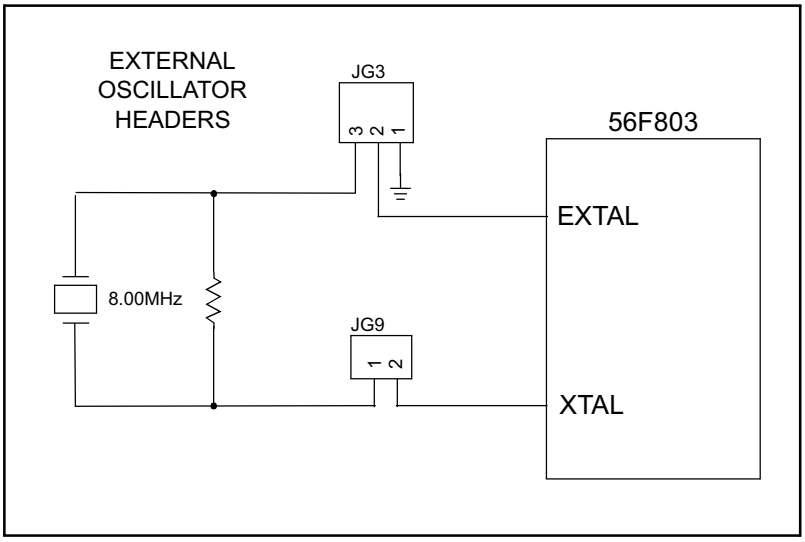

Figure 2-3. Schematic Diagram of the Clock Interface

2.5 Operating Mode

The 56F803EVM provides a boot-up MODE selection jumper, JG4. This jumper is used to select the operating mode of the controller as it exits RESET. Refer to the DSP56F801-7 User's Manual for a complete description of the chip's operating modes. Table 2-2 shows the two operation modes available on the 56F803.

Table 2-2. Operating Mode Selection

Operating Mode	JG4	Comment
0	1–2	Bootstrap from internal memory (GND)
3	No Jumper	Bootstrap from external memory (+3.3V)

2.6 Debug LED

An on-board Light-Emitting Diode, (LED), is provided to allow real-time debugging for user programs. This LED allows the programmer to monitor program execution without having to stop the program during debugging; refer to Figure 2-4. LED8 is controlled by the MOSI signal line. Setting MOSI to a Logic One value will turn on the LED.

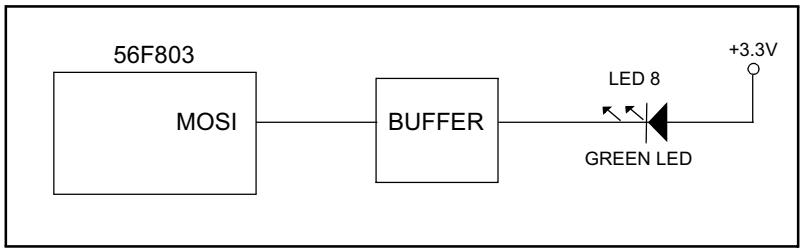

Figure 2-4. Schematic Diagram of the Debug LED Interface

2.7 Debug Support

The 56F803EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Host Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.7.1 JTAG Connector

The JTAG connector on the 56F803EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F803's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. Table 2-3 shows the pin-out for this connector.

Table 2-3. JTAG Connector Description

J1			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	NC	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG2. Reference Table 2-4 for this jumper's selection options.

Table 2-4. Parallel JTAG Interface Disable Jumper Selection

JG2	Comment
No jumper	On-board Parallel JTAG Interface Enabled
1–2	Disable on-board Parallel JTAG Interface

2.7.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P2, allows the 56F803 to communicate with a Parallel Printer Port on a Windows PC; see Figure 2-5. By using this connector, the user can download programs and work with the 56F803's registers. Table 2-5 shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG2 should be removed; refer to Table 2-4. A jumper, JG8, is provided to allow the on-board Host Target Interface to be powered by the Target board instead of the Host system, as shown in Table 2-6.

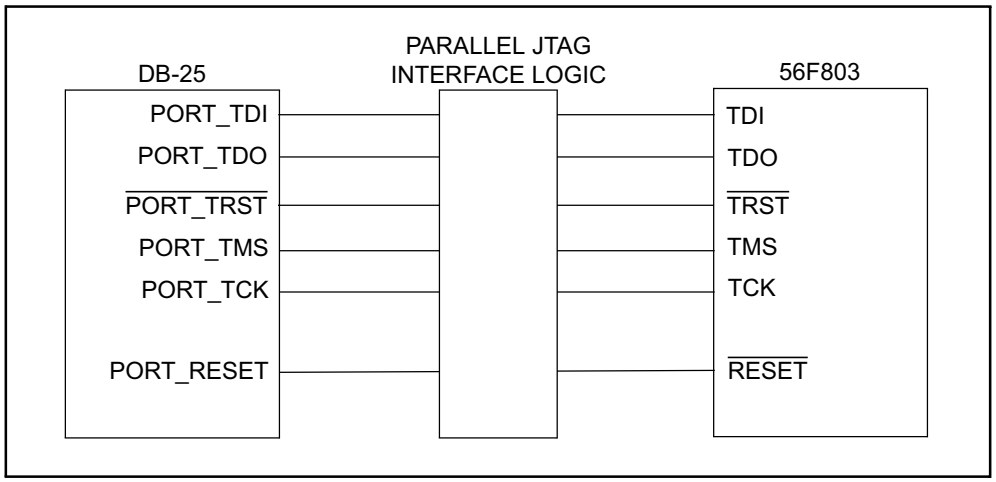

Figure 2-5. Block Diagram of the Parallel JTAG Interface

Table 2-5. Parallel JTAG Interface Connector Description

P2			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	NC
4	PORT_TCK	17	NC
5	PORT_TDI	18	GND
6	PORT_TRST	19	GND
7	NC	20	GND
8	PORT_IDENT	21	GND
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

Table 2-6. On-Board Host Target Interface Power Source Jumper Selection

JG8	Comment
1–2	Host supplied power
2–3	Target supplied power

2.8 External Interrupts

Two on-board push-button switches are provided for external interrupt generation, as shown in Figure 2-9. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$.; S3 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

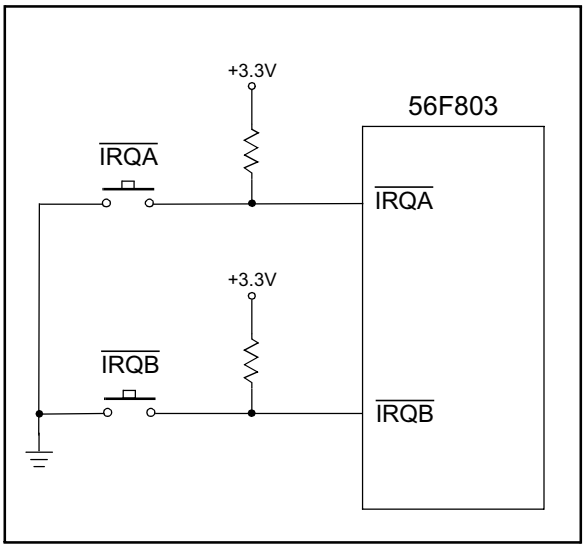

Figure 2-6. Schematic Diagram of the User Interrupt Interface

2.9 Reset

Logic is provided in the 56F803 to generate a clean power-on RESET signal. Additional, reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button; see Figure 2-7.

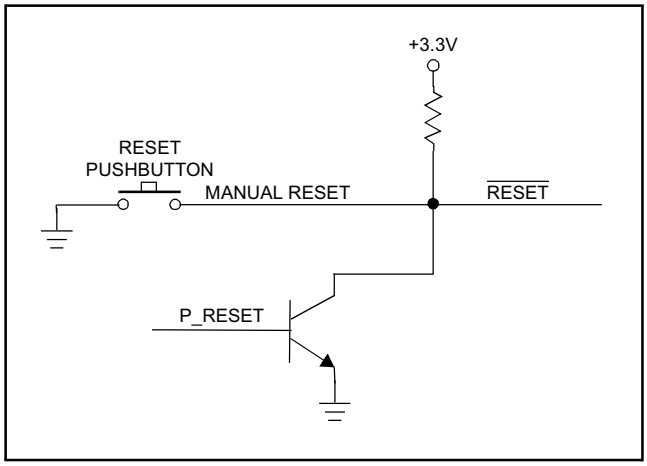

Figure 2-7. Schematic Diagram of the RESET Interface

2.10 Power Supply

The main power input, +12V DC at 4.0A, to the 56F803EVM is through a 2.1mm coax power jack. A 4.0A power supply is provided with the 56F803EVM; however, less than 500mA is required by the EVM. The remaining current is available for user motor control applications. The 56F803EVM provides +3.3V DC voltage regulation for the device, memory, RS-232, CAN, parallel JTAG interface and supporting logic; refer to Figure 2-8. Power applied to the 56F803EVM is indicated with a Power-On LED, referenced as LED1.

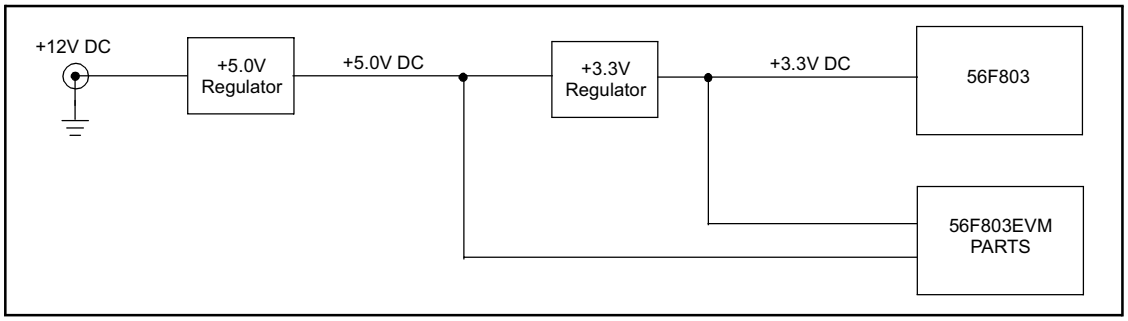

Figure 2-8. Schematic Diagram of the Power Supply

2.11 UNI-3 Interface

Motor control signals from a family of motor driver boards can be connected to the EVM board via the UNI-3 connector/interface. The UNI-3 connector/interface contains all of the signals needed to drive and control the motor drive boards. These signals are connected to differing groups of the device's input and output ports: A/D, TIMER and PWM. Refer to Table 2-7 for the pin out of the UNI-3 connector.

Table 2-7. UNI-3 Connector Description

P1			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWM_AT	2	Shield
3	PWM_AB	4	Shield
5	PWM_BT	6	Shield
7	PWM_BB	8	Shield
9	PWM_CT	10	Shield
11	PWM_CB	12	GND
13	GND	14	+5.0V DC
15	+5.0V DC	16	Analog +3.3V DC
17	Analog GND	18	Analog GND
19	Analog +15V DC	20	Analog -15V DC
21	Motor DC Bus Voltage Sense	22	Motor DC Bus Current Sense
23	Motor Phase A Current Sense	24	Motor Phase B Current Sense
25	Motor Phase C Current Sense	26	Motor Drive Temperature Sense
27	NC	28	Shield
29	Motor Drive Brake Control	30	Serial COM
31	PFC PWM	32	PFC Inhibit
33	PFC Zero Cross	34	Zero Cross A

Table 2-7. UNI-3 Connector Description (Continued)

P1			
Pin #	**Signal**	**Pin #**	**Signal**
35	Zero Cross B	36	Zero Cross C
37	Shield	38	Back-EMF Phase A Sense
39	Back-EMF Phase B Sense	40	Back-EMF Phase C Sense

2.12 Run/Stop Switch

A Run/Stop toggle switch is connected to GPIO signal AN7, as shown in Figure 2-9. An optional series resistor is provided which, when removed, allows the user to utilize the AN7 signal for other purposes.

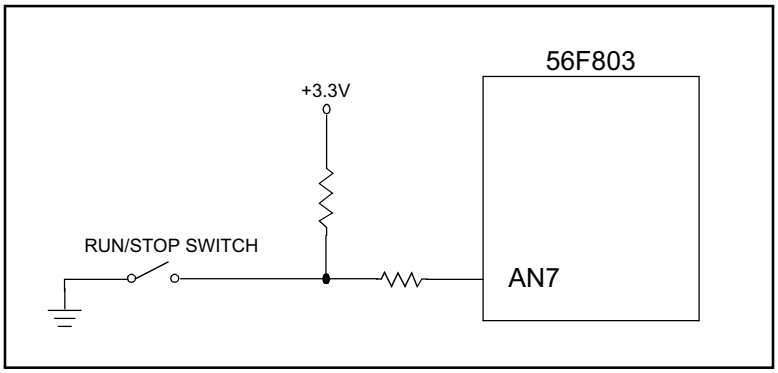

Figure 2-9. Run/Stop Switch

2.13 Motor Control PWM Signals and LEDs

The 56F803 has a dedicated PWM unit. The unit contains six PWM, three Phase Current sense and four Fault input lines. The PWM lines are connected to the UNI-3 interface connector and to a set of six PWM LEDs via inverting buffers. The buffers are used to isolate and drive the controller's PWM outputs to the PWM LEDs. The PWM LEDs indicate the status of PWM group signals, refer to Figure 2-12. The PWM group signals are routed out to headers and are available for use by the end user.

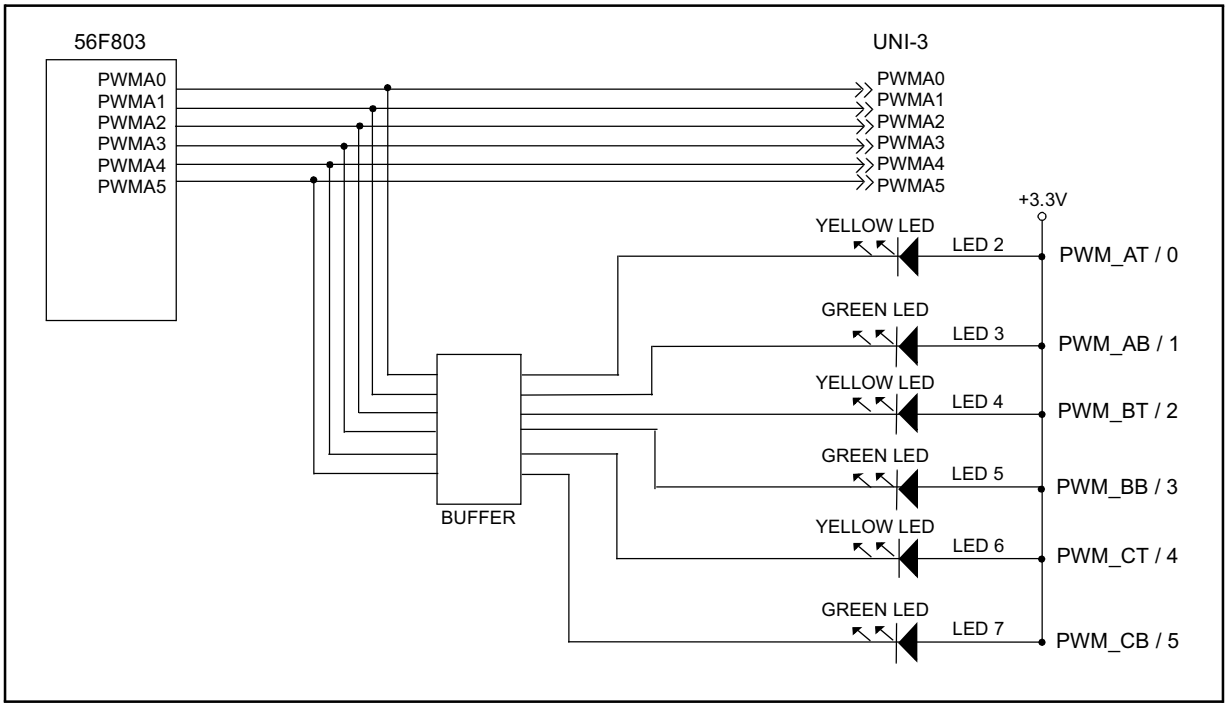

Figure 2-10. PWM Group Interface and LEDs

2.14 Motor Protection Logic

The 56F803EVM contains a UNI-3 connector that interfaces with various motor drive boards. The controller can sense error conditions generated by the motor power stage boards via signals on the UNI-3 connector. The motor driver board's Motor Supply DC Bus Voltage, Current and Motor Phase Currents are sensed on the power stage board. The conditioned signals are transferred to the device board via the UNI-3 connector. These analog input signals are compared to limits set by trimpots. If the input analog signals are greater than the limit set by the trimpot, a digital-compatible, +3.3V DC, fault signal is generated.

2.14.1 UNI-3 Motor Protection Logic

The UNI-3 DC Bus Over-Voltage signal is connected to the controller's PWM group's fault input, FAULT0. The UNI-3 DC Bus Over-Current signal is connected to the device's PWM group's fault input, FAULT1. Additionally, the UNI-3 DC Bus Over-Voltage and Over-Current analog signals are connected to two A/D inputs, AN0 and AN1, respectively. Figure 2-11 contains the diagram of the DC Bus Over-Voltage and DC Bus Over-Current circuit for the UNI-3 interface.

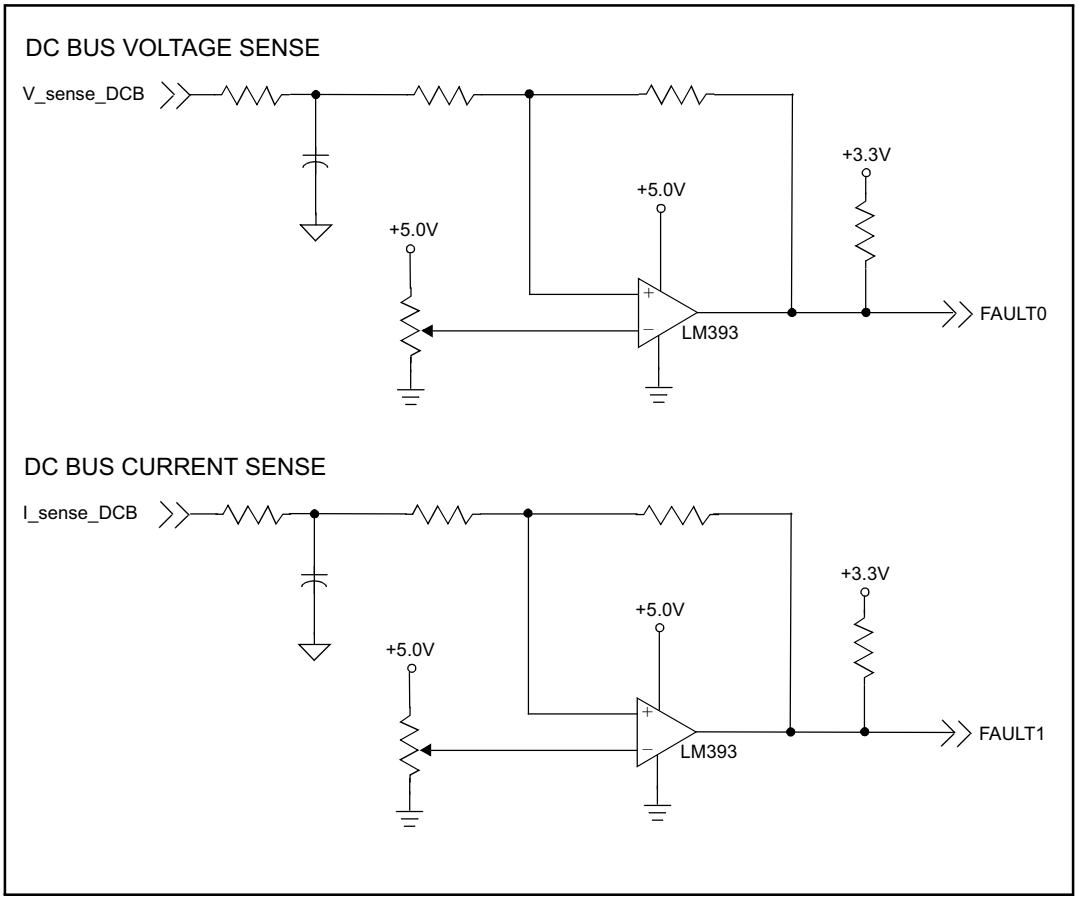

Figure 2-11. DC Bus Over-Voltage and Over-Current Detection Schematic Diagram

2.15 Back-EMF and Motor Phase Current Sensing

The UNI-3 connector supplies Back-EMF and Motor Phase Current signals from the three phases of a motor attached to a motor drive unit. The Back-EMF signals on the UNI-3 connectors are derived from a resistor divider network contained in the motor drive unit. These resistors divide down the attached motor's Back-EMF voltages to a 0 to +3.3V level. In certain instances, the Back-EMF signals can exceed this maximum range. The Motor Phase Current signals are derived from current sense resistors. Both of these signal groups are then routed to a group of header pins that allow the end user to select which signal group the device's A/D will monitor. Refer to Figure 2-12 for the design of a single channel.

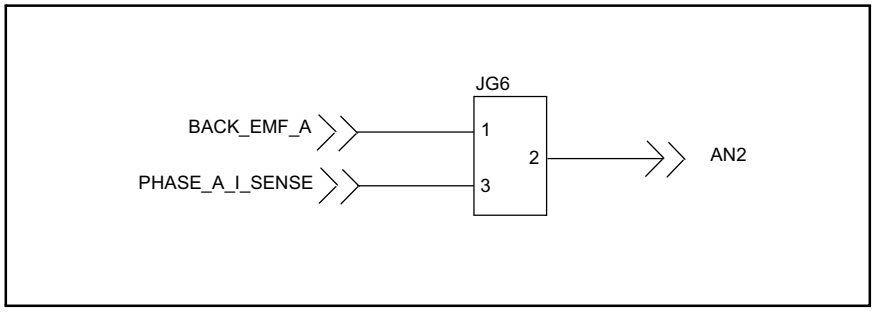

Figure 2-12. Primary Back-EMF or Motor Phase Current Sense Signals

2.16 Quadrature Encoder/Hall-Effect Interface

The 56F803EVM board contains a Quadrature Encoder/Hall-Effect interface connected to the device's Quad Encoder input port. The circuit is designed to accept +3.0V to +5.0V encoder or Hall-Effect sensor inputs. Input noise filtering is supplied on the input path for the Quadrature Encoder/Hall-Effect interface, along with additional noise rejection circuitry inside the controller. Figure 2-13 shows the encoder interface.

2.17 Zero-Crossing Detection

An attached UNI-3 motor drive board contains logic that can send out pulses when the phase voltage of an attached 3-phase motor drops to zero. The motor drive board circuits generate a 0 to +3.3V DC pulse via voltage comparators. The resulting pulse signals are sent to a set of jumper blocks shared with the Encoder/Hall-Effect interface. The jumper blocks allow the selection of Zero-Crossing signals or Quadrature Encoder/Hall-Effect signals. When in operation, the controller will only monitor one set of signals, either the Encoder/Hall-Effect or the Zero-Crossing. Figure 2-13 shows the Zero-Crossing and Encoder/Hall circuits.

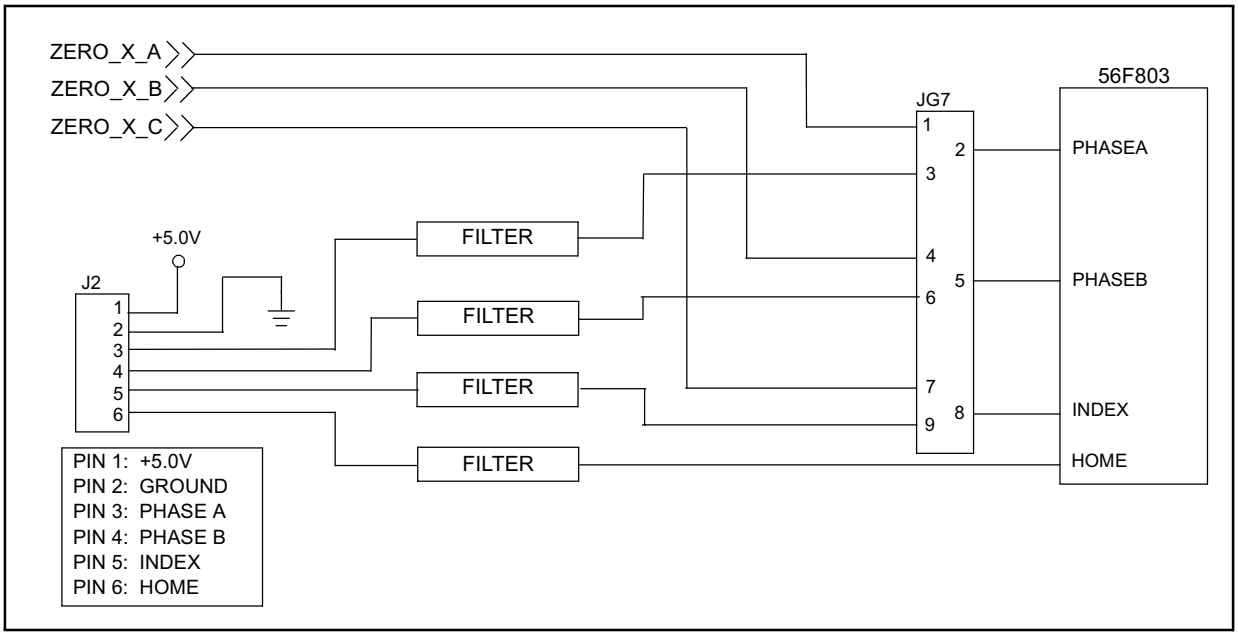

Figure 2-13. Zero-Crossing Encoder Interface

2.18 CAN Interface

The 56F803EVM board contains a CAN physical-layer interface chip that is attached to the MSCAN_RX and MSCAN_TX pins on the 56F803. The EVM board uses a Philips, PCA82C250, high speed, 1Mbps, physical layer interface chip. Due to the +5.0V operating voltage of the CAN chip, a pull-up to +5.0V is required to level shift the Transmit Data output line from the 56F803. A primary, J3, and a daisy-chain, J13, CAN connector are provided to allow easy daisy-chaining of CAN devices. Refer to Figure 2-14 for a connection diagram and to Table 2-8 for the CAN signals.

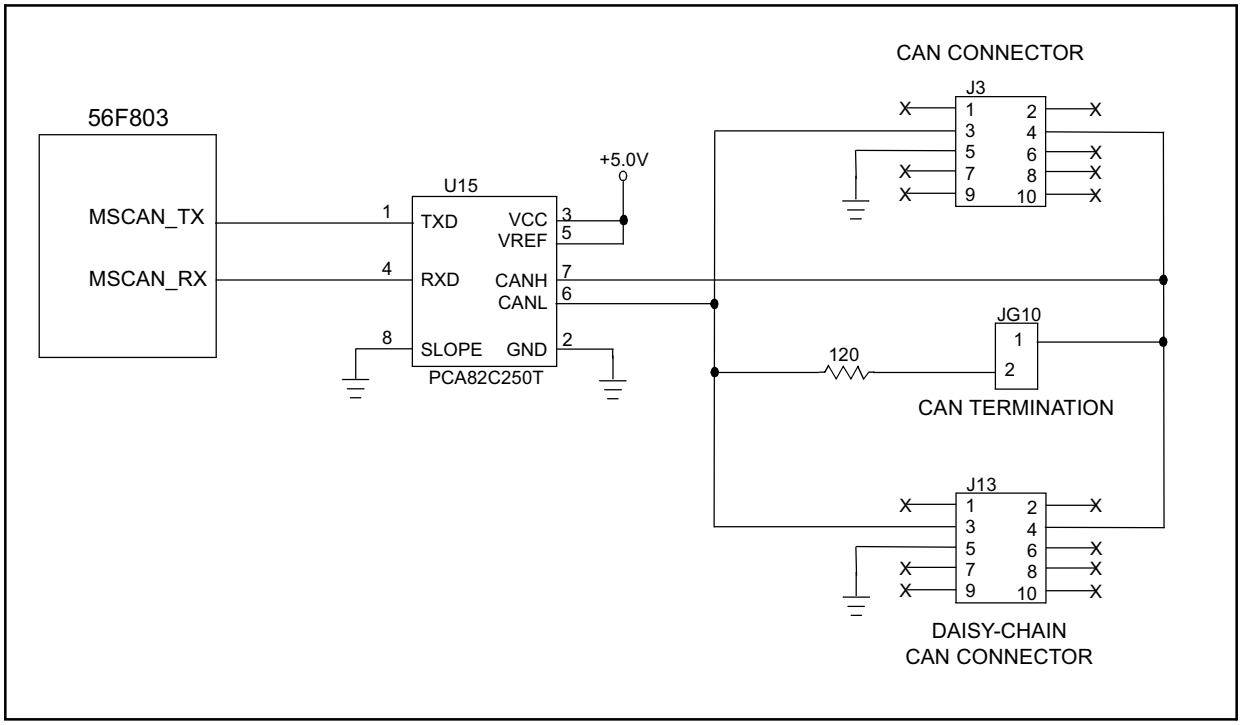

Figure 2-14. CAN Interface

Table 2-8. CAN Header Description

J3 and J13			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	2	NC
3	CANL	4	CANH
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC

2.19 Peripheral Connectors

The EVM board contains a group of Peripheral Expansion Connectors used to gain access to the resources of the 56F803. The following signal groups have Expansion Connectors:

- External Memory Control
- Encoder/Timer Channel
- Timer Channel
- Address Bus
- Data Bus
- A/D Input Port
- Serial Communications Port
- Serial Peripheral Interface Port
- CAN Port
- PWM Port

2.19.1 External Memory Control Signal Expansion Connector

The External Memory Control Signal connector contains the device's external memory control signal lines. See Table 2-9 for the names of these signals.

Table 2-9. External Memory Control Signal Connector Description

J8			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{\text{RD}}$	2	$\overline{\text{IRQA}}$
3	$\overline{\text{WR}}$	4	$\overline{\text{IRQB}}$
5	$\overline{\text{PS}}$	6	$\overline{\text{RESET}}$
7	$\overline{\text{DS}}$	8	NC
9	CLKO	10	$\overline{\text{DE}}$
11	GND	12	+3.3V

2.19.2 Encoder/Timer Channel Expansion Connector

The Encoder/Timer Channel port is an MPIO port attached to the Timer expansion connector. The port can act as a Quadrature Decoder interface port or as a general purpose Timer port. Refer to Table 2-10 for the signals attached to the connector.

Table 2-10. Timer Connector Description

J2	
Pin #	**Signal**
1	+5.0V
2	GND
3	PhaseA
4	PhaseB
5	INDEX
6	HOME

2.19.3 Timer Channel Expansion Connector

The Timer Channel port is a GPIO timer port attached to the Timer D expansion connector. See Table 2-11 for the signals attached to the connector.

Table 2-11. Timer D Connector Description

J10	
Pin #	**Signal**
1	TD1
2	TD2
3	GND
4	+3.3V

2.19.4 Address Bus Expansion Connector

The 16-bit Address bus connector contains the controller's external memory address signal lines. The upper 8 bits, A8 - A15, can also be used as Port A GPIO lines. See Table 2-12 for the Address bus connector information.

Table 2-12. External Memory Address Bus Connector Description

J7			
Pin #	**Signal**	**Pin #**	**Signal**
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	+3.3V

2.19.5 Data Bus Expansion Connector

The 16-bit Data bus connector contains the controller's external memory data signal lines. Refer to Table 2-13 for the Data bus connector information.

Table 2-13. External Memory Address Bus Connector Description

J11			
Pin #	**Signal**	**Pin #**	**Signal**
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	D8	10	D9
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	GND	18	+3.3V

2.19.6 A/D Port Expansion Connector

The 8-channel Analog-to-Digital conversion port is attached to this connector. See Table 2-14 for connection information.

Table 2-14. A/D Connector Description

J9	
Pin #	**Signal**
1	AN0
2	AN1
3	AN2
4	AN3
5	AN4
6	AN5
7	AN6
8	AN7
9	GNDA
10	+3.3VA

2.19.7 Serial Communications Port Expansion Connector

The Serial Communications Port, SCI, is attached to this connector. Refer to Table 2-15 for connection information.

Table 2-15. SCI Connector Description

J12	
Pin #	**Signal**
1	TXD
2	RXD
3	GND

2.19.8 Serial Peripheral Interface Expansion Connector

The Serial Peripheral Interface, SPI, is attached to this connector. See Table 2-16 for connection information.

Table 2-16. SPI Connector Description

J6			
Pin #	**Signal**	**Pin #**	**Signal**
1	SCLK	2	MOSI
3	MISO	4	$\overline{SS}$
5	GND	6	+3.3V

2.19.9 CAN Expansion Connector

The CAN port is attached to this connector. Refer to Table 2-17 for connection information.

Table 2-17. CAN Connector Description

J5	
Pin #	**Signal**
1	MSCAN_TX
2	MSCAN_RX
3	GND

2.19.10 PWM Port Expansion Connector

The PWM port is attached to this connector. Refer to Table 2-18 for connection information.

Table 2-18. PWM Port Connector Description

J4			
Pin #	**Signal**	**Pin #**	**Signal**
1	ISA0	2	ISA1
3	ISA2	4	FAULT0
5	FAULT1	6	FAULT2
7	PWM0	8	PWM1
9	PWM2	10	PWM3
11	PWM4	12	PWM5
13	GND	14	+3.3V

2.20 Test Points

The 56F803EVM board has nine test points: Five near the breadboard, (+3.3V, GND, +3.3VA, AGND and +5.0V), and four near the UNI-3 connector, (-15VA, GND, +15VA and GND).

Appendix A
56F803EVM Schematics

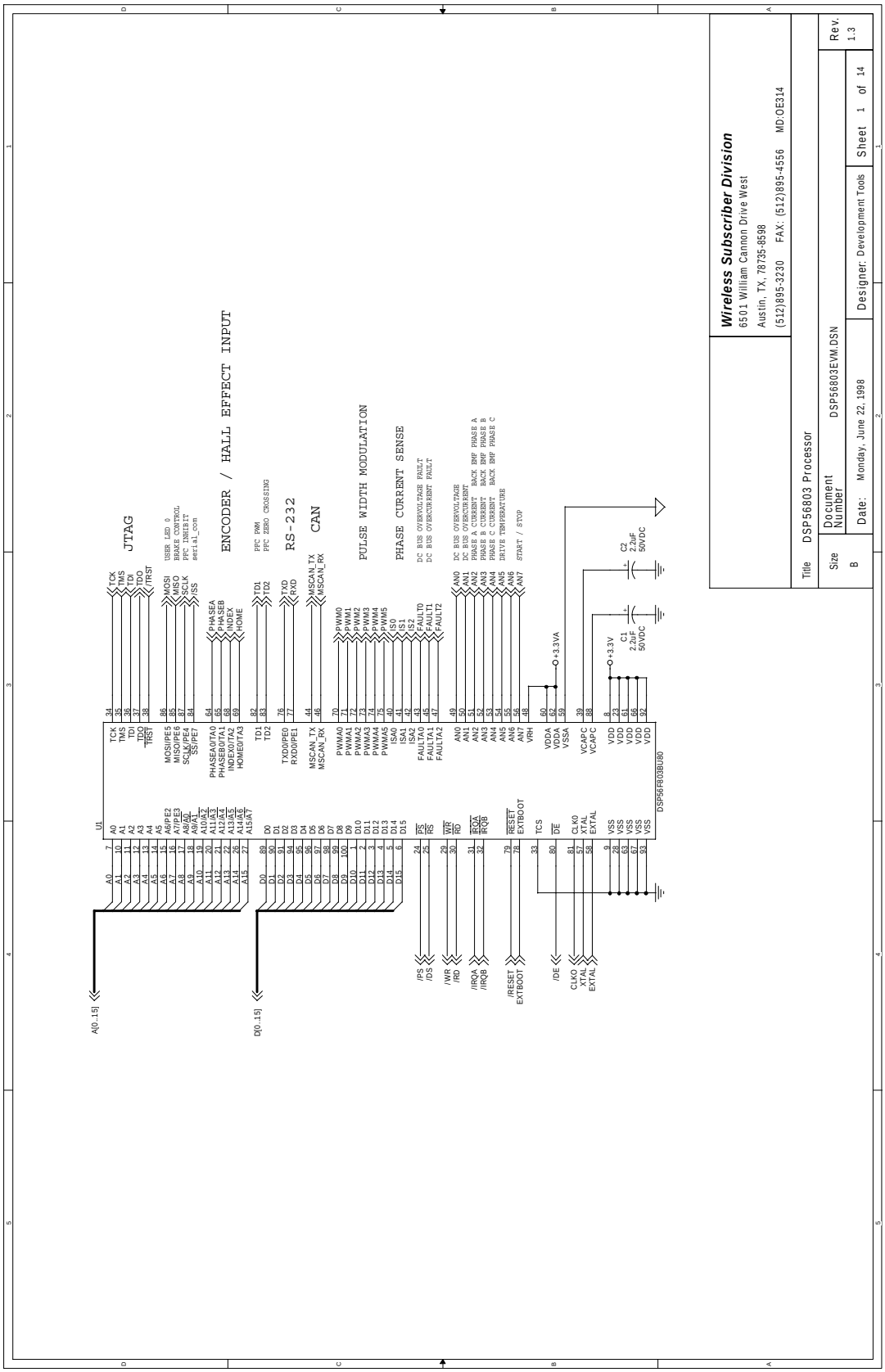

Figure A-1. 56F803 Processor

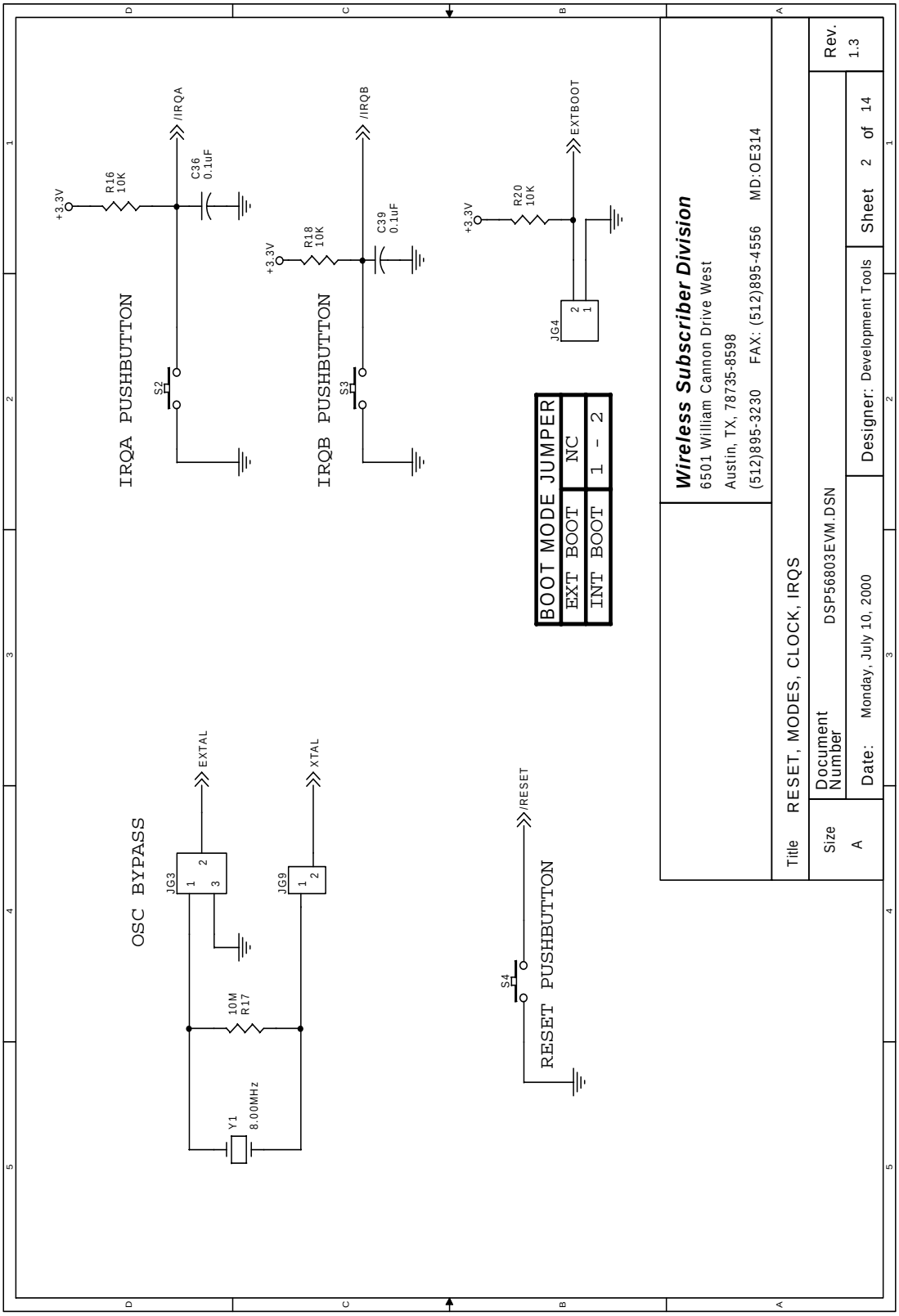

Figure A-2. Reset, Mode, Clock & IRQsL

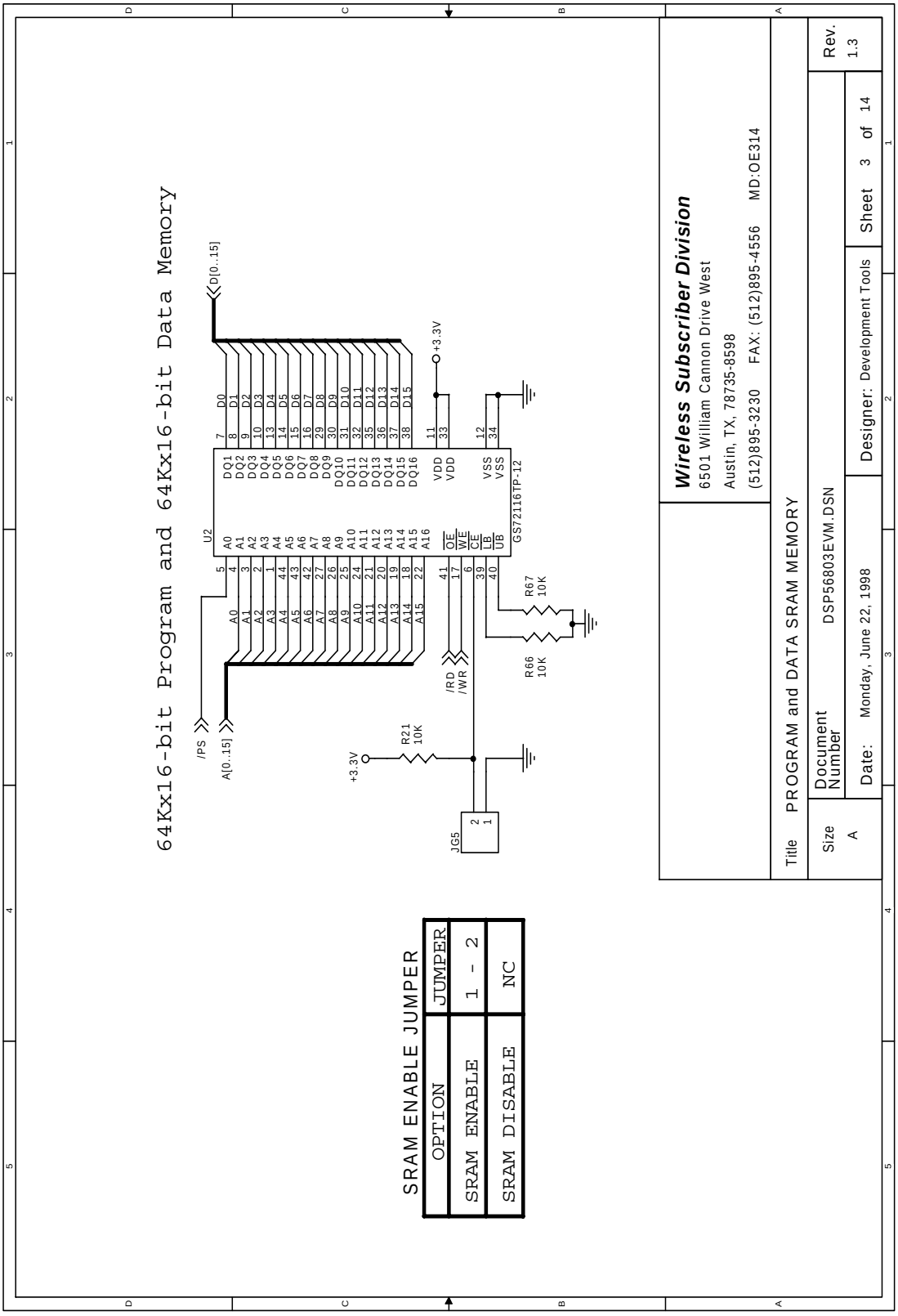

Figure A-3. Program & Data SRAM Memory

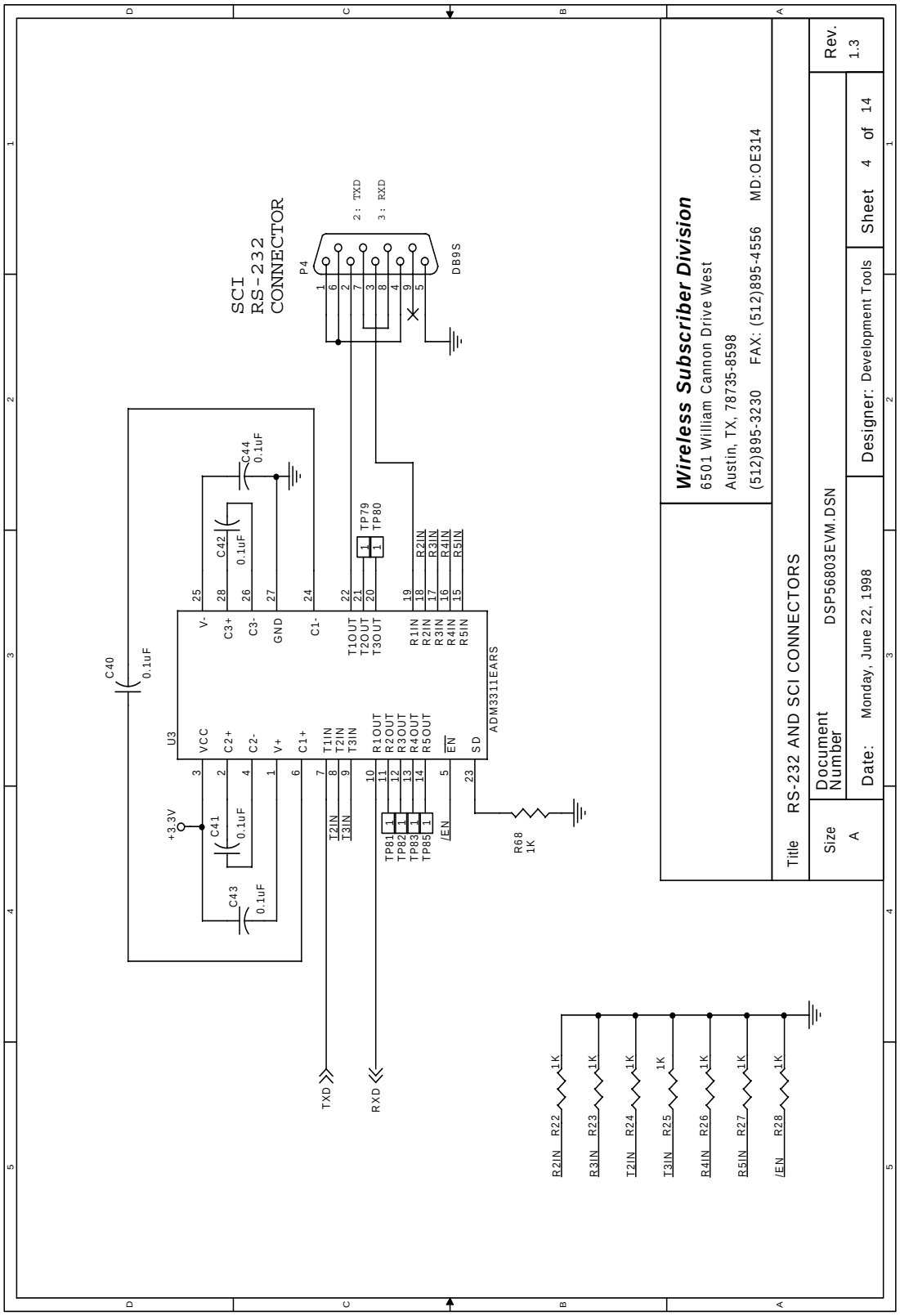

Figure A-4. RS-232 and SCI Connectors

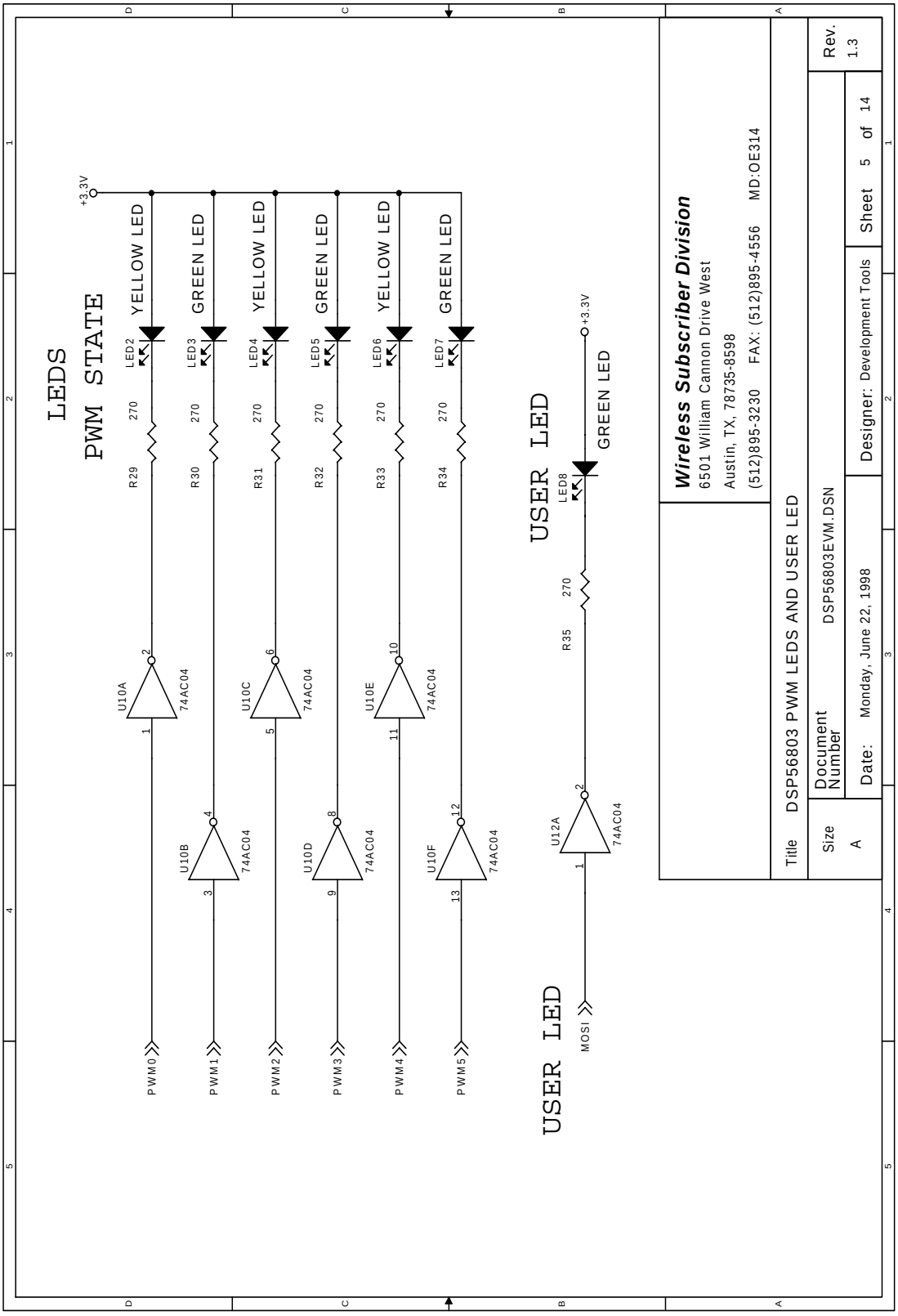

Figure A-5. 56F803 PWM LEDs and User LED

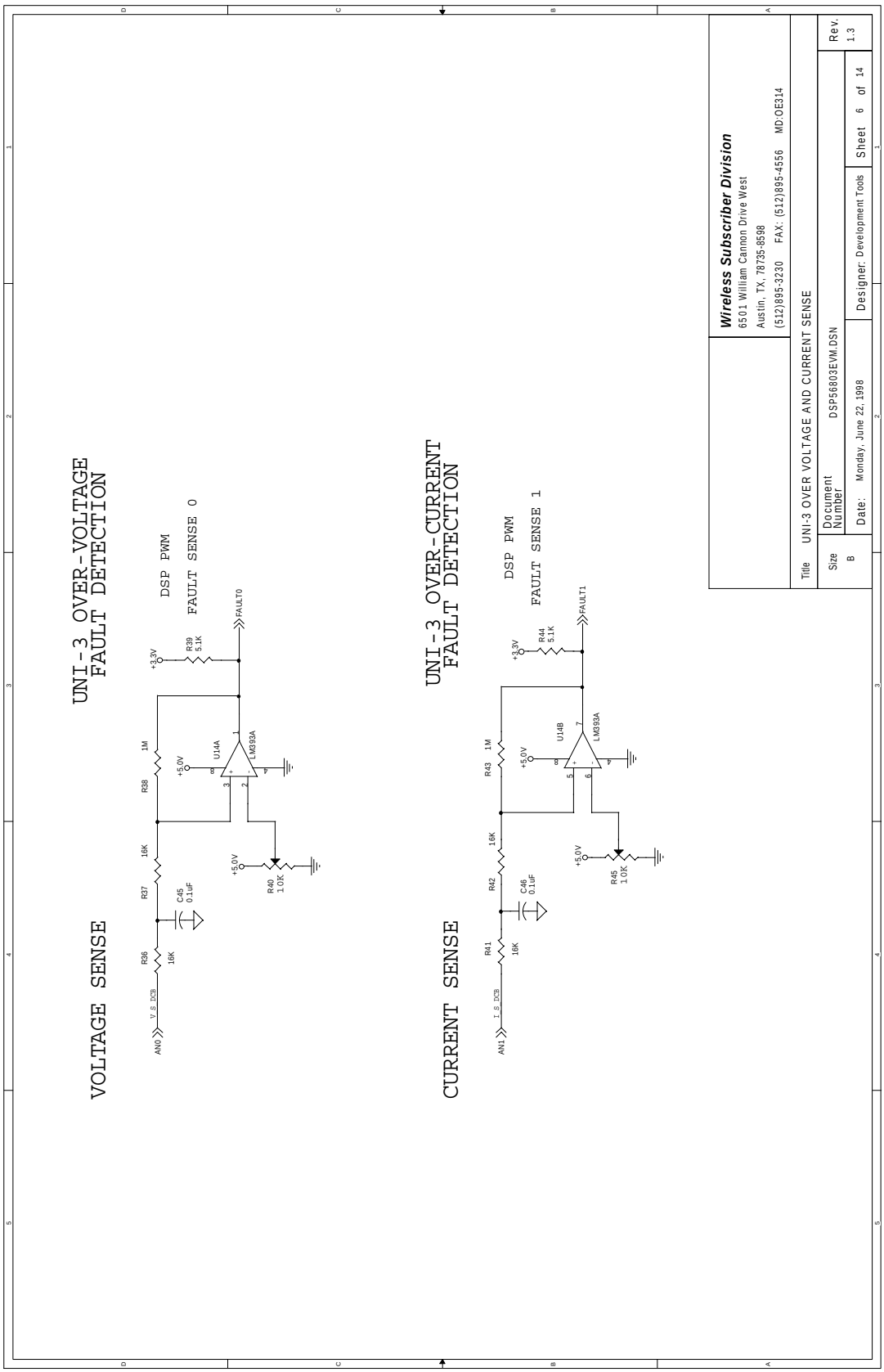

Figure A-6. UNI-3 Over-Voltage and Current Sense

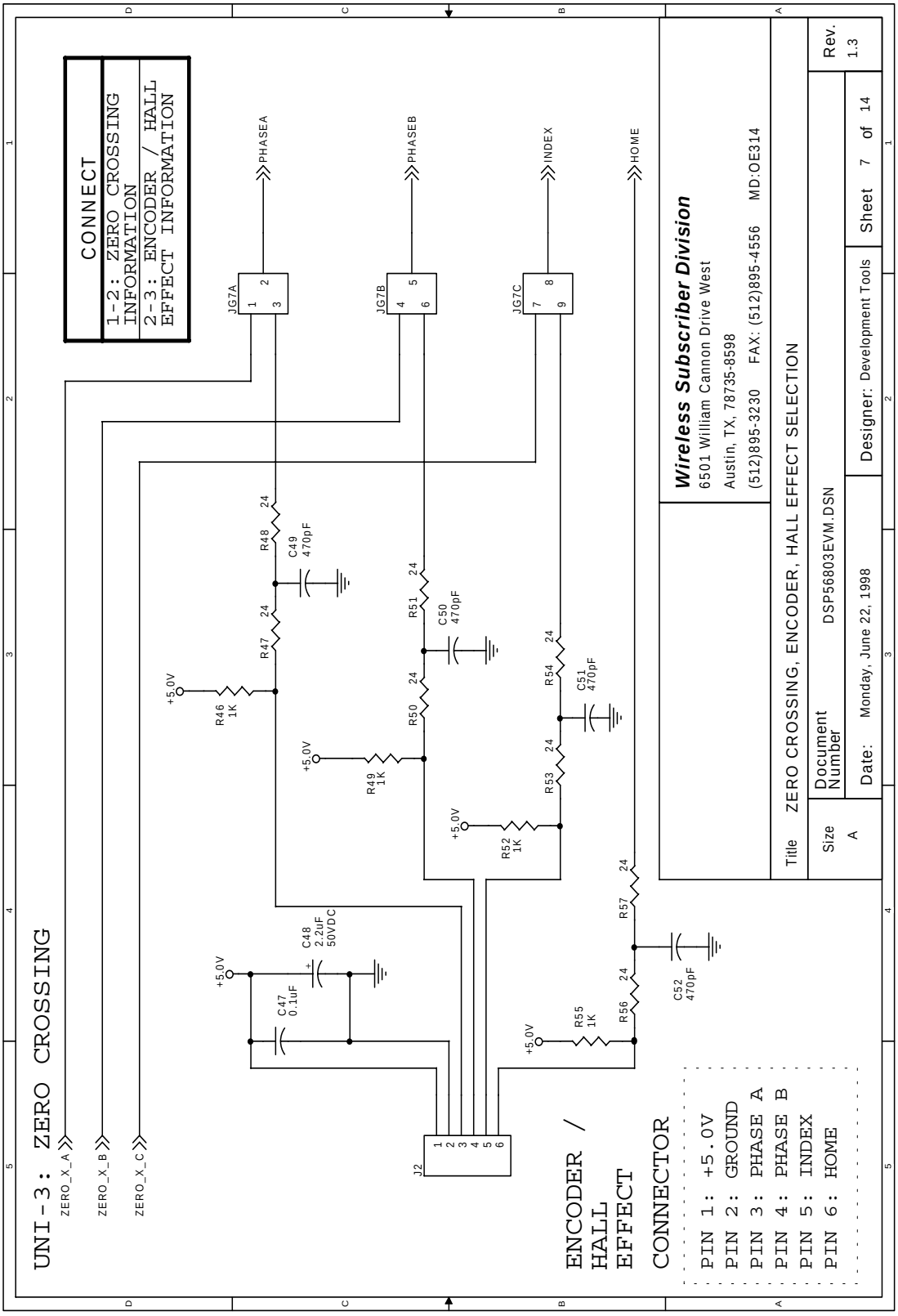

Figure A-7. Zero-Crossing/ Encoder or Hall-Effect Selection

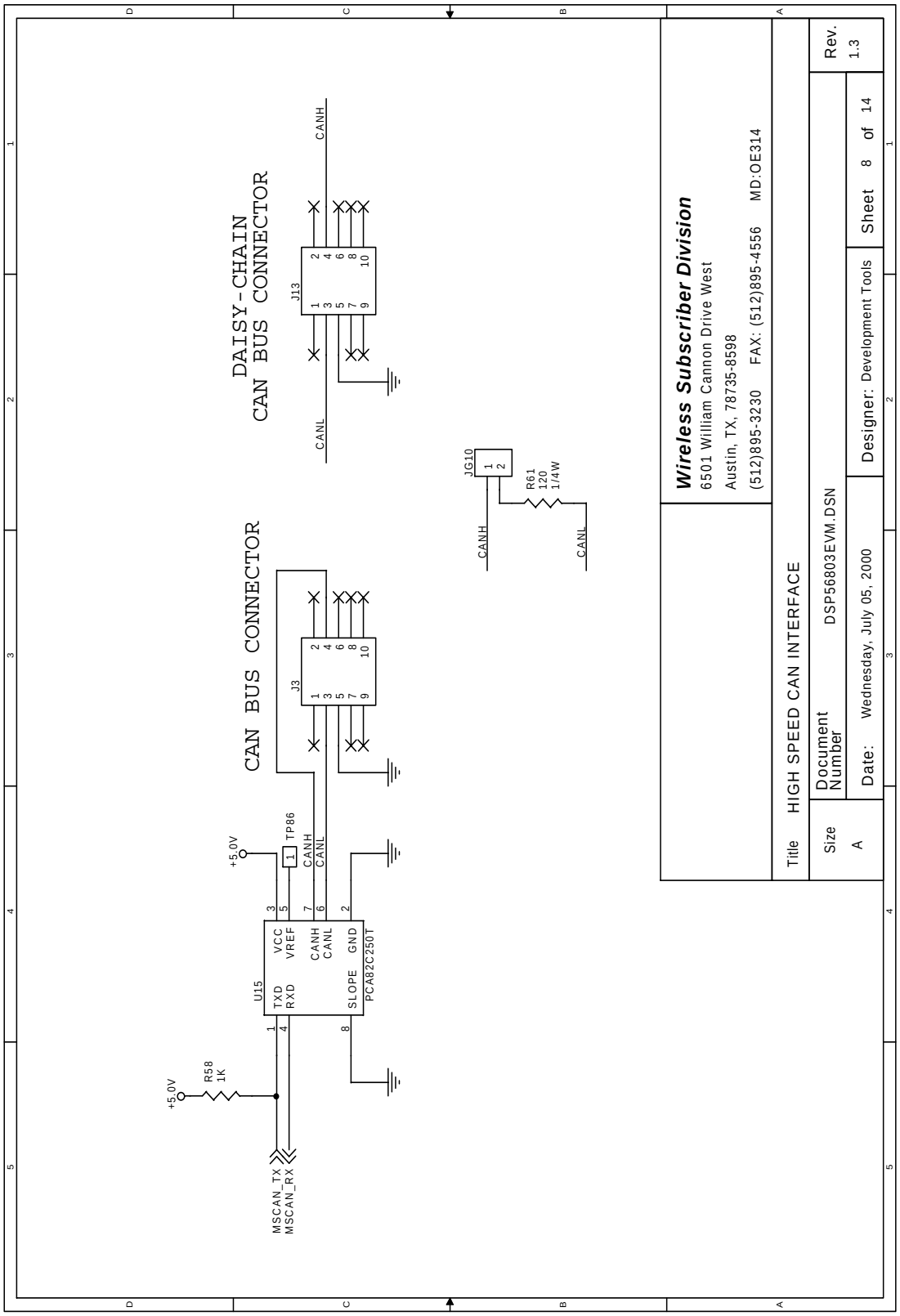

Figure A-8. High Speed CAN Interface

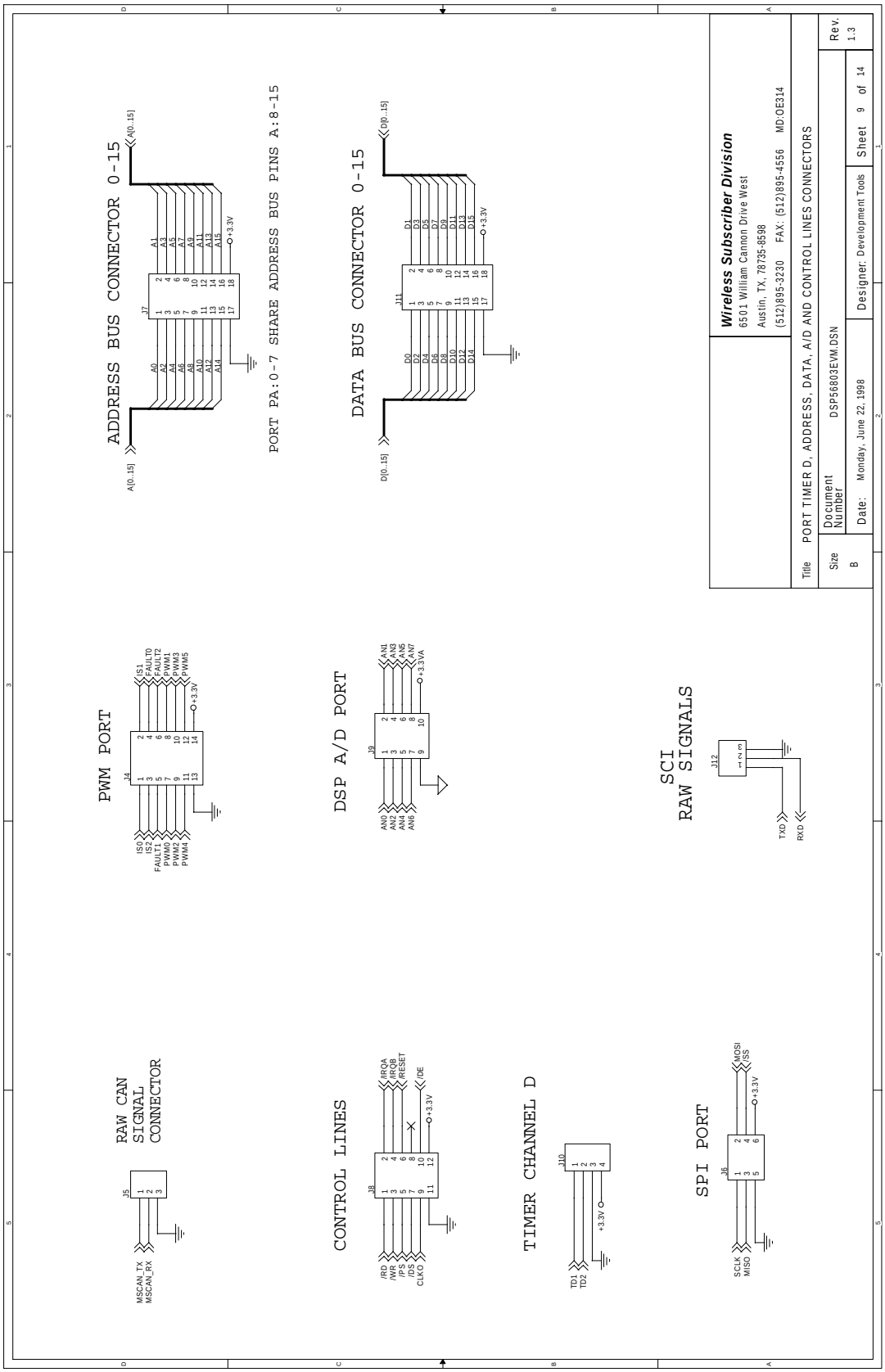

Figure A-9. Port Timer D, Address, Data, A/D and Control Line Connectors

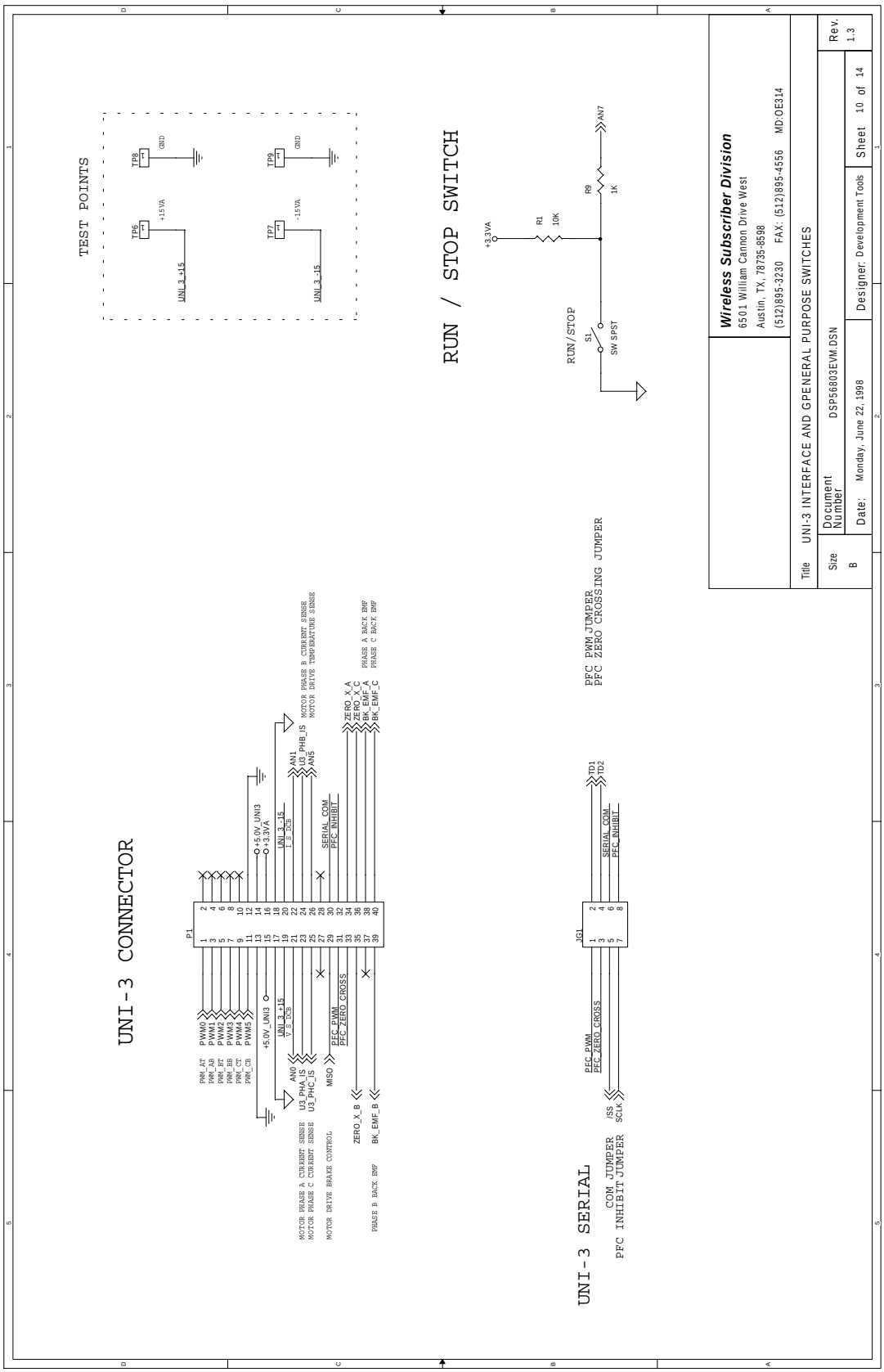

Figure A-10. UNI-3 Interface and General Purpose Switches

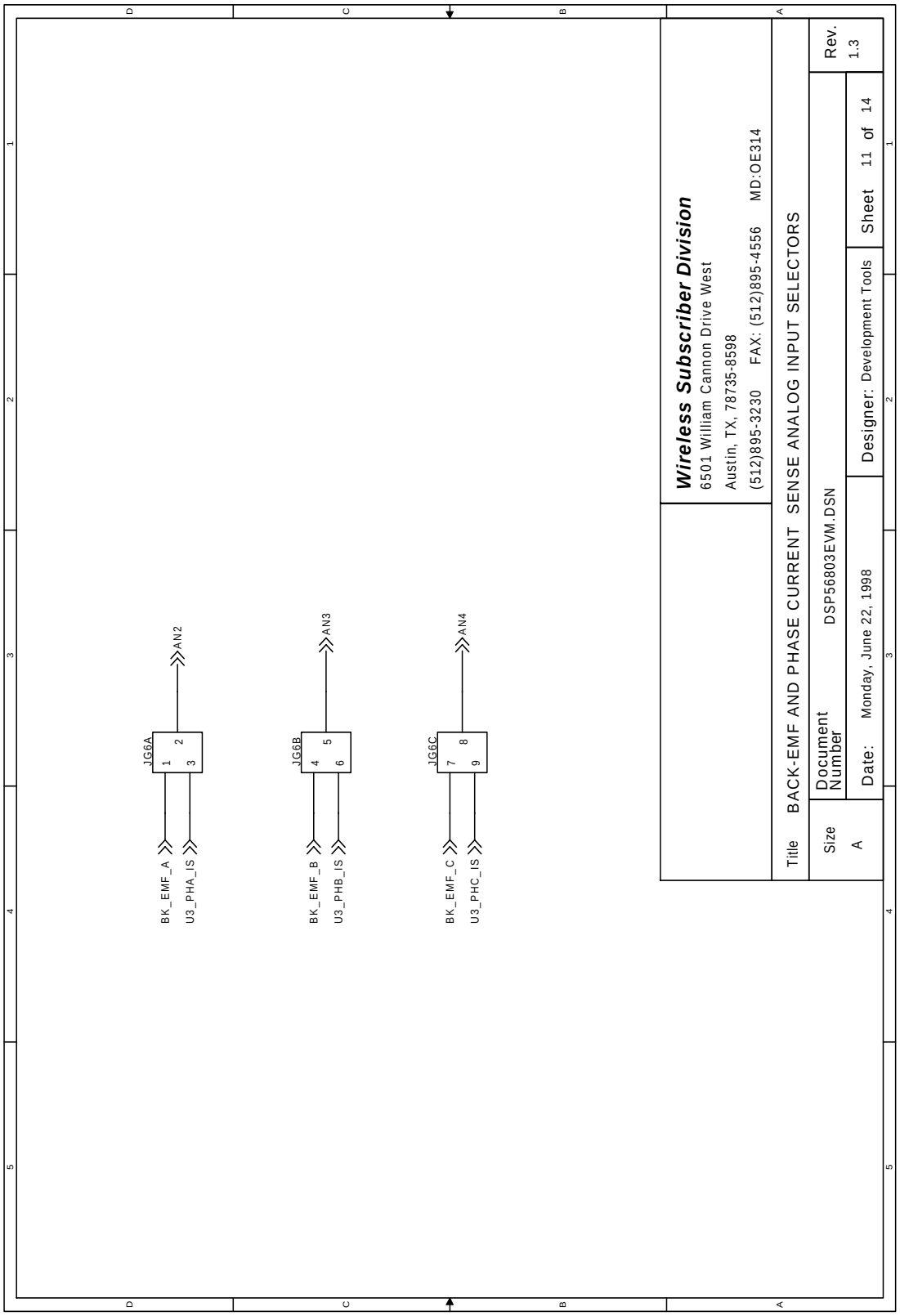

Figure A-11. Back-EMF and Phase Current Sense Analog Input Selectors

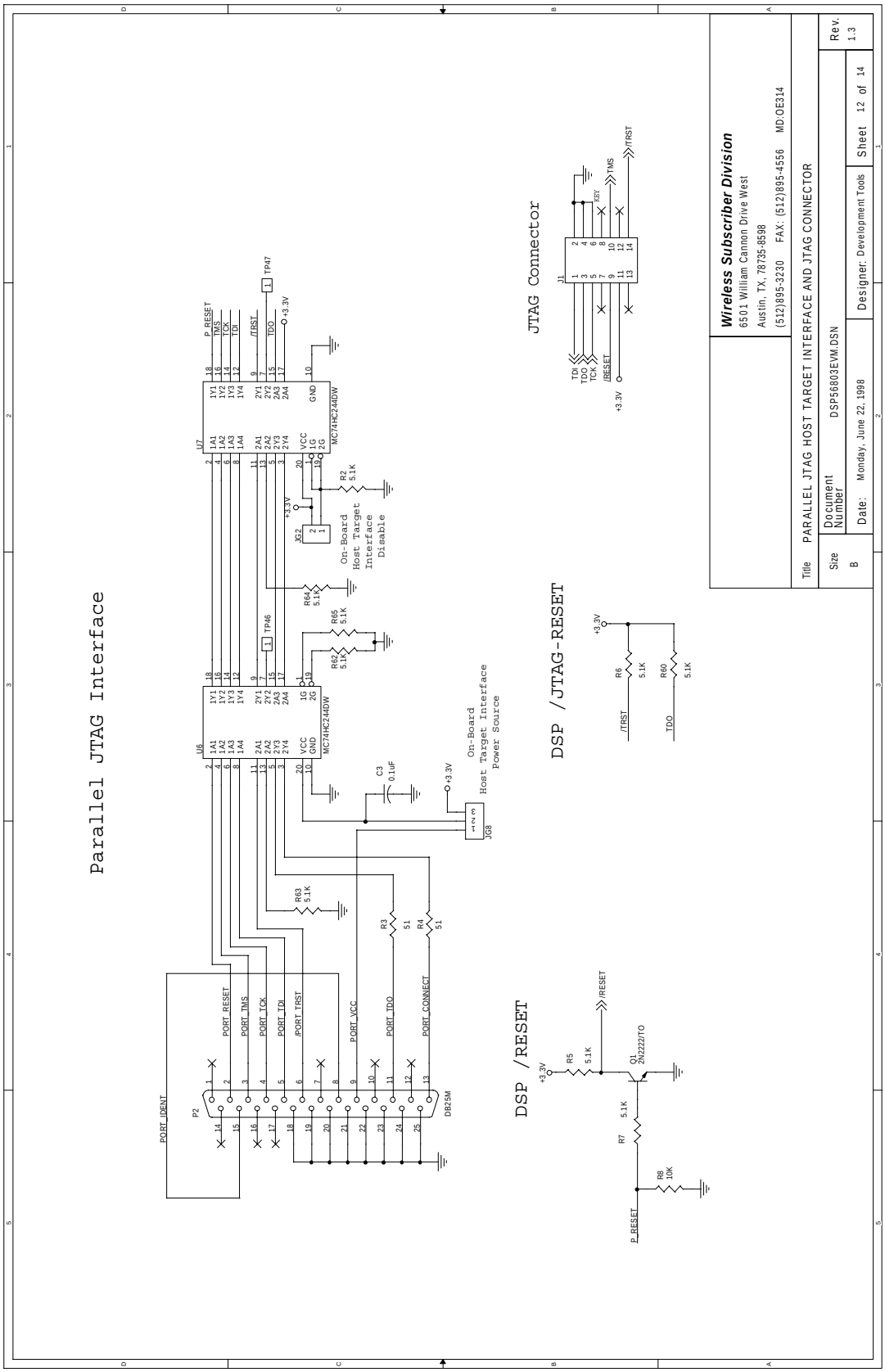

Figure A-12. Parallel JTAG Host/Target Interface and JTAG Connector

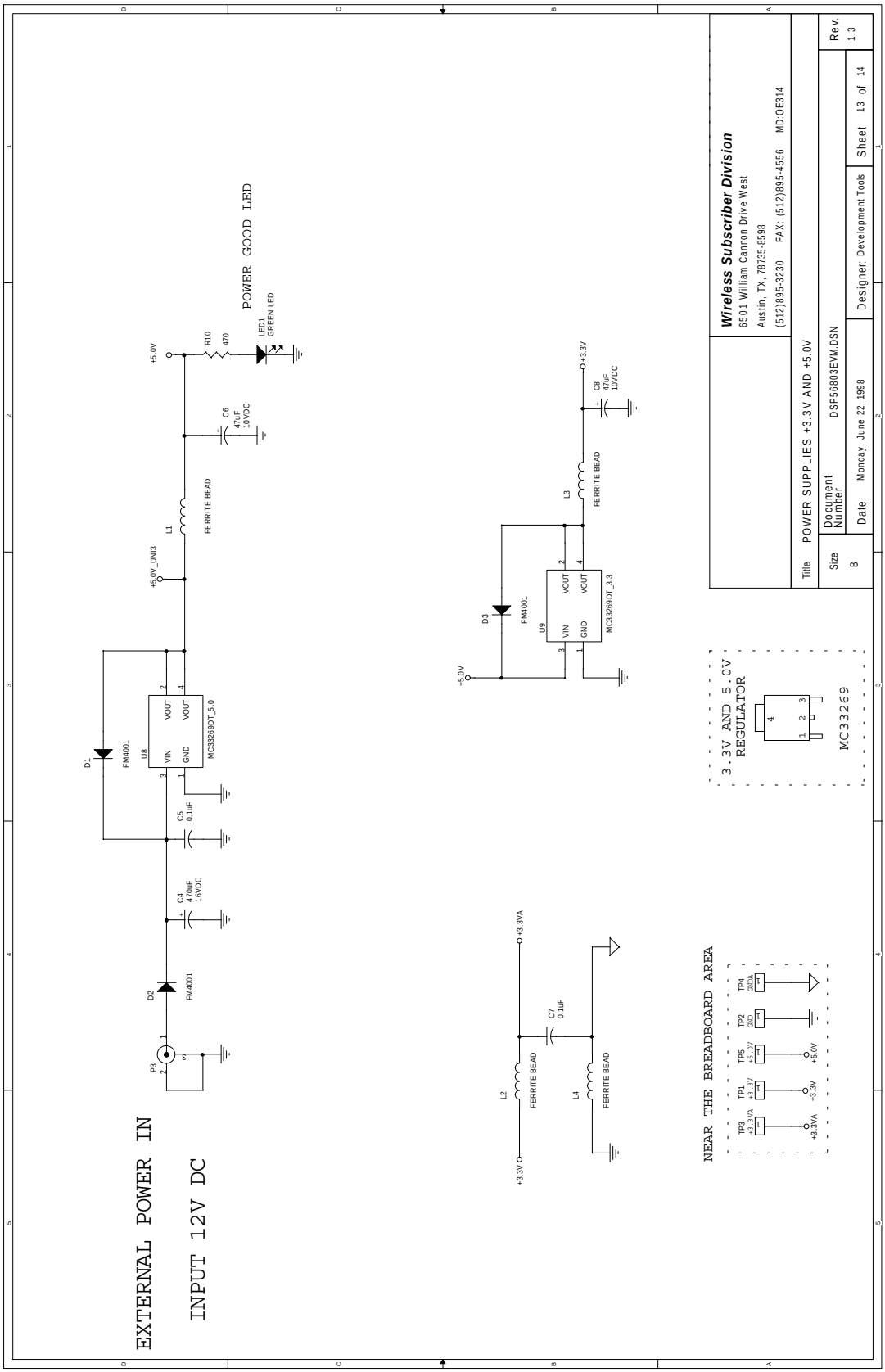

Figure A-13. Power Supplies 3.3V and 5.0V

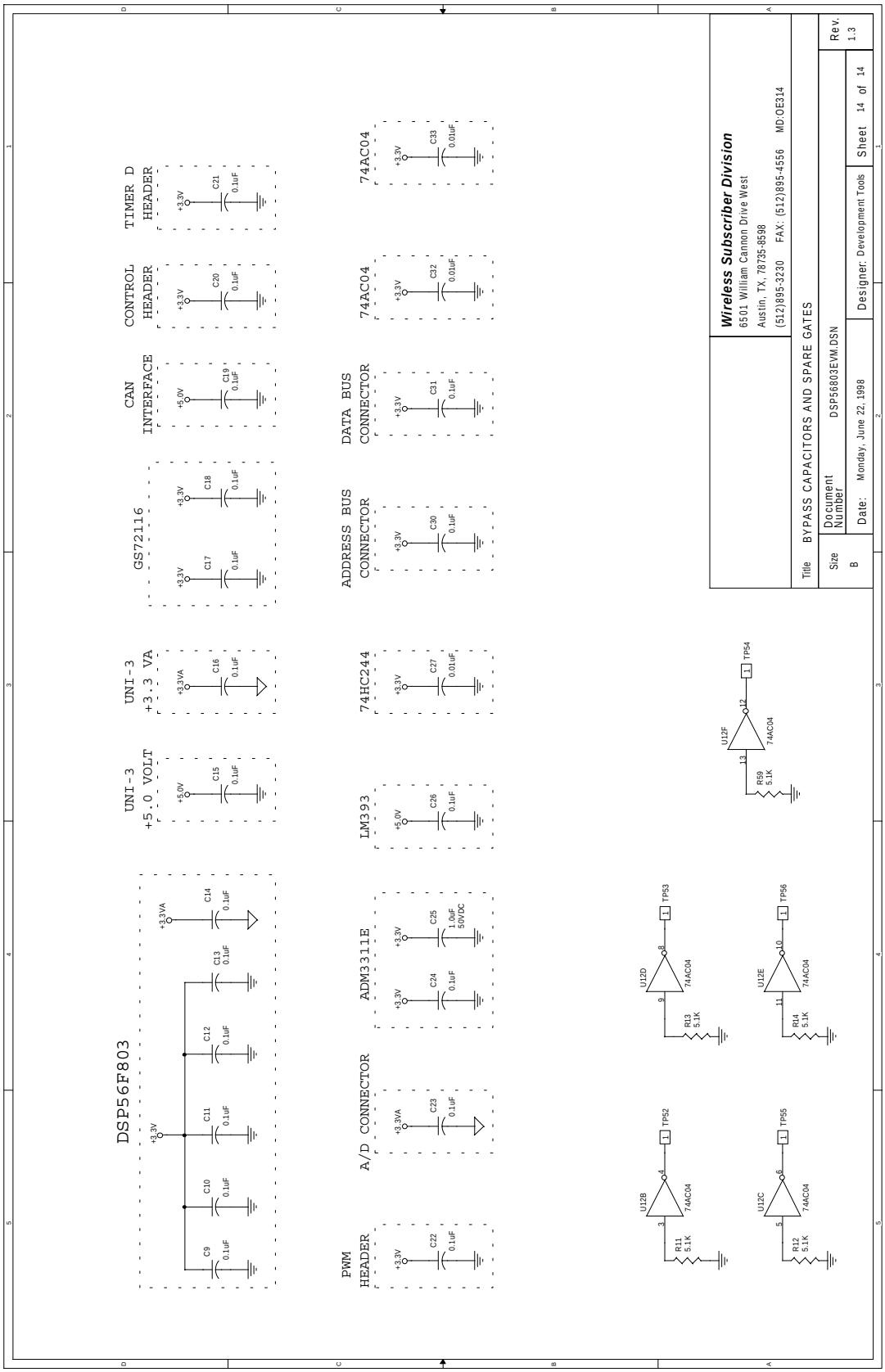

Figure A-14. Bypass Capacitors and Spare Gates

Appendix B
56F803EVM Bill of Material

Qty	Description	Ref. Designators	Vendor Part #s
Integrated Circuits			
1	DSP56F803BU80	U1	Freescale, DSP56F803BU80
1	GS72116TP-12	U2	GSI, GS72116TP-12
1	ADM3311EARS	U3	Analog Devices, ADM3311EARS
2	MC74HC244DW	U6, U7	ON Semiconductor, MC74HC244DW
1	MC33269DT-5.0	U8	ON Semiconductor, MC33269DT-5.0
1	MC33269DT-3.3	U9	ON Semiconductor, MC33269DT-3.3
2	74AC04SC	U10, U12	Fairchild, 74AC04SC
1	LM393	U14	National Semiconductor, LM393
1	PCA82C250T	U15	Philips Semiconductor, PCA82C250T
Resistors			
4	16K Ω	R36, R37, R41, R42	SMEC RC73L2A16KOHMJT
2	1M Ω	R43, R38	SMEC RC73L2A1MOHMJT
16	5.1K Ω	R2, R5 - R7, R11 - R14, R39, R44, R59, R60, R62 - R65	SMEC RC73L2A5.1KOHMJT
8	10K Ω	R1, R8, R16, R18, R20, R21, R66, R67	SMEC RC73L2A10KOHMJT
2	51 Ω	R3, R4	SMEC RC73L2A51OHMJT
1	470 Ω	R10	SMEC RC73L2A470OHMJT
1	10M Ω	R17	SMEC RC73L2A10MOHMJT
14	1K Ω	R9, R22 - R28, R46, R49, R52, R55, R58, R68	SMEC RC73L2A1KOHMJT

Qty	Description	Ref. Designators	Vendor Part #s
Resistors (Continued)			
7	270 Ω	R29 - R35	SMEC RC73L2A270OHMJT
8	24 Ω	R47, R48, R50, R51, R53, R54, R56, R57	SMEC RC73L2A24OHMJT
1	120 Ω, 1/4W	R61	YAGEO CFR 120QBK
Potentioneters			
2	10K Ω	R40, R45	BC/MEPCOPAL ST4B103CT
Inductors			
4	1.0mH	L1 - L4	Fair-Rite 2743015112
LEDs			
5	Green LED	LED1, LED3, LED5, LED7, LED8	Hewlett-Packard HSMG-C650
3	Yellow LED	LED2, LED4, LED6	Hewlett-Packard HSMY-C650
Diode			
3	FM4001	D1, D2, D3	Vishay DL4001DICT
Capacitors			
3	2.2μF, 50V DC	C1, C2, C48	TTI UWX1H2R2MCR2GB
32	0.1μF	C3, C5, C7, C9 - C24, C26, C30, C31, C35, C36, C39 - C47	SMEC MCCE104K2NR-T1
3	0.01μF	C27, C32, C33	SMEC MCCE103K2NR-T1
1	470μF, 16V DC	C4	PANASONIC ECE-V1CA471P
2	47μF, 10V DC	C6, C8	PANASONIC ECE-V1AA470P
1	1.0μF, 50V DC	C25	TTI UWT1H010MCR1GB
4	470pF	C49 - C52	SMEC MCCE471J2NO-T1
Jumpers			
4	3 × 1 Bergstick	JG3, JG8, J5, J12	SAMTEC TSW-103-07-S-S
1	4 × 2 Bergstick	JG1	SAMTEC TSW-104-07-S-D
5	1 × 2 Bergstick	JG2, JG4, JG5, JG9, JG10	SAMTEC TSW-102-07-S-S

Qty	Description	Ref. Designators	Vendor Part #s
Jumpers (Continued)			
2	3 x 3 Bergstick	JG6, JG7	SAMTEC TSW-103-07-S-T
3	5 x 2 Bergstick	J3, J9, J13	SAMTEC TSW-105-07-S-D
1	4 x 1 Bergstick	J10	SAMTEC TSW-104-07-S-S
1	3 x 2 Bergstick	J6	SAMTEC TSW-103-07-S-D
2	9 x 2 Bergstick	J7, J11	SAMTEC TSW-109-07-S-D
2	7 x 2 Bergstick	J1, J4	SAMTEC TSW-107-07-S-D
1	6 x 1 MTA	J2	AMP MTA 640456-6
1	6 x 2 Bergstick	J8	SAMTEC TSW-106-07-S-D
Test Points			
9	1 × 1 Bergstick	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Samtec TSW-101-07-S-S
Crystals			
1	8.00MHz Crystal	Y1	ECS-80-18-5P
Connectors			
1	20 x 2 Shrouded	P1	3M 2540-6002UB
1	DB25M Connector	P2	AMPHENOL 617-C025P-AJ121
1	2.1mm coax Power Connector	P3	Switch Craft RAPC-722
1	DE9F Connector	P4	AMPHENOL 617-C009S-AJ120
Switches			
1	SPDT Toggle	S1	C&K GT11MSCKE
3	SPST Pushbutton	S2, S3, S4	Panasonic EVQ-QS205K
Transistors			
1	2N2222A	Q1	ZETEX FMMT2222ACT
Miscellaneous			
11	Shunt	SH1–SH11	Samtec SNT-100-BL-T
6	Rubber Feet	RF1–RF6	3M SJ5018BLKC

INDEX

F

G

H

I

J

L

M

O

P

Q

R

S

T

U

Z

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

DSP56F803EVMUM
Rev. 5
07/2005