Evaluation Boards for ADF7021-V Narrow-Band Transceiver

Preliminary Technical Data

EVAL-ADF7021-VDBxZ

FEATURES

ADF7021-V Transceiver Radio module

Used with EVAL-ADF70XXMBZ2 mother board (development platform with embedded microcontroller)

Combined output matching circuit (no external antenna switch) optimized at different frequency ranges

Software programmable modulation schemes; GFSK/ FSK/ MSK/3FSK/ RC3FSK /4FSK/RC4FSK

PC Software for Register Programming

Loop filter setup for operation up to 4.8kbps.
Higher data-rates possible by altering PLL loop filter.

GENERAL DESCRIPTION

The ADF7021-V is 2FSK/3FSK/4FSK transceivers which are designed for operation in the licensed and unlicensed VHF/UHF bands from 80MHz to 956MHz. There are different versions of the evaluation daughter board available, each optimized for different frequency bands, see Table 1. The daughter-board contains all the required components for operation of the radio, including loop filter, output matching, antenna and connector to mother board.

To control the ADF7021-V via the PC you will need the EVAL-ADF70XXMBZ2 mother board. This technical note describes usage with the EVAL-ADF70XXMBZ2 boards (PCB RevD and higher). This is a multi-function board that can be used for:

- detailed evaluation and RF testing of the parts.
- running the ADIismLINK protocol to evaluate the ADF7xxx performance in a networked environment, perform range testing and Packet Error Rate (PER) tests
- run the low-level device drivers, to perform timing critical tests or simply to patch into existing firmware.

Table 1: Ordering Codes

Board Number	RF Band	Rx Data Rate[2]	Tx Data Rate[1]	Loop Bandwidth
EVAL-ADF70XXMBZ2	Recommended	-	-	-
EVAL-ADF7021-VDB1Z	450 MHz – 470 MHz	Up to 24 kbps	Up to 4.8 kbps	6.0KHz
EVAL-ADF7021-VDB2Z	868 MHz - 870 MHz	Up to 24 kbps	Up to 4.8 kbps	6.0KHz

1. The data rate may be increased by increasing the PLL Loop Bandwidth, see ADI SRD Design Studio for design details.

2. Note this is with 18.5 kHz IF bandwidth

Rev. Pr D

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HARDWARE DESCRIPTION

The RF module, which is plugged into the mother board, consists of the ADF7021-V device, output matching circuit optimized for operation in a certain frequency band, harmonic filter, PLL loop filter, external VCO, de-coupling and TCXO. This RF module provides a low-cost, optimally matched RF reference design which you can use as a starting point for your design. A low-cost BOM is achieved by using a 4-layer PCB, a low-cost TCXO, and a simple combined output matching circuit which eliminates the need for an external antenna switch.

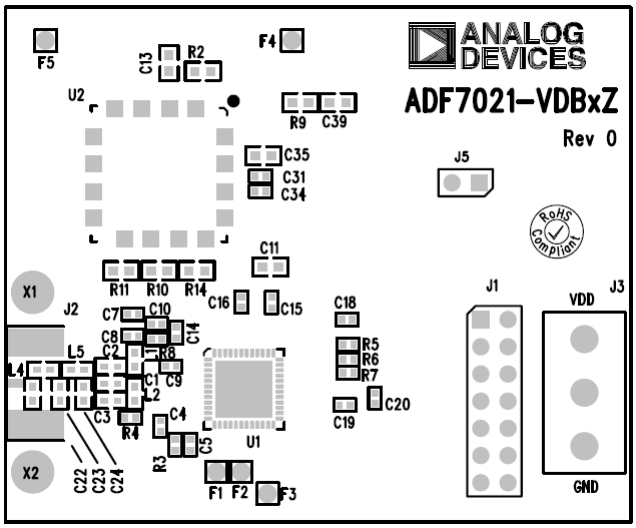


Figure 1: EVAL-ADF7021-VDBxZ – Top Ssilkscreen

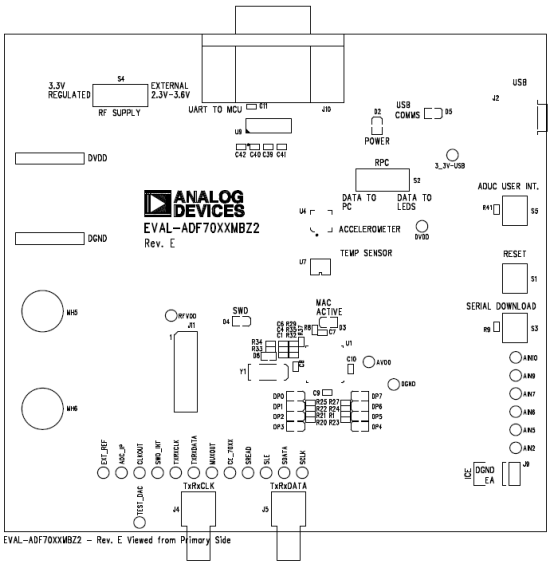


Figure 2. Mother Board Silkscreen – component side view

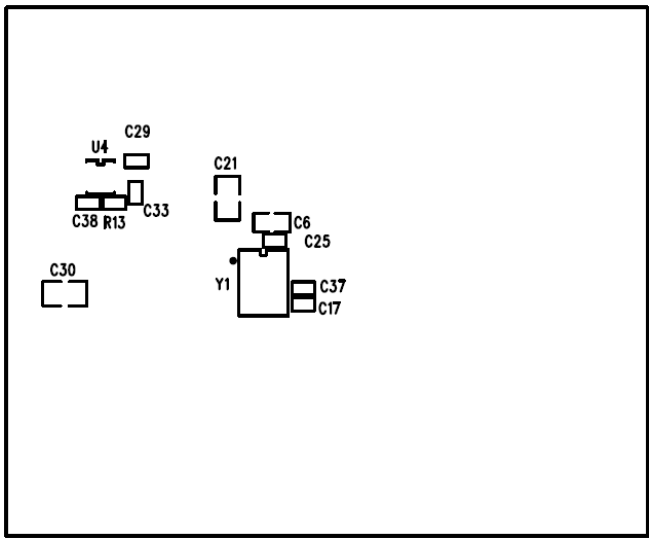


Figure 2.1: EVAL-ADF7021-VDBxZ –Bottom Ssilkscreen

Power Supply Options

The mother board and daughter need to be powered seperately.

The MBZ2 board has several supply options. The simplest method is to simply supply the board with power from the USB cable. The 5V from the USB cable is regulated down to 3.3V for the microcontroller and radio board. It is possible to also supply the board with an external 5V - 9V supply (via J3) or a ½ AA battery. The MBZ2 kit ships with a 3.6V ½ AA battery.

The EVAL-7021-VDBxZ must be powered separately to the motherboard. The ADF7021-V and the VCO are powered together through a precision 3V regulator on boad. This regulator requires a voltage greater than 3.05V and less than 12V. The current drawn by this supply include the currents drawn by the ADF7021-V, TCXO and VCO.

Data Interface (TxRxData, TxRxCLK, INT, CE)

TxRxData and TxRxCLK are both brought out on SMAs. This allows you to either input Txdata view or else view the demodulated data on a oscilloscope or connect into a Bit Error Rate tester. These two pins are connected into the SPI interface on the on-board microcontroller (ADuC847).

CE is a hardware reset pin for the ADF7021-V and can be controlled from the ADI configuration software. These pins are also brought out as test points.

Configuration Interface (SDATA, SCLK, SLE, SREAD)

The configuration interface on the ADF7021-V is connected to GPIO on the ADuC847 microcontroller which bit-bangs the ports to configure the ADF7021-V device. These four configuration pins are also brought out as test points. Low level device drivers are available on the analog.com website as example code of how to interface and configure to the ADF7021-V device.

ADF7XXX CONFIGURATION SOFTWARE DESCRIPTION

Before using the MBZ2 board you should run the "ADF7xxx_ ADIismLINK Install" which contains the relevant USB drivers and setup files for the EVAL-ADF70XXMBZ2. This needs to be done before plugging in the hardware. See Installing USB Drivers section for details.

The ADF7021-V configuration software and the network demo software, ADIismLINK, are also installed as part of the install process. You should check the Analog Devices Website periodically for updates. http://www.analog.com/srd

Once the programs have installed, run ADF7021-V1_0.exe (or later) from the Analog Devices folder in the Start menu. The window shown below should appear – you will need a screen resolution of 1024 x 768 to use the program.

This is the main window and is divided up into several sections some of which have their own sub-windows which are indicated by a raised button. For example in the PLL Options section, you enter the sub-window by clicking on the "Synth Settings…" button. The green and red toggle buttons turn a feature on or off. You can use the software in stand-alone mode, that is with the hardware unconnected to calculate register values for example. In this mode the USB button at the bottom of screen should read 'Connect USB' and should not be clicked. However in most cases you will want to use the software to control the ADF7021-V device. After opening the software, simply click on 'Connect USB'. Once the software has connected to the target board, the button should change to "Disconnect USB". The USB comunications are now initiated and you should be able to communicate with the device using the software. The software also supports the EVAL-ADF70XXMBZ which uses the parallel port interface.

The software eases the programming challenge by allowing you to input your desired RF frequency, modulation scheme, data-rate etc. and then auto-calculating the ADF7021-V register settings based on these inputs. The calculated register settings are displayed in the "Update Registers" panel.

For direct programming of the ADF7021-V, click on the "Manual Register Edit" button. This allows you to enter Hex values into individual registers. This is useful for debugging the register settings that you will use in your program code.

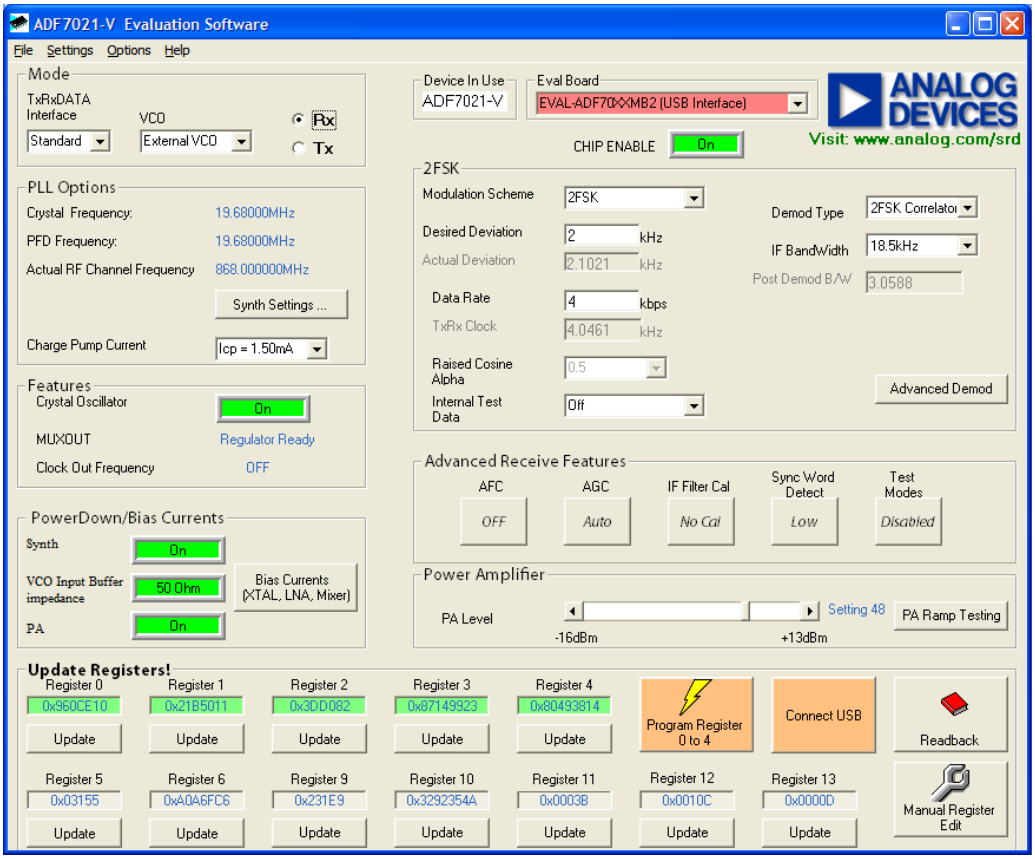


Figure 3. Software Front Panel Display

GETTING STARTED WITH THE ADF7021-V

The evaluation performed will be specific to each application, but this section will enable users to familiarizeze themselves with the features of the ADF7021-V.

Before plugging in the hardware please run "ADF7xxx_ ADIismLINK Install", which contains the necessary USB drivers and dlls! Note if you have installed ADIismLINK Rev1.0 previously you should also run "purge_ADIism_ LINK.bat" to remove the old USB setup from the registry.

Initial Hardware Setup

As described in the Hardware Description section, the evaluation board is divided into two; an RF module containing the ADF7021-V and a mother-board which accepts the RF module and contains the power supply block, analog microcontroller, USB bridge and some I/O pins. You need to mount the RF module onto the mother-board, ensuring correct alignment by having the drill-holes in the module above the supports on the mother board.

The EVAL-7021-VDBxZ must be powered separately to the motherboard. This is done by connecting a voltage supply in the range (3.05V<Vin<12V) to the positive and negative screw terminals on the Daughter Board. The ADF7021-V and the VCO are powered together through a precision 3V regulator on boad.

Communicating to the Hardware and simple debug

To allow register programming of the ADF7021-V, click on 'Connect USB'. Once the software has connected to the target hardware, the button should change to "Disconnect USB".

You will now be able to communicate with the device. To check this you should click on the Readback button and select silicon revision. If you are communicating with the target board and the radio module is plugged in, you should readback a valid code which is then displayed on the top-right of the front panel.

A valid readback code is 0x2120.

Other useful debug modes to check before proceeding onto the main Tx and Rx evaluation are checking CLKOUT operation on an oscilloscope. By default the CLKOUT frequency should be XTAL/8. You can change this value in the software. Another useful debug point is the voltage on the Regulator pins. This should be approximately 2.2V, when CE is active. You can check this by probing the top of C5 (VREG4 pin) on the RF module.

Evaluating the ADF7021-V in Rx and Tx modes

Before setting up an RF link, it is usually informative to evaluate the ADF7021-V in either Tx mode or Rx mode. The typical setup for this is shown in Figures 6 and 7. To select between Tx and Rx modes in the software select the required mode in the top left of the front display panel.

Note: The ADF7021-V daughter boards have a 19.62 MHz TCXO. In the following text for simplicity it will be assumed that the TCXO/crystal is 19.62 MHz.

Test Procedure for the ADF7021-V in Tx Mode

With the USB cable connected use the setup as shown in Figure 6.

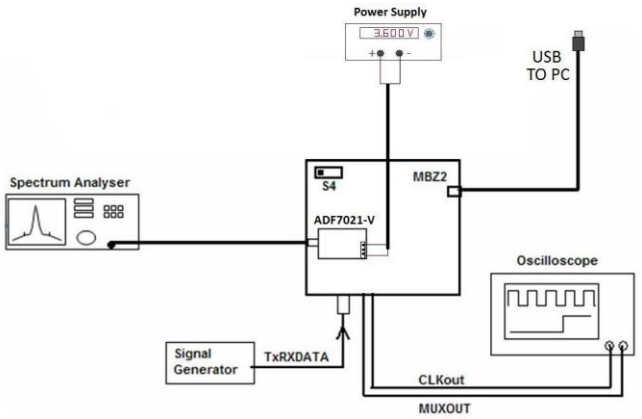


Figure 4. Evaluation board setup for Tx mode

1. Using the ADF7021-V Software, setup the following Tx parameters:
    a. Ensure Tx Mode is selected in Mode sub-section.
    b. Click on Synth Settings and set
        i. RF Channel Frequency (Direct Output) to your desired frequency.
        ii. F(TCXO\XTAL) = 19.68MHz
        iii. FPFD = 19.68MHz
        iv. Hit Calculate and Return to Front Panel.

c. Power-Down/Bias Currents sub-section. Defaults should be

i. Crystal oscillator (OSC) ON

ii. Chip Enable ON

iii. PA ON

d. Modulation Options

i. Select 2FSK

ii. Set Internal Test Data to "Tx Carrier"

iii. Using slide-bar change the power setting to 48.

2. Hit the Program Registers 0-4 Button on the Software. This will will program the registers using the correct power up sequence as outlined in the ADF7021-V datasheet.
3. Examine the output using the spectrum analyser. The output should be locked to the programmed output frequency and the output power should be approximately +10dBm. There will be some small error in the TX frequency due to the TCXO error but this should be <500Hz. You can adjust the output power using the output power slide-bar in the software.
4. Re-enter the Synth Settings sub-window and change the output frequency and verify it covers your required frequency range.
5. In-band Phase Noise is measured by narrowing the span on the spectrum analyser to10kHz and turning Marker Noise ON. ADI SRD Design Studio will help you predict the expected phase noise numbers.
6. You can now apply modulation to the TxDATA pin using an external data generator connected to the TxRxDATA SMA. This will allow you to monitor spurious, adjacent channel power and harmonic levels. Alternatively you can select the "Tx PN9 sequence" testmode from the "Internal Test Data" pull-down menu which uses an internal PN9 pattern generator to modulate the RF carrier.

Test Procedure for the ADF7021-V in Rx mode

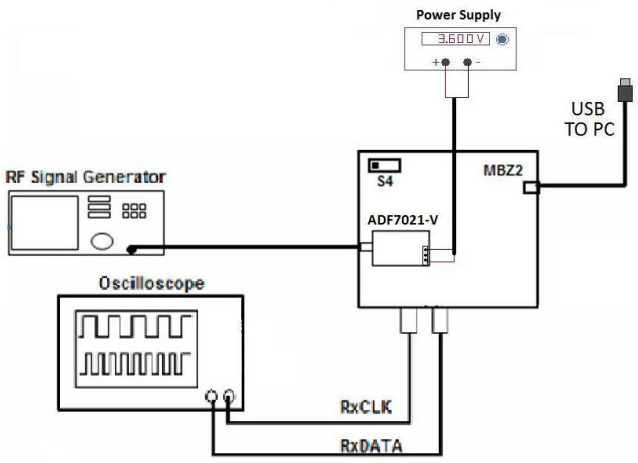


Figure 5. Evaluation board setup for Rx mode

With the USB cable connected use the setup as shown in Figure

7. It is important to note that the ADF7021-V uses a low-IF architecture where the IF is operating at 100 kHz. This means the LO frequency should be set to 100 kHz below the incoming RF frequency. The ADF7021-V software takes care of this automatically for you.
8. Setup your signal generator to output a 2FSK signal at the desired frequency, and –70dBm level. Select the data-rate (4.8kbps) and deviation frequency (2.4 kHz). Set the data modulation to 1010 data.
9. Using the ADF7021-V software, setup the following Rx parameters:

a. Ensure Rx Mode is selected in Mode sub-window

b. In Synth Settings select the RF Frequency to the signal generator Output frequency. The LO will automatically be programmed to RF – 100 kHz.

c. Modulation Options

i. Select 2FSK Modulation

ii. Set Desired Deviation = 2.4kHz

iii. Set Data-Rate = 4.8 (kbps)

iv. Set Demod Type = Correlator

v. Set IF Bandwidth = 18.5kHz

10. Hit the Program Registers 0-4 Button on the Software
11. Click on the IF Filter cal button. This will open the IF filter cal window. Click the "Do Coarse cal" button. This will automatically perform an IF Filter coarse calibration (which is recommended on every power up in Rx mode).

12. Using the scope, probe the RxTxData pin and RxTxCLK. They should be 3V p-p square-waves with frequencies of 2.4 kHz (i.e. 1010 data at 4.8kbps) and 4.8 kHz respectively. Ensure that these square-waves are triggered correctly and are not flickering.

13. If you don't have a built-in BER tester you can estimate the sensitivity point, by reducing the level on the frequency generator until you see the RxTxData waveform 'flickering' which corresponds to errors in the received data. Typically if you see a flicker/error once per second you can roughly estimate this to be the sensitivity point. Note the level on the Signal Generator when this happens. For this setup it should be –116dBm +/- 2dBm.

Readback Function

It is possible to enable the on-chip ADC on the ADF7021-V and readback a selection of parameters, including battery voltage, temperature (from the on-board temperature sensor), Frequency Error, External voltage and RSSI.

To activate this feature, click on the Readback Toggle button. In the sub-window select the type of readback required. The appropriate value should be displayed on the screen. In Tx mode the ADC is powered-off by default to save power, so in order to readback correctly you need to enable the ADC. This can be done by clicking the status button in the ADC Status section to "ON" before clicking the Readback button. Since the ADC is used in Rx mode for the AGC function, the ADC is powered-on by default in this mode. Thus in Rx mode, valid battery voltage, temperature, frequency error and external voltage readback data are not possible.

In practical cases the user would typically do a battery voltage readback in Tx mode or in low-power measure mode. Lowpower measure mode is entered by simply bringing CE high, enabling the ADC in Register8, selecting the desired readback value in Register7 and performing the readback.

SETTING UP AN RF LINK USING ADIISMLINK

The ADIismLINK software is the simplest way to setup an RF Link. This allows you to perform several functions:

- Setup a wireless star-network and send back sensor data (temperature/accelerometer or user defined) to the basestation to be displayed or logged on the pc.
- transmit simple text messages from Base Station node to remote nodes and vice versa.
- Transmit temperature data using the temperature sensor (TMP36) or tilt (pitch and roll angle) data using the accelerometer (ADXL322).
- Run a Packet Error Rate (PER) test to test link quality
- Perform range tests
- Develop user applications on top of the example PHY/MAC layer (Frequency hopping and duty-cycle MAC options)

Refer to the ADIismLINK User Guide and Manual for more information on using ADIismLINK.

SETTING PLL LOOP BANDWIDTHS

The Eval Boards have been built using a 6kHz PLL LBW. From measurements made on SNR and modulation quality of the FSK signal, it is recommended to use a LBW > 1.5 x Datarate.

So for the default filter on the Eval Board, this gives a max. data rate close to 4.8kbps. If you want to operate the board at higher data-rates you need to modify the loop filter. For the ADF7021-V it is recommended to use ADI SRD Design Studio to design the loop filter. The loop filter is set at this value to give optimum ACP and ACR for 12.5 kHz and 25 kHz channel spacing's. For the ADF7021-V it is recommended to use ADI SRD Design Studio to design the loop filter.

ADI SRD Design Studio allows you to simulate these effects and design loop filters for various data-rates and different RF Output frequencies. For output frequency/xtal/data-rate combinations not covered below you should use ADI SRD Design Studio.

ADF7021-VDBXZ BOARD OPTIMISATION

Output Matching Circuit

The ADF7021-V exhibits optimum performance in terms of sensitivity, transmit power, and current consumption, only if its RF input and output ports are properly matched to the antenna impedance. For cost-sensitive applications, the ADF7021-V is equipped with an internal Rx/Tx switch, which facilitates the use of a simple combined passive PA/LNA matching network as outlined in Figure 4.

For ease of design the matching and harmonic filter components are provided for the most commonly used bands (see Tables5 to11) Please refer to Application Note AN-764 and Application Note AN-859 for more details on PA/LNA matching for the ADF7021-V devices.

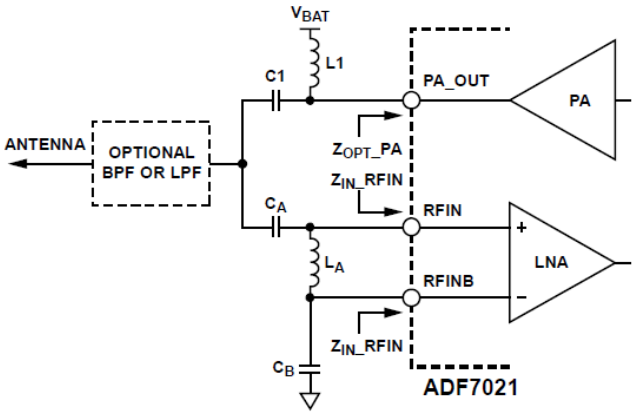


Figure 6. LNA/PA Output Matching Circuit

Choice of VCO for ADF7021-V

The ADF7021-V uses an external VCO.

- The ADF7021DB1Z uses a 900-940Mhz VCO
- The ADF7021DB2Z uses a 1736-1740MHz VCO
- Voltage supply range for both is (2.85<Vcc<3.15)
- Tuning Voltage range for both is (0.2V<Vtune<2.2V)
- Both VCO's are supplied by Sangshin.

IF Filter

The IF Filter response can be viewed on a SA by AC coupling either test point F1 or F2 pf the ADF7021-V to the Spectrum Analyzer as shown in Figure 7.

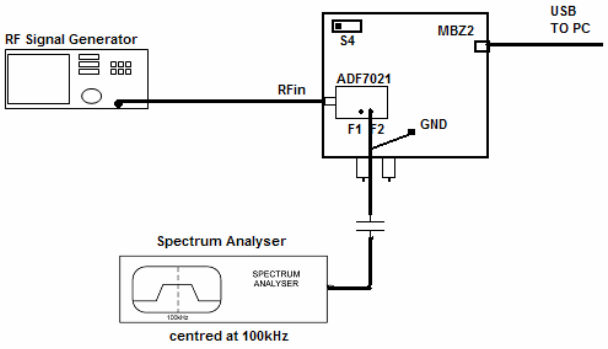


Figure 7. Setup for viewing IF Filter response

Using an External Reference Frequency

During evaluation it may be necessary to use a signal generator instead of a crystal/TCXO for debug or evaluation purposes. To allow this simply remove capacitor C18 from the ADF7021-V daughter board and place a 100pF capacitor at C17. The external signal source can then be connected to the EXT_REF test point on the MBZ2 mother board.

Analog RSSI

For debug of your design it may be useful to look at the analog RSSI. This can be enabled in the software under Test Modes and ticking "Analog RSSI". The analog RSSI signal is then available on the daughter board test point T1.

Test DAC Output

The ADF7021-V provides access to the 2FSK/3FSK/4FSK demodulator output to facilitate external measurement of functions such as demodulator output SNR, receiver eyediagram analysis, and analog FM demodulation. For these measurements, access to the digital FSK demodulator output is achieved by using an on-chip ΣΔ (SD) modulator in conjunction with an external, passive RC network. This network provides an analog output signal (test DAC output) to replicate the output of the on-chip digital FSK demodulator.

Refer to Application Note AN-852 for information on setting up and using the Test DAC.

Figure 8 shows the Test DAC RC filter connections. To allow use of the Test DAC the following modifications need to be made to the mother board:

- Populate R40 with a zero ohm link

- Populate R43 with a 660 ohm resistor.
- Remove R39. This is necessary in order to disconnect the SWD line from the MCU interrupt pin. If the user wishes to use ADIismLINK at some stage then this resistor will have to be re-populated (100ohm) as the ADIismLINK protocol needs the SWD interrupt.

The RC filters components R44, R45, C36. C37 and C38 are already populated. This will provide adequate filtering for datarates between 1kbps and 4.8kbps.

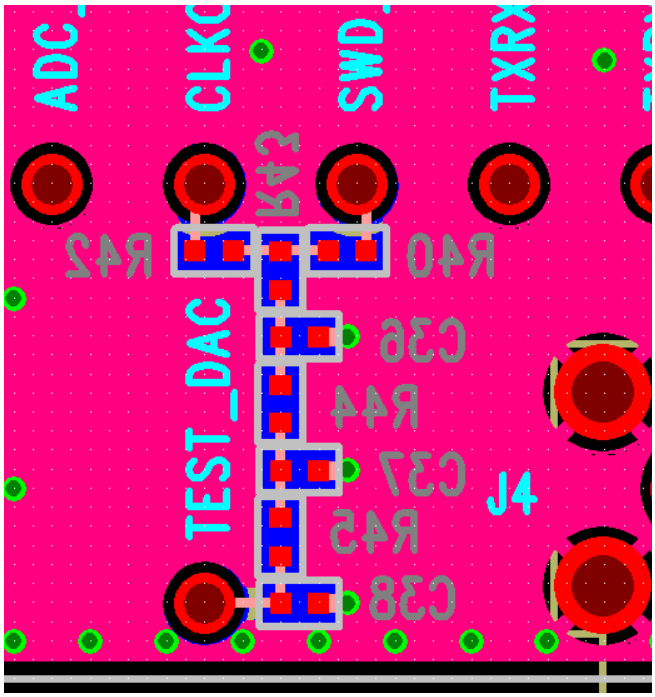


Figure 8. Underside of EVAL-ADF70xxMBZ2 board showing Test DAC Connections

INSTALLING THE USB DRIVERS FOR THE EVAL-ADF70XXMBZ2 BOARD

System Requirements

- Microsoft Windows 2000 or XP
- One available USB port (preferably USB2)

Driver files

The files required to install the UDB driver are:

- `CyUSB.sys` – the Cypress generic USB driver
- `ADF70XXDK2.inf` – the setup information file
- `ADF70XXDK2.spt` – the EZ-USB firmware (the last three digits of the filename represent the version)

Make sure you have these files available before plugging the board in for the first time.

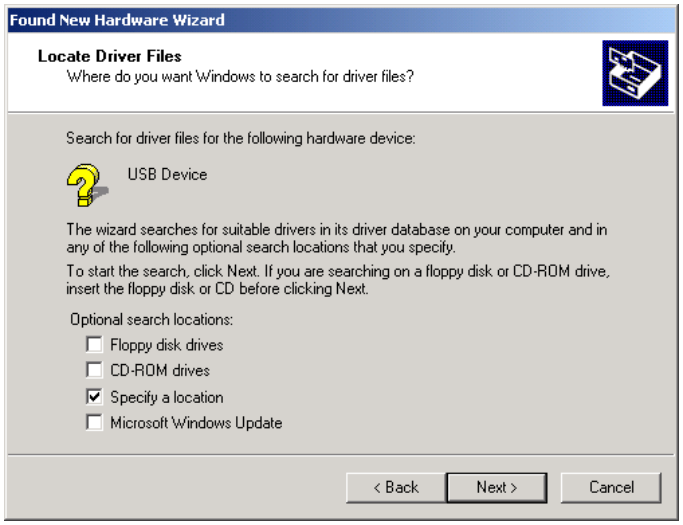
Installing

The software "ADF7xxx_ADIismLINK Install" should be downloaded from the CD or analog.com website and installed on your pc before plugging in the hardware. This zip file contains the relevant USB drivers and firmware necessary for operation of the EVAL-ADF70XXMBZ2 board. Note if you have installed ADIismLINK Rev1.0 previously you should run "purge_ADIismLINK.bat" to remove the old USB setup from the registry.

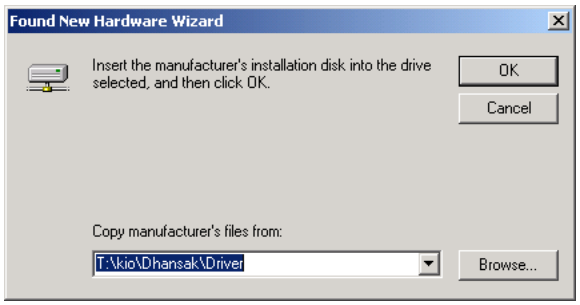
1. Windows 2000

Plug in the ADF7021-V development board, the "**Found New Hardware Wizard**" will appear after a while, click "Next >":

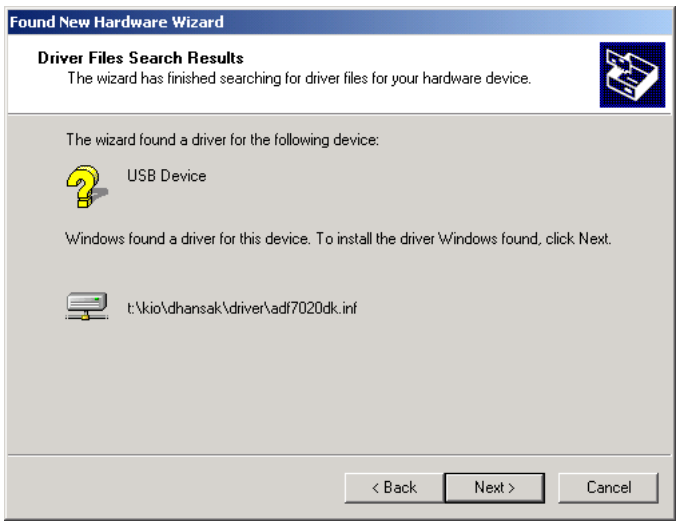
Choose "Search for a suitable driver for my device (recommended)" and click "Next >". You will be asked where Windows should look for the driver files:



Make sure that **only** "Specify a location" is checked then click "Next >". You will be prompted for the location of the driver files:



Browse to the directory where you put the driver files then click "OK". The default path is C:\Program Files\Analog Devices BV\ADF7xxx Evaluation Software/USB Drivers. You will be told that Windows has found a driver:

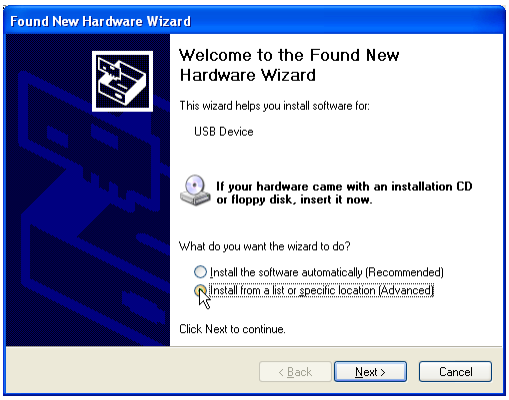


Click "Next >". You will be told that the software is now installed:

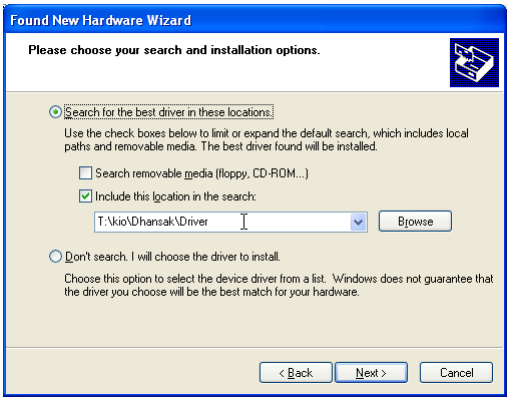
Click "Finish". The EZ-USB firmware will now be loaded and the development will appear as a new device, Windows should find the driver for it automatically.

2. Windows XP

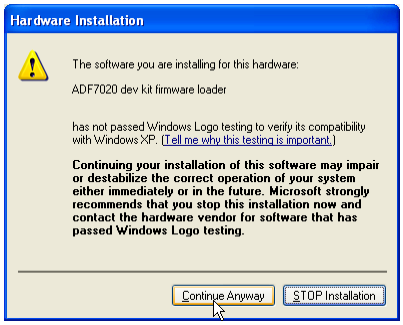
Plug in the ADF7021 development board, the "**Found New Hardware Wizard**" will appear after a while:



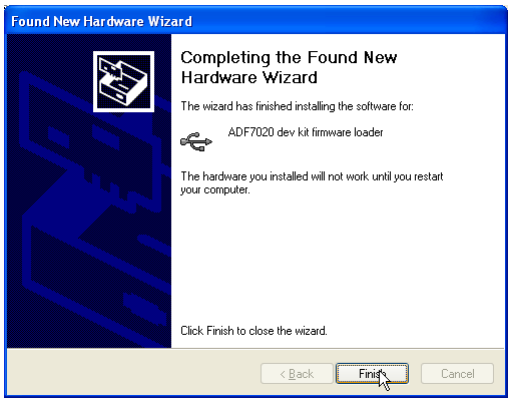
Choose "Install from a list of specific location (Advanced)" and click "Next >". You will be asked where Windows should look for the driver files:



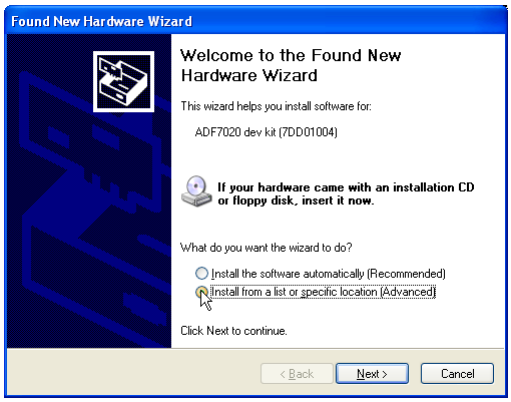
Choose "Search for the best driver in these locations", make sure "Search removable media" is **not** selected and that "Include this location in the search" **is** selected. Browse to the directory where you put the driver files then click "Next >". You will be informed that the driver has not passed Windows testing:



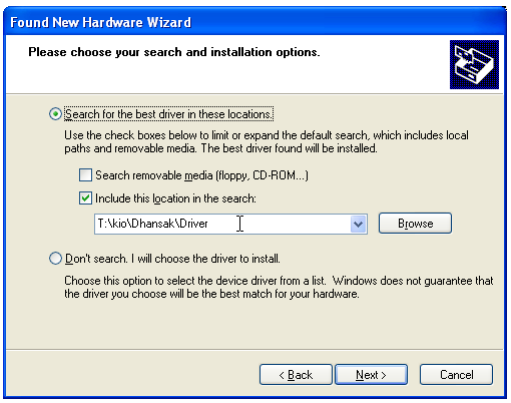
Click "Continue Anyway". Once Windows has finished copying files and installing the driver you will be told that the wizard has completed:



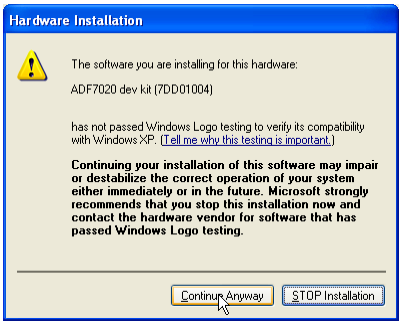
Click "Finish". At this point the EZ-USB firmware will be loaded into the development kit and it will reappear as a different USB device, the "Found New Hardware Wizard" will pop up again:



Choose "Install from a list or specific location (Advanced)" then click "Next >". You will be asked where Windows should look for the driver files:

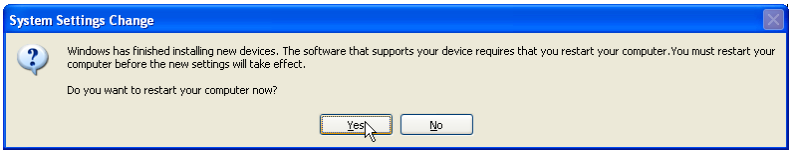


As before, choose "Search for the best driver in these locations" and "Include this location in the search". Click "Next >". You will be reminded that the driver has not passed Windows testing:



Click "Continue Anyway". Once Windows has finished copying files and installing the driver you will be told that the wizard has completed:

Click "Finish". You may be prompted to restart your computer:



If this appears you should restart the computer before trying to use any of the software that depends on the USB driver (ADF7020, ADF7012, ADF7025, ADF7021 .exes or ADF70xxHost).

BILL OF MATERIALS

Table 2. Bill Of Materials for the EVAL-ADF7021-VDBX Daughter Boards

EVAL-ADF7021-VDB1Z BOM (450-470MHz using 920MHz VCO)				
ADF7021-VDBxZ				
Qty	Name	VALUE	MFG PART#	PART DESCRIPTION
1	U4		ADP3300ARTZ-3	LDO 3.0V
1	C1	4.7pF	GRM1555C1H4R7CZ01D	CAP 0402
1	C3	6.8pF	GRM1555C1H6R8DZ01D	CAP 0402
1	C2	10pF	GRM1555C1H100JZ01D	CAP 0402
1	C11	39nF	ECJ-0EB1A393K	CAP 0402
1	C39	1uF	GRM155R60J105ME19D	CAP 0402
1	C13	10nF	GRM155F51E103ZA01D	CAP 0402
1	C34	10pF	GRM1555C1H100JZ01D	CAP 0402
8	C4 C7 C9 C16 C20 C25 C31 C38	10nF	GRM155R71E103KA01D	CAP CER 10000PF 25V 10% X7R 0402
4	C5 C10 C15 C19	100nF	GRM155R61A104KA01D	CAP CER .1UF 10V 10% X5R 0402
2	C29 C33	1uF	GRM155R60J105ME19D	CAP 0402
1	C17	22pF	GRM1555C1H220JZ01D	CAP CER 22PF 50V 5% C0G 0402
1	C8	220pF	GRM1555C1H221JA01D	CAP CER 220PF 50V 5% C0G 0402
1	C14	22nF	ECJ-0EB1C223K	CAP 0402
2	C6 C35	0.1uF	GRM188R71C104KA01D	CAP 0603
1	C21	10uF	C0805C106K8PAC-TU	CAPACITOR, 0805, 10UF, 10V, X5R
1	C22	8.2pF	ECD-G0E8R2C	CAP CERAMIC 8.2PF 25V C0G 0402
1	C23	12pF	GRM1555C1H120JZ01D	CAP CER 12PF 50V 5% C0G 0402
1	C24	8.2pF	ECD-G0E8R2C	CAP CERAMIC 8.2PF 25V C0G 0402
1	C30	22uF	GRM21BR60J226ME39L	CAP CER 22UF 6.3V 20% X5R 0805
1	J3		CTB5000/3	3 Pin Terminal Block (5mm Pitch)
1	J5			2 Pin Jumper
1	Y1		TXO812025LJ-19.68MHz-3.0R	TXCO 19.68MHz 2.5ppm 5.0x3.2x1.3
1	J1		76342-307LF	14 Pin (7x2)
1	l4	11nH	0402CS-11NX-JLU	Coilcraft 0402CS-11NX-JLU
1	L5	11nH	0402CS-11NX-JLU	Coilcraft 0402CS-11NX-JLU
1	L1	13nH	0402CS-13NX-JLU	Coilcraft 0402CS-13NX-JLU
1	L2	27nH	0402CS-27NX-JLU	Coilcraft 0402CS-27NX-JLU
1	R2	240	RC0402JR-07240RL	RES 0402
3	R5-7	180r	ERJ-2GEJ181X	RES 0402
1	R4	2.7k	ERJ-2GEJ272X	RES 0402
1	R13	390k	ERJ-2GEJ394X	RES 0402
1	R3	3.6k	ERJ-2RKF3601X	RES 0402
1	R8	4.3r	RC0402JR-074R3L	RES 0402
1	R9	56	RC0402JR-0756RL	RES 0402
1	R10	0r	RC0402JR-070RL	RES 0603
1	U2		SEV-3V920AP	Low Voltage, Low PN VCO
1	U1		ADF7021-VBCPZ	ISM Band TRX (Ext VCO)
1	J2		142-0701-851	CONN JACK END LAUNCH PC GOLD SMA
1	F5	Black	20-2137	TERMINAL, PCB BLACK

Table 3. Bill Of Materials for the EVAL-ADF7021-VDB2Z Daughter Boards

EVAL-ADF7021-VDB2Z BOM				
ADF7021-VDBZ				
Qty	Reference	VALUE	MFG PART#	PART DESCRIPTION
1	U4		ADP3300ARTZ-3	LDO 3.0V
1	C1	2.7pF	GRM1555C1H2R7CZ01D	CAP 0402
1	C3	3.0pF	GRM1555C1H3R0CZ01D	CAP 0402
1	C2	8.2pF	500R07S8R2CV4T	CAP 0402
1	C11	6.8nF	GRM155R71E682KA01D	CAP 0402
1	C39	100nF	GRM155R61A104KA01D	CAP 0402
1	C13	1.8nF	ECJ-0EB1H182K	CAP 0402
1	C34	10pF	GRM1555C1H100JZ01D	CAP 0402
8	C4 C7 C9 C16 C20 C25 C31 C38	10nF	GRM155R71E103KA01D	CAP CER 10000PF 25V 10% X7R 0402
4	C5 C10 C15 C19	100nF	GRM155R61A104KA01D	CAP CER .1UF 10V 10% X5R 0402
2	C29 C33	1uF	GRM155R60J105ME19D	CAP 0402
1	C17	22pF	GRM1555C1H220JZ01D	CAP CER 22PF 50V 5% C0G 0402
1	C8	220pF	GRM1555C1H221JA01D	CAP CER 220PF 50V 5% C0G 0402
1	C14	22nF	ECJ-0EB1C223K	CAP 0402
2	C6 C35	0.1uF	GRM188R71C104KA01D	CAP 0603
1	C21	10uF	C0805C106K8PAC-TU	CAPACITOR, 0805, 10UF, 10V, X5R
1	C22	NC	NC	NC
1	C23	3.9pF	GJM1555C1H3R9CB01D	CAP CER 3.9PF 50V C0G 0402
1	C24	NC	NC	NC
1	C30	22uF	GRM21BR60J226ME39L	CAP CER 22UF 6.3V 20% X5R 0805
1	J3		CTB5000/3	3 Pin Terminal Block (5mm Pitch)
1	J5			2 Pin Jumper
1	Y1		TXO812025LJ-19.68MHz-3.0R	TXCO 19.68MHz 2.5ppm 5.0x3.2x1.3
1	J1		76342-307LF	14 Pin (7x2) vertical card connector
1	14	5.1nH	0402CS-5N1X-JLU	Coilcraft 0402CS-5N1X-JLU
1	L5	6.8nH	0402CS-6N8X-JLU	Coilcraft 0402CS-6N8X-JLU
1	L1	4.3nH	0402CS-4N3X-LU	Coilcraft 0402CS-4N3X-LU
1	L2	8.7nH	0402CS-8N7X-LU	Coilcraft 0402CS-8N7X-LU
1	R2	1.3k	ERJ-2GEJ132X	RES 0402
3	R5-7	180r	ERJ-2GEJ181X	RES 0402
1	R4	2.7k	ERJ-2GEJ272X	RES 0402
1	R13	390k	ERJ-2GEJ394X	RES 0402
1	R3	3.6k	ERJ-2RKF362X	RES 0402
1	R8	4.3r	RC0402JR-074R3L	RES 0402
1	R9	470R	ERJ-2GEJ471X	RES 0402
1	R10	0r	RC0402JR-070RL	RES 0603
1	U2		SEV-3V1738AP	Low Voltage, Low PN VCO
1	U1		ADF7021-VBCPZ	ISM Band TRX (Ext VCO)
1	J2		142-0701-851	CONN JACK END LAUNCH PC GOLD SMA
1	F5	Black	20-2137	TERMINAL, PCB BLACK

SCHEMATICS

EVAL-ADF7021-VDBxZ Daughter Board

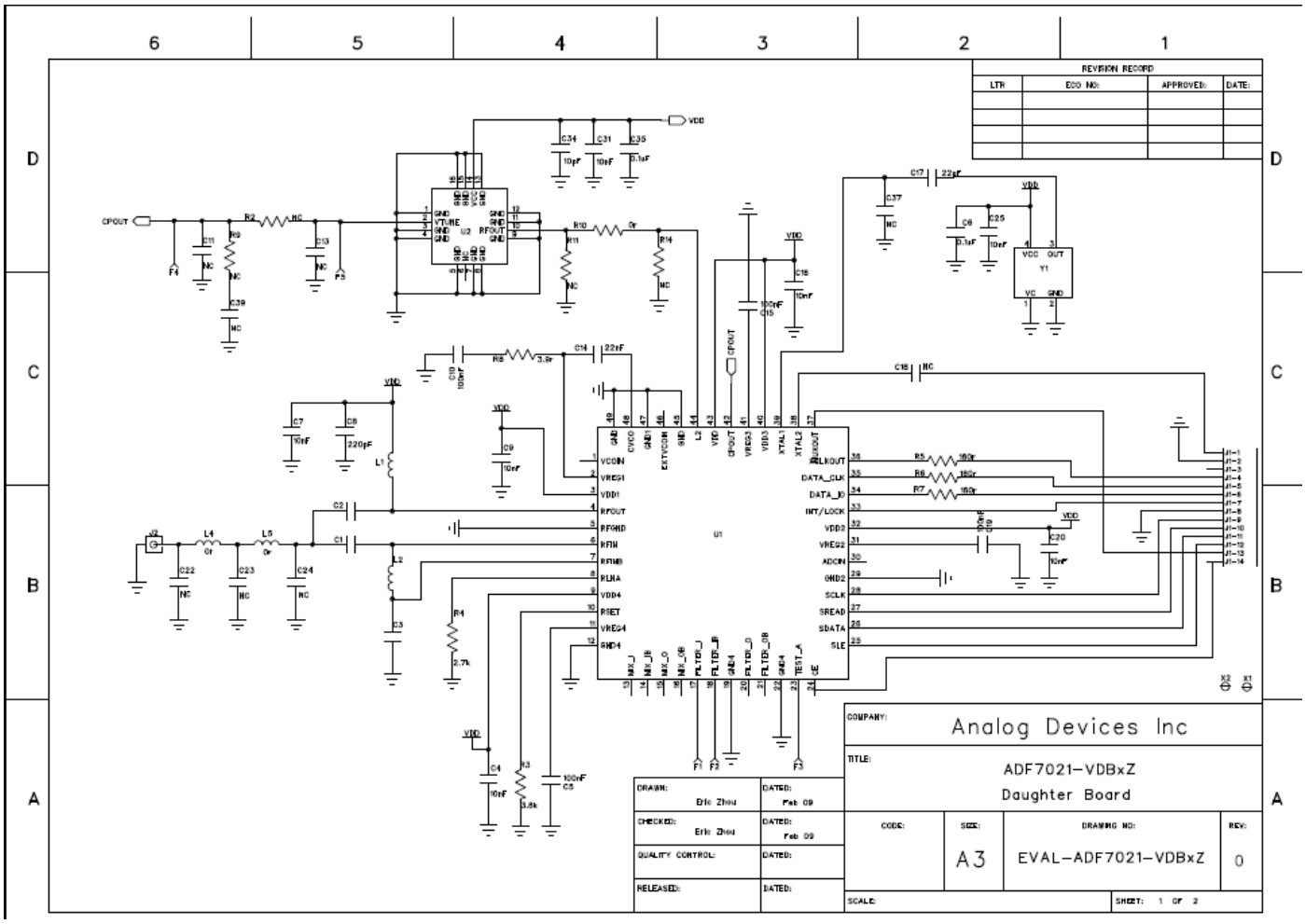


FIGURE 9. TOP LAYER SCHEMATIC FOR EVAL-ADF7021-VDBXZ DAUGHTER BOARDS

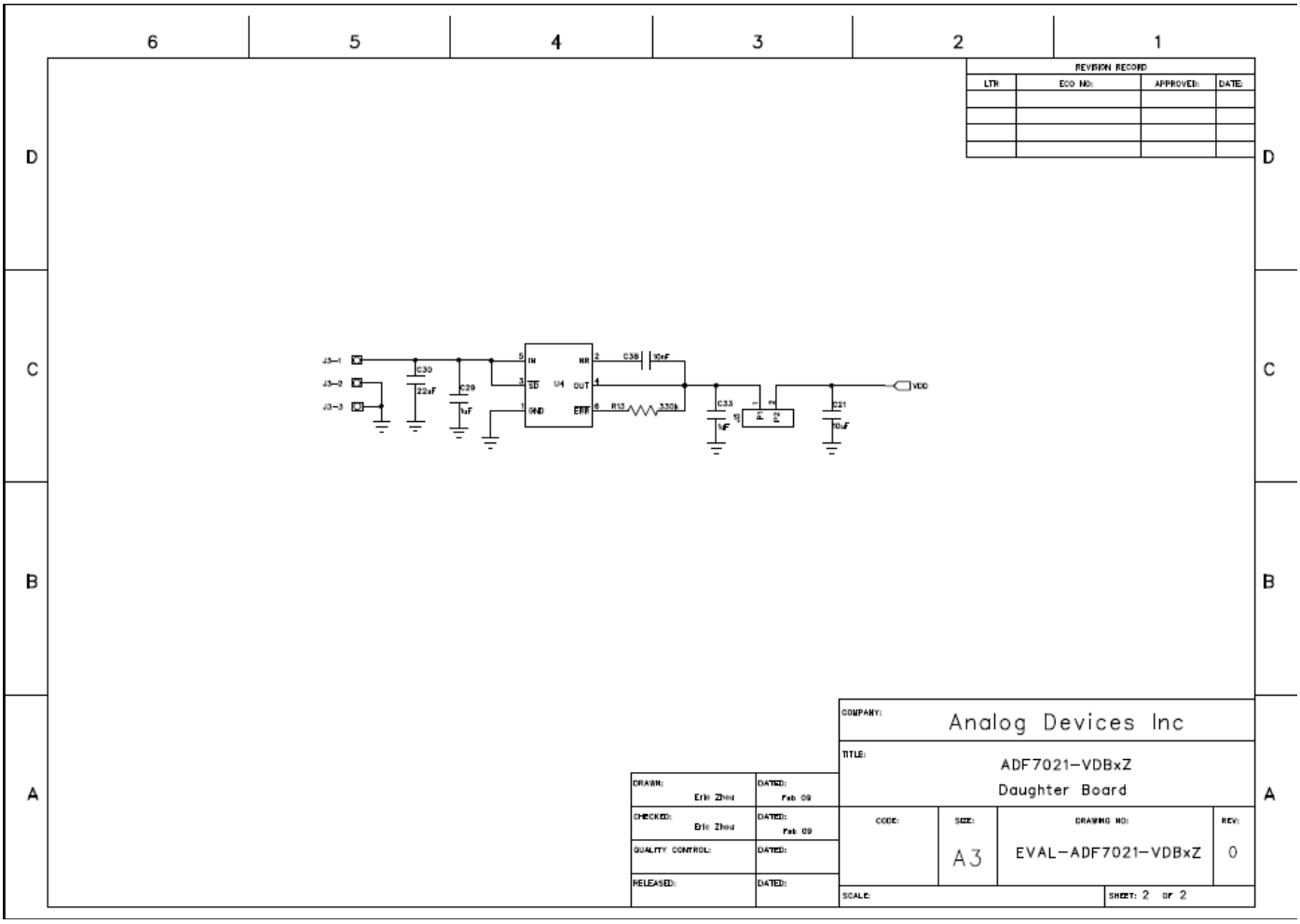


FIGURE 10. BOTTOM LAYER SCHEMATIC FOR EVAL-ADF7021-VDBXZ DAUGHTER BOARDS

ADF70XXMBZ2 Mother Board

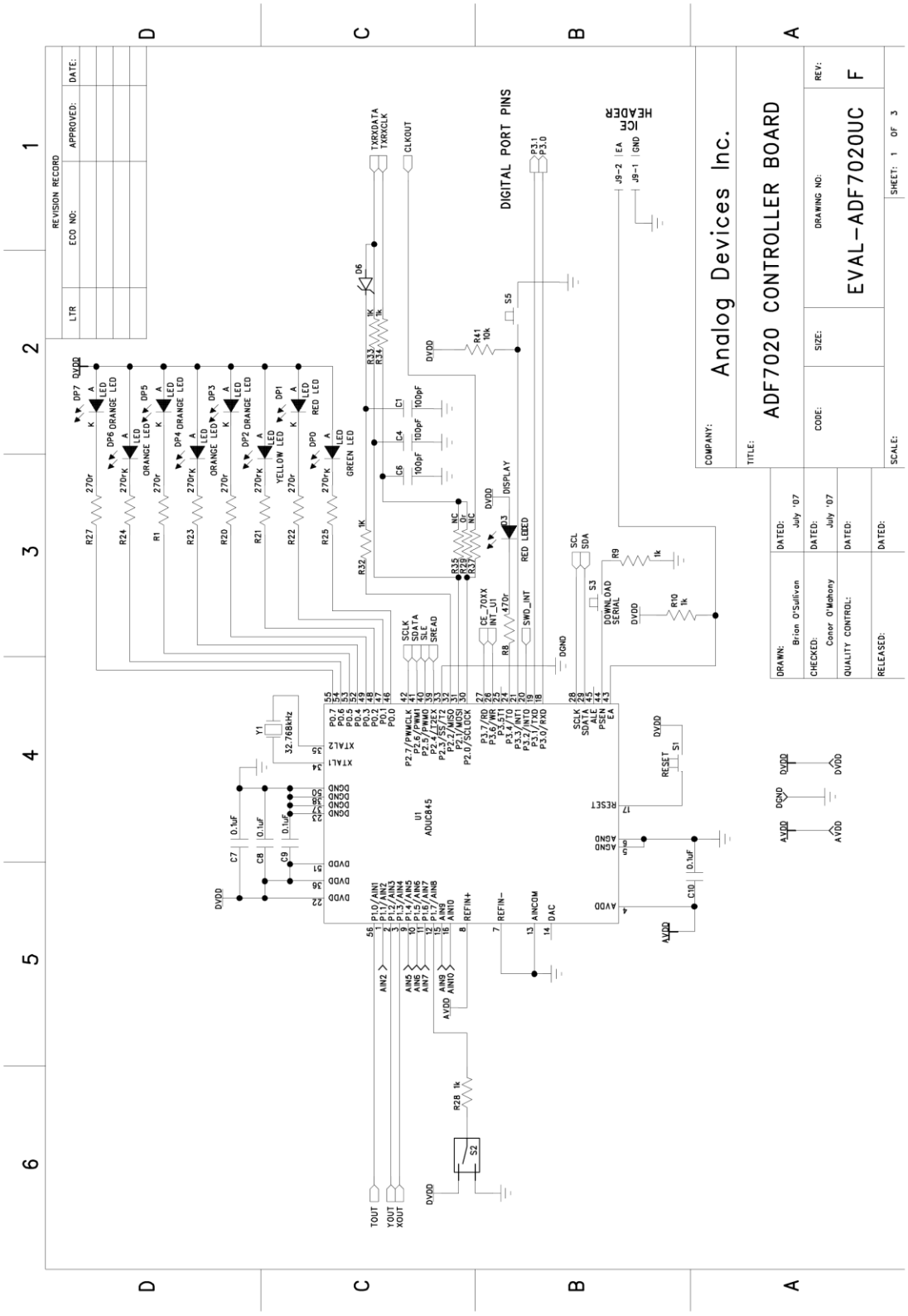


Figure 11. EVAL-ADF70XXMBZ2 Mother Board Schematic – MCU to RF Header section

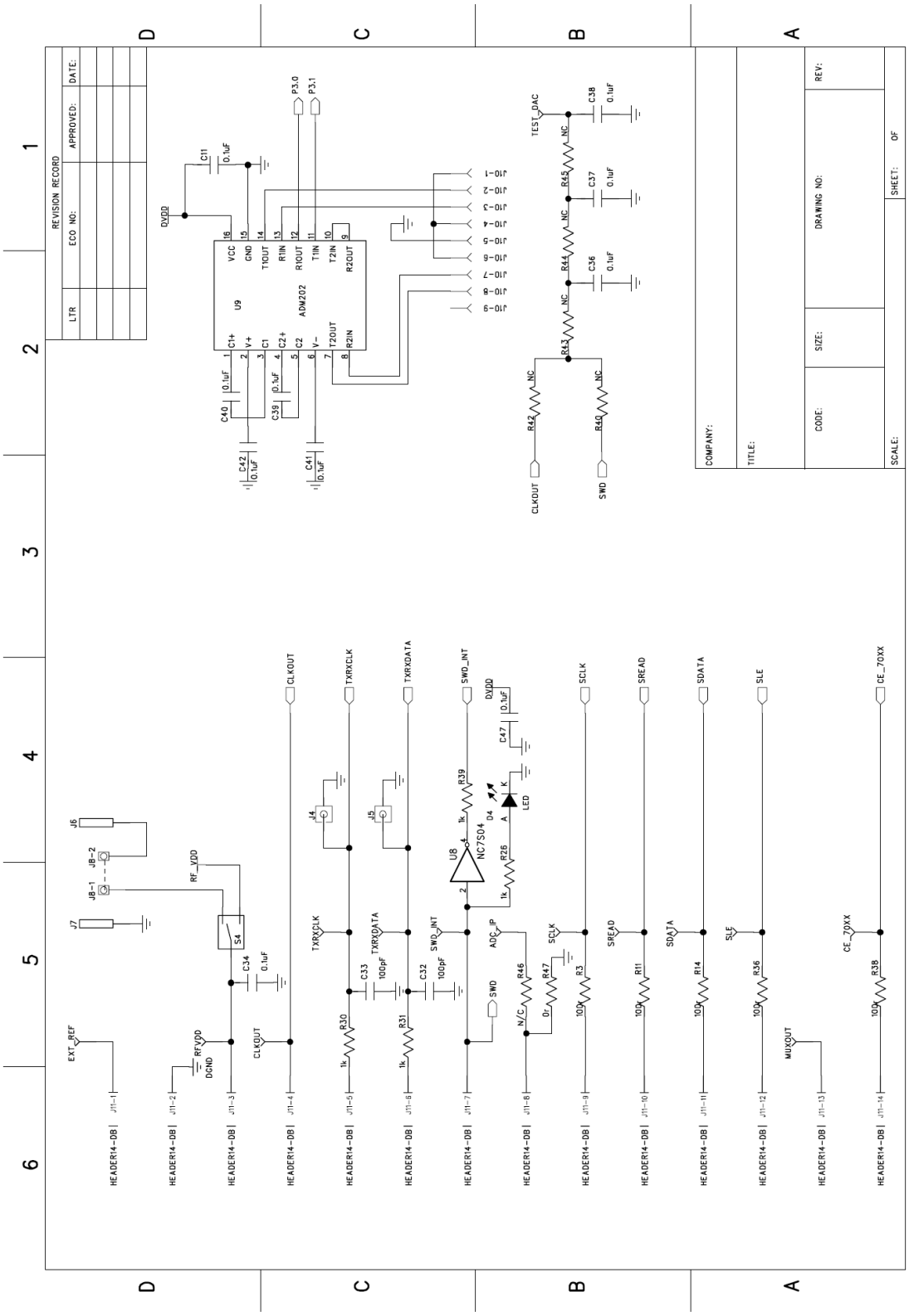


Figure 12. EVAL-ADF70XXMBZ2 Mother Board Schematic – MCU to RF Header section

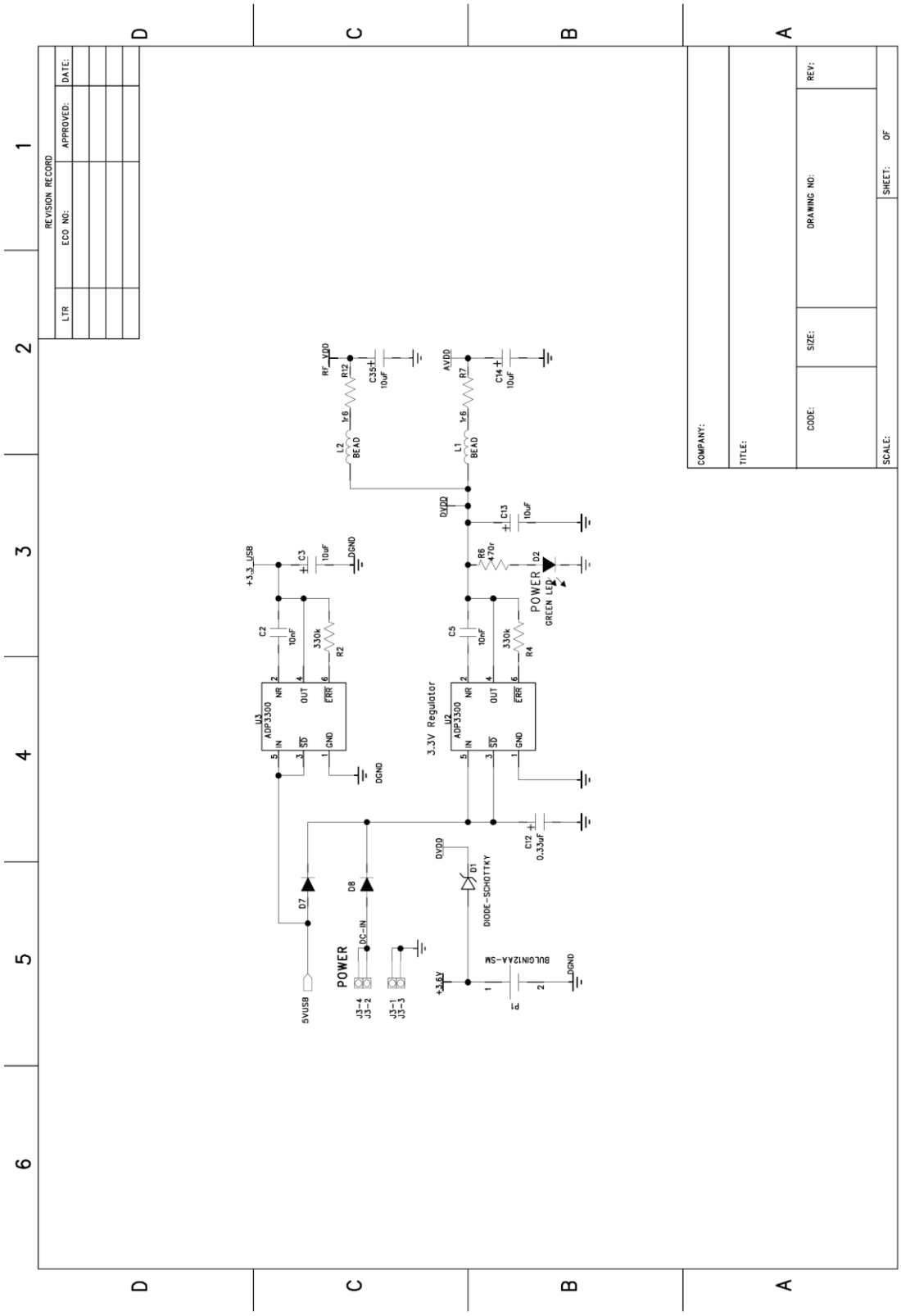


Figure 13. EVAL-ADF70XXMBZ2 Mother Board Schematic - Power section

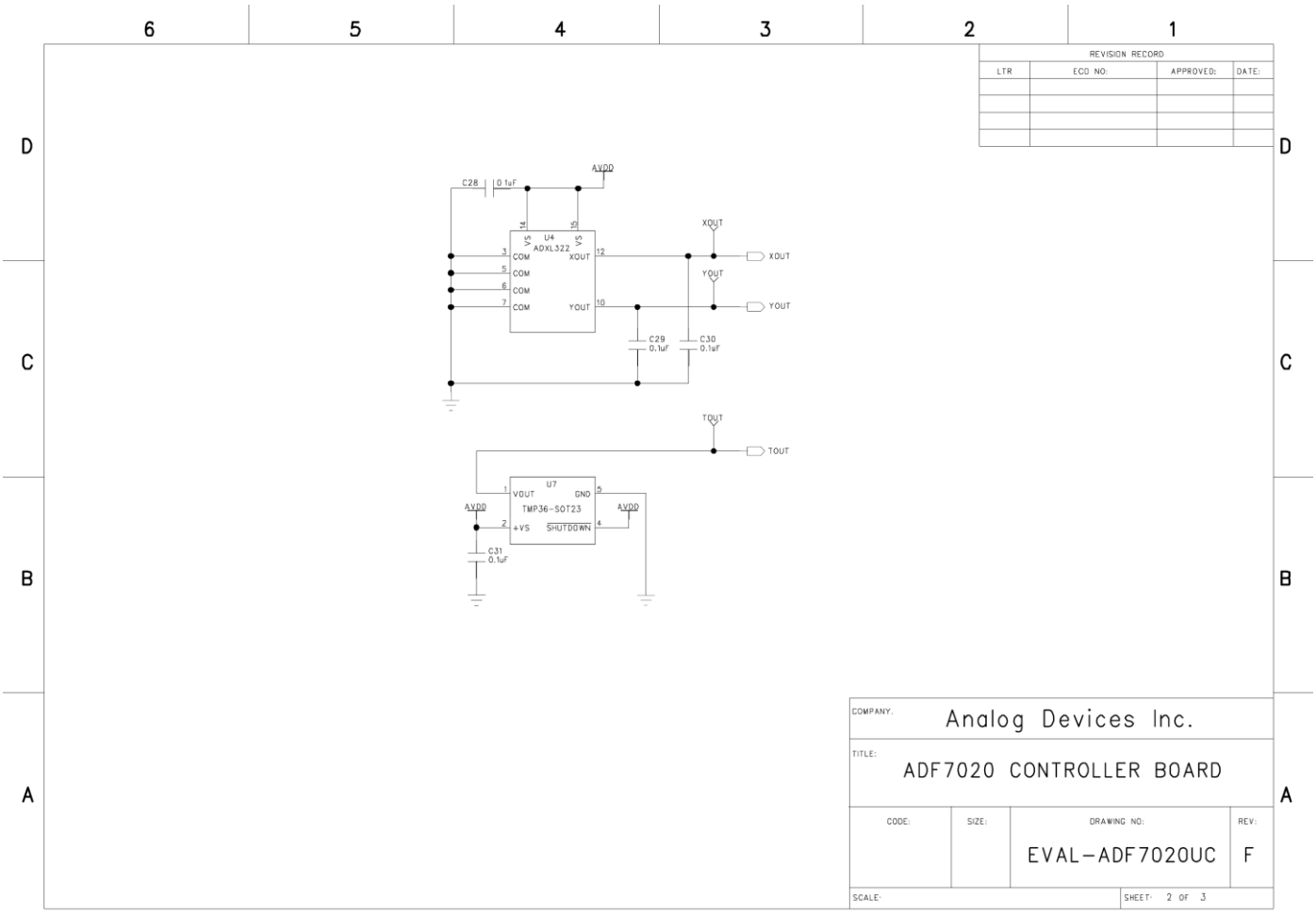


Figure 14. EVAL-ADF70XXMBZ2 Mother Board Schematic - Sensor section

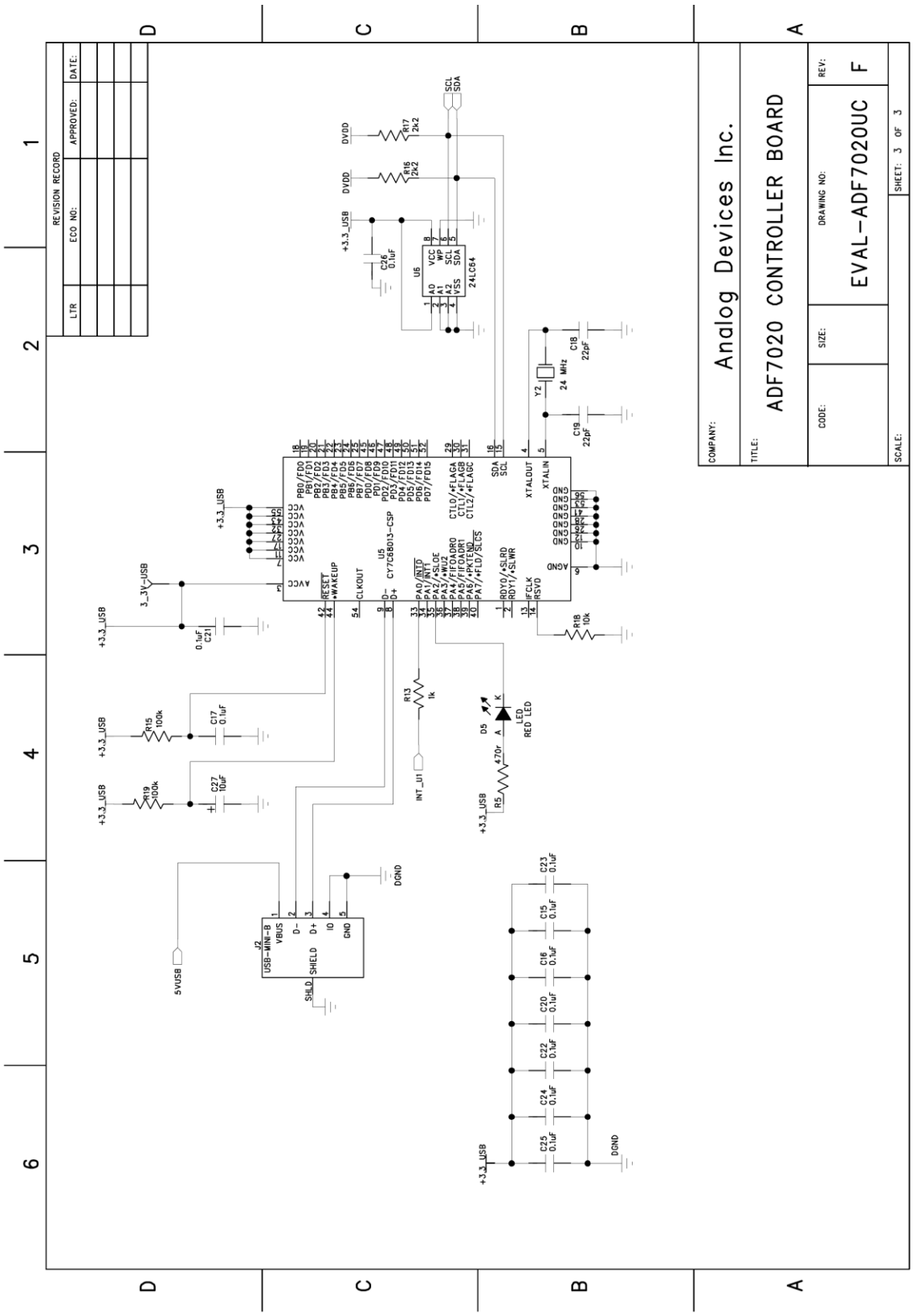


Figure 15. EVAL-ADF70XXMBZ2 Mother Board Schematic - USB section

NOTES