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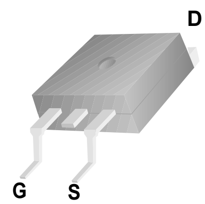
August 2015

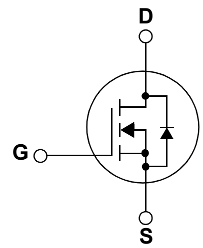
FDB9403L_F085

N-Channel Logic Level PowerTrench® MOSFET

40 V, 110 A, 1.2 mΩ



TO-263
FDB SERIES



Features

- Typical $R_{DS(on)}$ = 1.0 mΩ at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 186 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems

For current package drawing, please refer to the Fairchild website at https://www.fairchildsemi.com/package-drawings/TO/TO263A02.pdf

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1)	T_C = 25°C	110	A
	Pulsed Drain Current	T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	634	mJ
P_D	Power Dissipation		333	W
	Derate Above 25°C		2.22	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.45	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	43	°C/W

Notes:
1: Current is limited by bondwire configuration.
2: Starting T_J = 25°C, L = 0.3mH, I_{AS} = 65A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.
3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB9403L	FDB9403L_F085	D2-PAK(TO-263)	330mm	24mm	800 units

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Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=40V,	T_J = 25°C	-	-	1	μA
		V_{GS} = 0V	T_J = 175°C (Note 4)	-	-	3	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		1.0	1.8	3.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80A, V_{GS}= 4.5V		-	1.2	1.6	mΩ
		I_D = 80A,	T_J = 25°C	-	1.0	1.2	mΩ
		V_{GS}= 10V	T_J = 175°C (Note 4)	-	1.7	2.0	mΩ
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0V, f = 1MHz		-	13500	-	pF
C_{oss}	Output Capacitance			-	4300	-	pF
C_{rss}	Reverse Transfer Capacitance			-	280	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.7	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V	V_{DD} = 32V I_D = 80A	-	186	245	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	23	-	nC
Q_{gs}	Gate-to-Source Gate Charge			-	33	-	nC
Q_{gd}	Gate-to-Drain “Miller“ Charge			-	22	-	nC
Switching Characteristics							
t_{on}	Turn-On Time	V_{DD} = 20V, I_D = 80A, V_{GS} = 10V, R_{GEN} = 6Ω		-	-	156	ns
$t_{d(on)}$	Turn-On Delay			-	16	-	ns
t_r	Rise Time			-	63	-	ns
$t_{d(off)}$	Turn-Off Delay			-	142	-	ns
t_f	Fall Time			-	107	-	ns
t_{off}	Turn-Off Time			-	-	399	ns
Drain-Source Diode Characteristics							
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} =80A, V_{GS} = 0V		-	-	1.25	V
		I_{SD} = 40A, V_{GS} = 0V		-	-	1.2	V
t_{rr}	Reverse-Recovery Time	I_F = 80A, dI_{SD}/dt = 100A/μs, V_{DD}=32V		-	114	171	ns
Q_{rr}	Reverse-Recovery Charge			-	205	328	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics

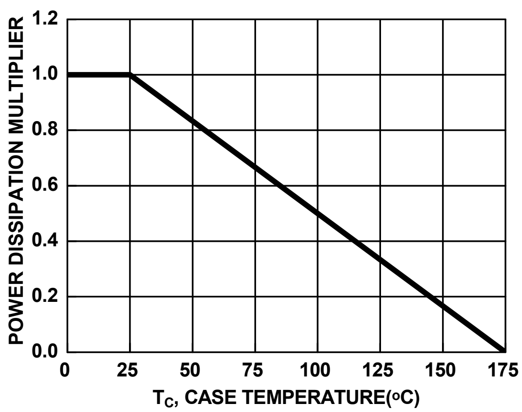


Figure 1. Normalized Power Dissipation vs. Case Temperature

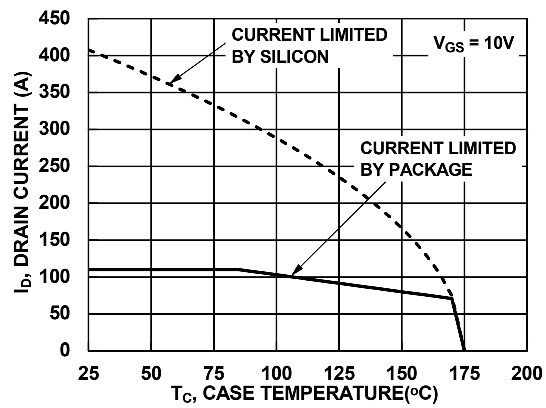


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

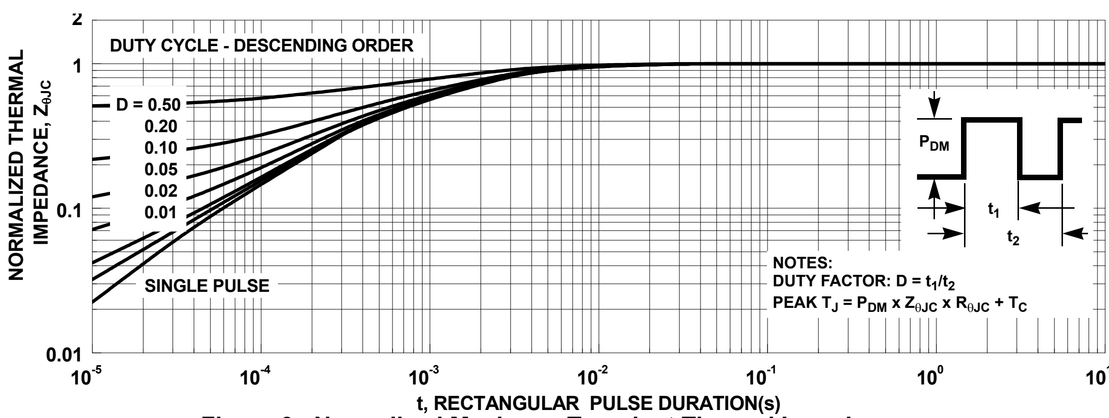


Figure 3. Normalized Maximum Transient Thermal Impedance

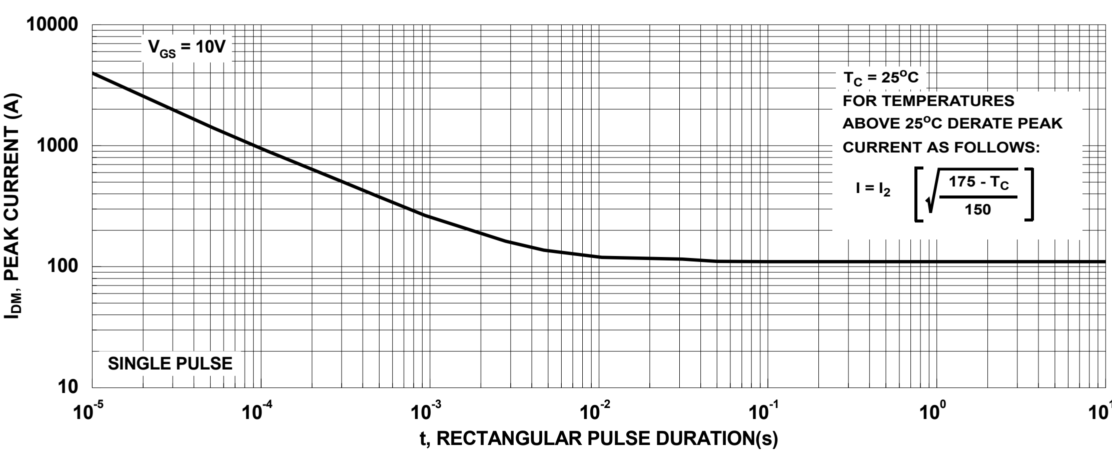


Figure 4. Peak Current Capability

Typical Characteristics

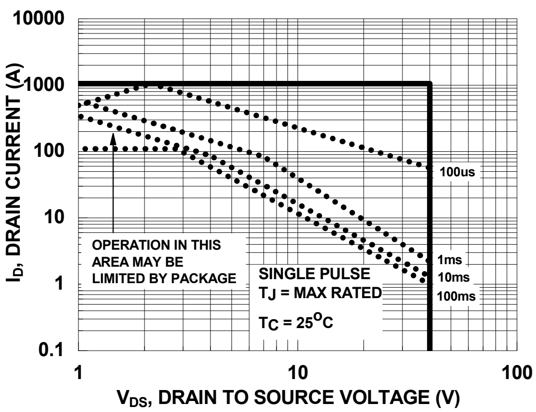
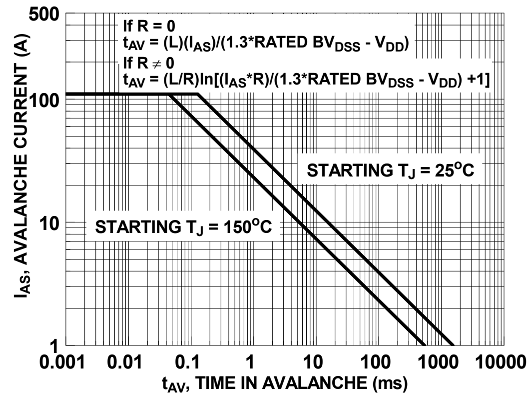


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

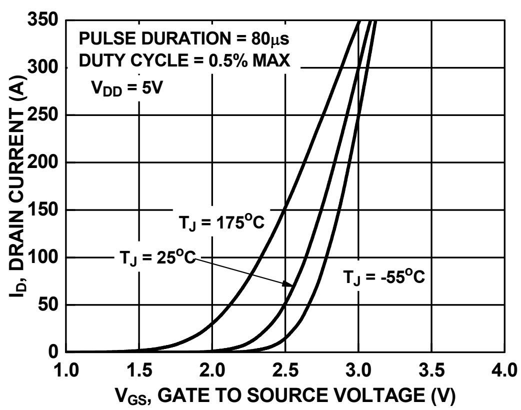


Figure 7. Transfer Characteristics

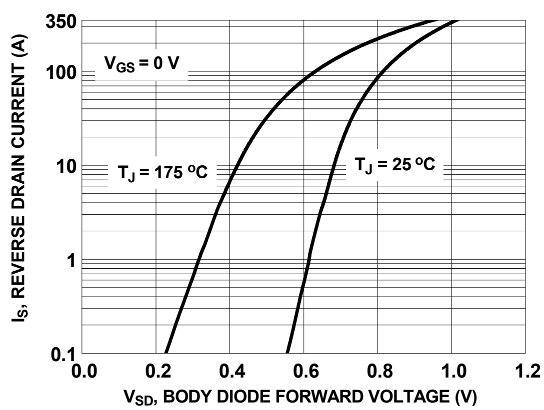


Figure 8. Forward Diode Characteristics

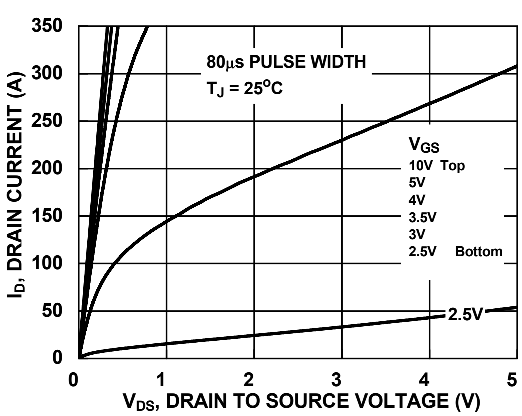


Figure 9. Saturation Characteristics

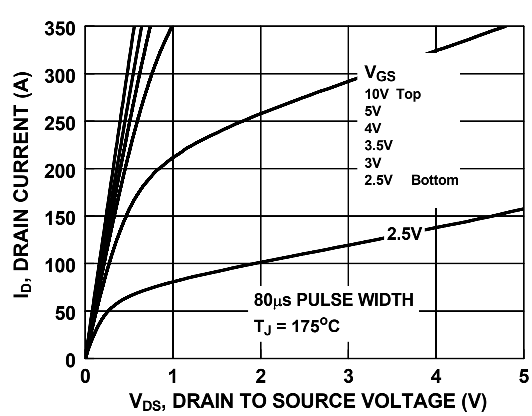


Figure 10. Saturation Characteristics

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Typical Characteristics

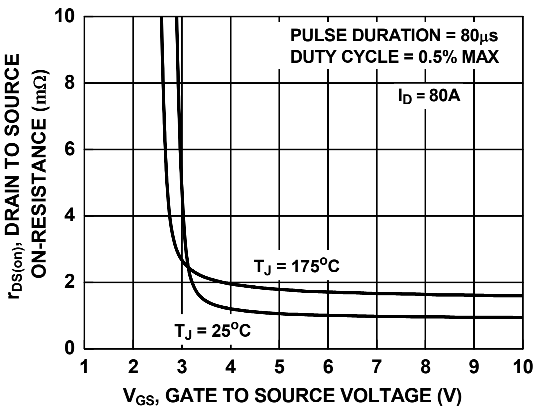


Figure 11. R_{DSON} vs. Gate Voltage

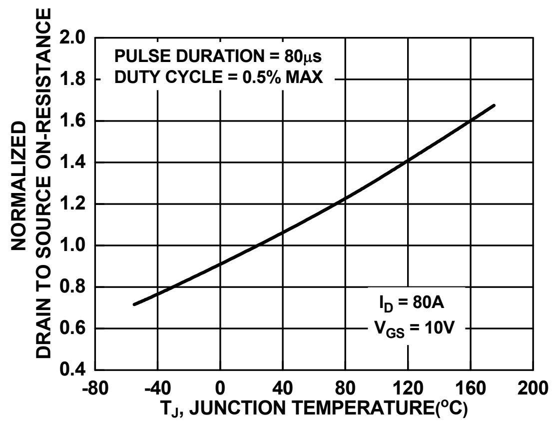


Figure 12. Normalized R_{DSON} vs. Junction Temperature

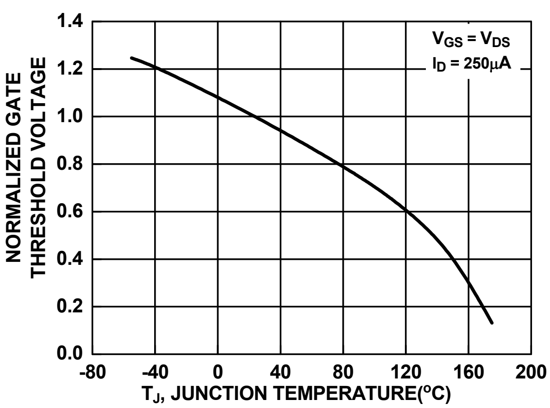


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

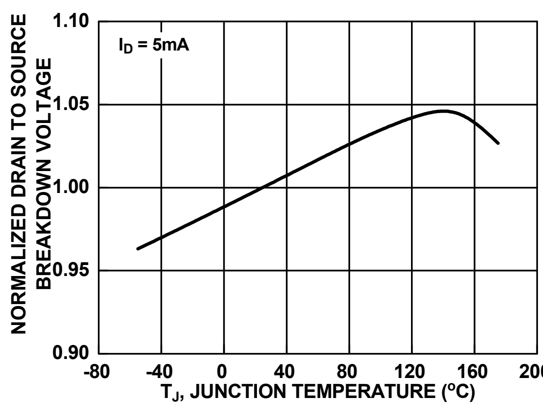


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

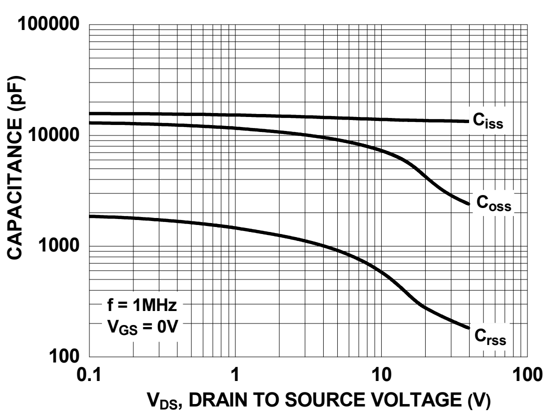


Figure 15. Capacitance vs. Drain to Source Voltage

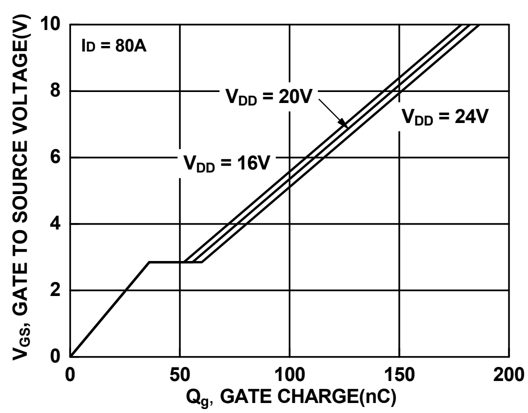
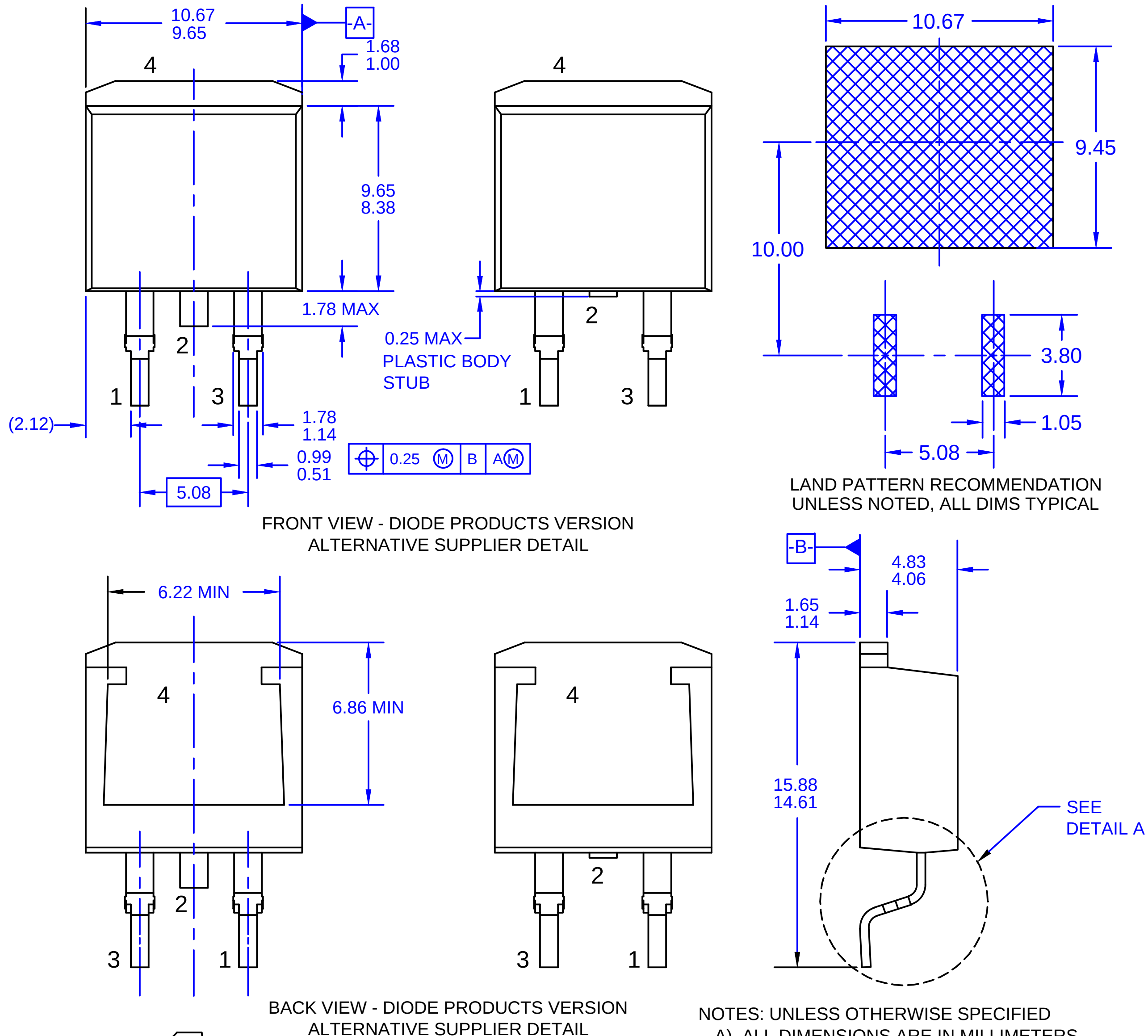
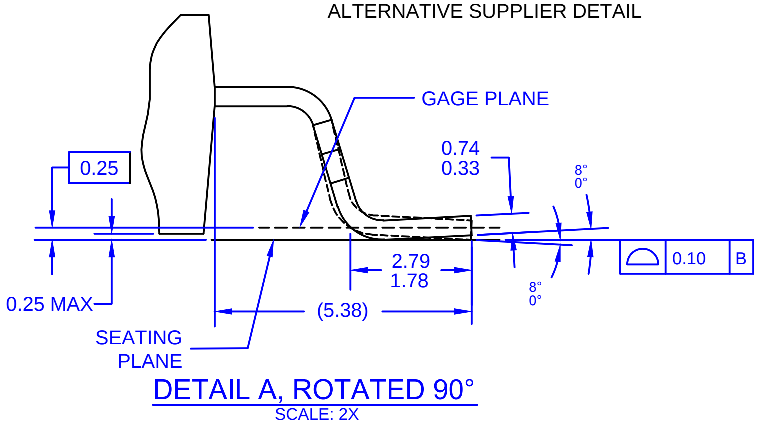


Figure 16. Gate Charge vs. Gate to Source Voltage





NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) REFERENCE JEDEC, TO-263, VARIATION AB.
C) DIMENSIONING AND TOLERANCING PER
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   ASME Y14.5 - 2009.
D) LOCATION OF THE PIN HOLE MAY VARY
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   AND CENTER OF THE PACKAGE).
E) LANDPATTERN RECOMMENDATION PER IPC
   TO254P1524X482-3N
F) FILENAME: TO263A02REV8

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