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**FDC655BN** Single N-Channel, Logic Level, PowerTrench<sup>®</sup> MOSFET 30 V, 6.3 A, 25 m $\Omega$ 

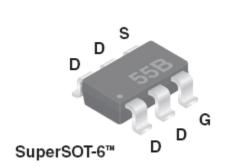
## Features

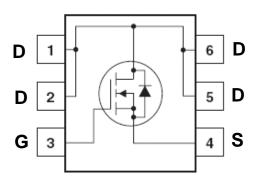
- Max  $r_{DS(on)} = 25 \text{ m}\Omega \text{ at } V_{GS} = 10 \text{ V}, I_D = 6.3 \text{ A}$
- Max  $r_{DS(on)}$  = 33 m $\Omega$  at V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 5.5 A
- Fast switching
- Low gate charge
- High performance trchnology for extremely low r<sub>DS(on)</sub>
- Termination is Lead-free and RoHS Compliant

## **General Description**

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.





## MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter			Ratings		Units	
V <sub>DS</sub>	Drain to Source Voltage			30		V	
V <sub>GS</sub>	Gate to Source Voltage			±20		V	
ID		-Continuous	$T_{A} = 25^{\circ}$	°C (Note 1a)	6.3		^
		-Pulsed			20		A
P <sub>D</sub>	Power Dis	ssipation		(Note 1a)	1.6		W
	Power Dis	ssipation		(Note 1b)	0.8		vv
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to + 150		°C	
Thermal Ch	naracteris	tics					
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient (Note 1a)			) 78		°C/W	
Package M	arking an	d Ordering Inform	nation				
Device Ma	arking	Device	Package	Reel Size	Tape Width	Qua	antity
.55B		FDC655BN	SSOT-6 <sup>™</sup>	7 "	8 mm	3000 units	

January 2010

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	icteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu A$ , referenced to $25^{\circ}C$		25		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 V, V_{GS} = 0 V$			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V			±100	nA
On Chara	cteristics					
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \ \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25°C		-5		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.3 A		21	25	mΩ
		$V_{GS} = 4.5 V, I_{D} = 5.5 A$		26	33	
		$V_{GS}$ = 10 V, I <sub>D</sub> = 6.3 A, T <sub>J</sub> = 125°C		30	36	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6.3 A		35		S
	Characteristics					_
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V,		470	620	pF
C <sub>oss</sub>	Output Capacitance	f = 1MHz		100	130	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			60	90	pF
	Gate Resistance			3.0		Ω
Rg						
	g Characteristics					
Switching	g Characteristics Turn-On Delay Time			6	11	ns
Switching t <sub>d(on)</sub>		V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1 A,		6 2	11 10	ns ns
<b>Switching</b> t <sub>d(on)</sub> t <sub>r</sub>	Turn-On Delay Time	$V_{DD}$ = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		-		
Switching t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		2	10	ns
Switching t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-On Delay Time Rise Time Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$		2 15	10 26	ns ns
Switching t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub> Q <sub>g</sub>	Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{GS} = 0 \text{ V to } 5 \text{ V}$ $V_{DD} = 15 \text{ V},$		2 15 2	10 26 10	ns ns ns
Rg           Switching           t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub> Q <sub>g</sub> Q <sub>g</sub> Q <sub>gs</sub>	Turn-On Delay Time         Rise Time         Turn-Off Delay Time         Fall Time         Total Gate Charge	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$		2 15 2 9	10 26 10 13	ns ns ns nC

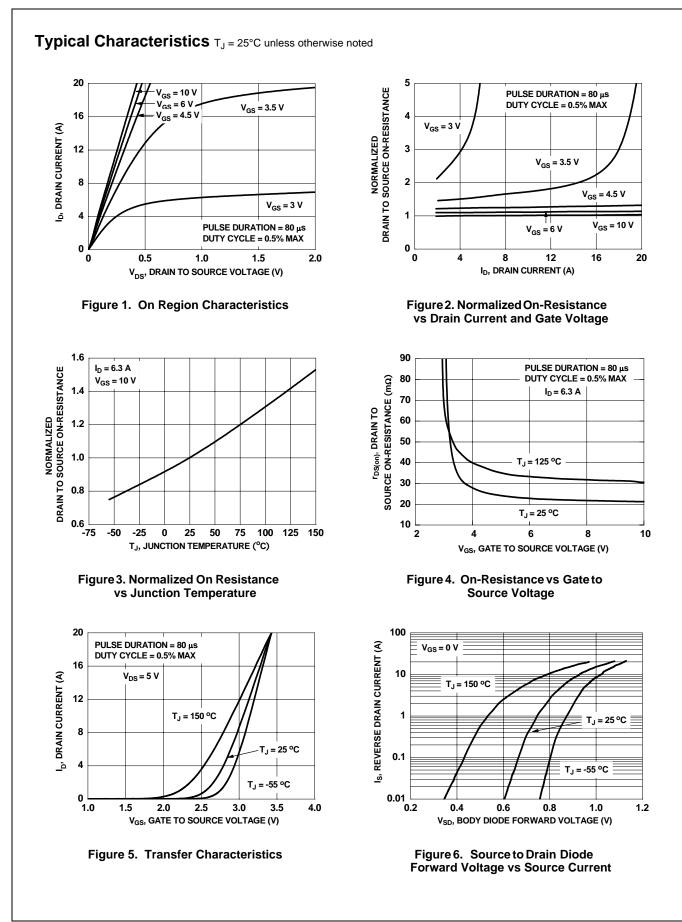
I <sub>S</sub>	Maximum Continuous Drain-Source Diod		1.3	Α	
V <sub>SD</sub>	Source-Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 1.3 A$ (Note 2)	0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 6.3 A, di/dt = 100 A/μs	15	26	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$= 1_{\rm F} = 0.5 \text{ A}, \text{ u/ut} = 100 \text{ A/}\mu\text{s}$	4	10	nC

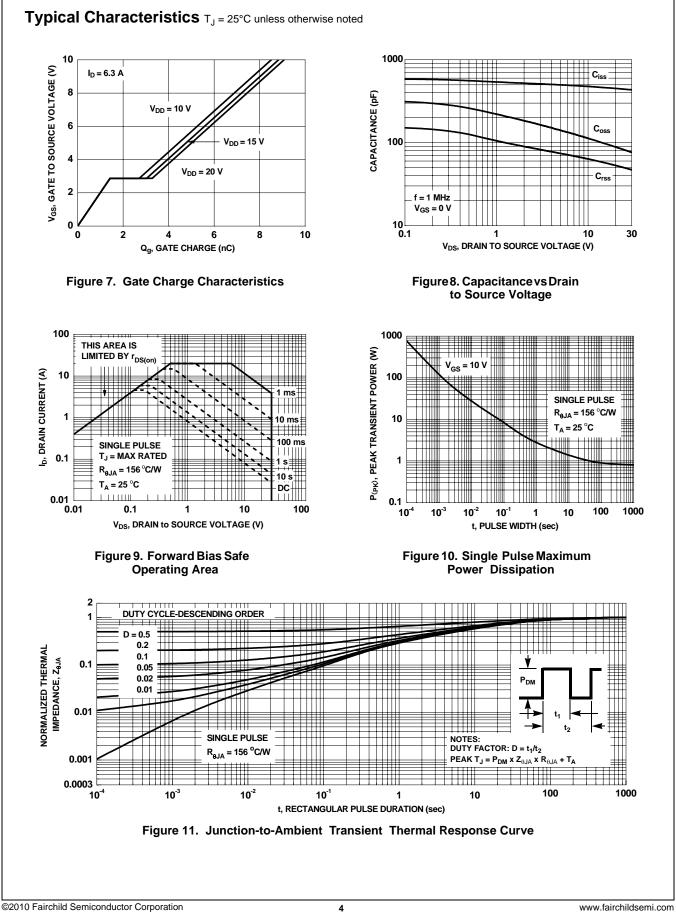
Notes:

 $R_{0,LA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{0,LC}$  is guaranteed by design while  $R_{0,CA}$  is determined by the user's board design.

a. 78 °C/W when mounted on a 1 in² pad of 2 oz copper on FR-4 board. b. 156 °C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width<300 us, Duty Cycle<2.0%.





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FDC655BN Rev. C2

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