## Product Description

KMX62 is a 6 Degrees-of-Freedom inertial sensor system that features 16-bit digital outputs accessed through $I^2C$ communication. The KMX62 sensor consists of a tri-axial magnetometer plus a tri-axial accelerometer coupled with an ASIC. It is packaged in a 3 x 3 x 0.9 mm Land Grid Array (LGA) package. The ASIC is realized in standard 0.18µm CMOS technology and features flexible user programmable ±2g / ±4g / ±8g / ±16g full scale range for the accelerometer and ±1200µT full scale range for the magnetometer. Accelerometer and Magnetometer data can be accumulated in an internal 384-byte FIFO buffer and transmitted to the application processor.
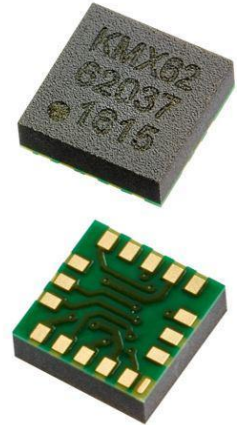
Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias, and sensitivity adjustments, as well as temperature compensation.

Magnetic sensing is based on the principle of magnetic impedance. The magnetic sensor detects very small magnetic fields by passing an electric pulse through a special electron spin aligned amorphous wire. Due to the high Curie temperature of the wire, the sensor's thermal performance shows excellent stability.

Noise performance is excellent with bias stability over temperature. Bias errors resulting from assembly can be trimmed digitally by the user. These sensors can accept supply voltages between 1.7V and 3.6V, and digital communication voltages between 1.2V and 3.6V.

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| | ± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications | PART NUMBER: KMX62-1031 Rev. 4.0 20-Dec-2017 |
|---|---|---|

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**PART NUMBER:**

**KMX62-1031**
**Rev. 4.0**
**20-Dec-2017**

± 1200uT Tri-axis Digital Magnetometer/
± 2g/4g/8g/16g Tri-axis Digital
Accelerometer Specifications

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## Functional Diagram

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## Product Specifications

Note: Specifications are for operation at VDD = 2.5V, T = 25ºC, High Resolution Mode (<RES> = 10, 11) unless stated otherwise.

## Mechanical

### Magnetometer

| Parameters | Units | Min | Typical | Max |
|---|---|---|---|---|
| Operating Temperature Range | ºC | -40 | - | +85 |
| Full Scale Range | $\mu$T | | ±1200 | |
| Digital Bit Depth | bits | | 16 | |
| Offset at Zero Magnetic Field | $\mu$T | | 0 | |
| Offset Temperature Coefficient | $\mu$T/ºC | | ±0.3 | |
| Magnetic Sensitivity | counts/$\mu$T | | 27.3 | |
| Sensitivity Accuracy | % | | ±20 | |
| Sensitivity Temperature Coefficient. | %/ºC | | ±0.05 | |
| Positive Self Test Output change on Activation | $\mu$T | | 800 | |
| Integral Non-Linearity | % of FS | | 0.5 | |
| Noise[1,2] | $\mu$T (RMS) | | 0.3 | |
| Cross Axis Sensitivity | % of FS | | 2 (XY)<br>0.5 (XZ)<br>0.3 (YX)<br>0.2 (YZ)<br>0.9 (ZX)<br>0.2 (ZY) | |
| Maximum Exposed Field[3] | $\mu$T | | | 500000 |

**Table 1:** Magnetometer Specifications

Notes:
1. Noise varies with Output Data Rate (ODR) as set by OSM<3:0> bits in ODCNTL and RES<1:0> bits in CNTL2 registers.
2. Measured at ODR = 50Hz, RES = 10, 11.
3. No permanent effect on Zero Magnetic Field Offset

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**Accelerometer**

| Parameters | | Units | Min | Typical | Max |
| --- | --- | --- | --- | --- | --- |
| Operating Temperature Range | | ºC | -40 | - | +85 |
| Full Scale Range | GSEL1=0, GSEL0=0 | g | | ±2 | |
| | GSEL1=0, GSEL0=1 | | | ±4 | |
| | GSEL1=1, GSEL0=0 | | | ±8 | |
| | GSEL1=1, GSEL0=1 | | | ±16 | |
| Digital Bit Depth | | | | 16 | |
| Zero-g Offset | | mg | | ±25 | ±90 |
| Zero-g Offset Temperature Coefficient | | mg/ºC | | ±0.25 | |
| Sensitivity | GSEL1=0, GSEL0=0 (±2g) | counts/g | | 16384 | |
| | GSEL1=0, GSEL0=1 (±4g) | | | 8192 | |
| | GSEL1=1, GSEL0=0 (±8g) | | | 4096 | |
| | GSEL1=1, GSEL0=1 (±16g) | | | 2048 | |
| Sensitivity Accuracy | | % | | ±5 | |
| Sensitivity Temperature Coefficient | | %/ºC | | ±0.01 | |
| Positive Self Test Output change on Activation | | g | 0.25 (xy) 0.2 (z) | 0.5 | 0.75 |
| Signal Bandwidth (-3dB) | | Hz | | 3500 (xy) 1800 (z) | |
| Integral Non-Linearity | | % of FS | | 1 | |
| Cross Axis Sensitivity[1] | | % | | -2 (XY) 0.1 (XZ) 2.7 (YX) -0.7 (YZ) -0.8 (ZX) 1.4 (ZY) | |
| Noise[2,3] | RMS | mg | | 0.75 | |
| | Density | µg/√Hz | | 130 | |

**Table 2**: Accelerometer Specifications

Notes:
1. As measured in a test socket at the factory. The cross-axis sensitivity that is measured is the by-product of positional inaccuracies at all stages of test and assembly.
2. Noise varies with Output Data Rate (ODR) as set by OSA<3:0> bits in ODCNTL, and RES<1:0> bits in CNTL2 registers.
3. Measured at ODR = 50Hz, RES = 10, 11.

## Temperature Sensor

(specifications are for operation at VDD = 2.5V and T = 25ºC unless stated otherwise)

| Parameters | Units | Min | Typical | Max |
|---|---|---|---|---|
| Operating Temperature Range | ºC | -40 | - | +85 |
| Output Accuracy | ± ºC | | 5 | |
| Sensitivity (16-bit digital) | counts/ºC | | 256 | |
| Sensitivity (8-bit digital, TEMP<15:8>) | counts/ºC | | 1 | |

**Table 3:** Temperature Sensor Mechanical Specifications

## Electrical

| Parameters | | Units | Min | Typical | Max |
|---|---|---|---|---|---|
| Supply Voltage (VDD) | Operating | V | 1.7 | 2.5 | 3.6 |
| I/O Pads Supply Voltage (IO_VDD) | | V | 1.2 | | 3.6 |
| Current Consumption[1]<br>(High Resolution Mode)<br>(<RES> = 10 or 11) | Operating (mag + accel) | µA | | 395 | |
| | Magnetometer only | | | 295 | |
| | Accelerometer only | | | 150 | |
| | Standby | | | 1 | 5 |
| Output Low Voltage[2] (IO_VDD < 2V) | | V | - | - | 0.2 * IO_VDD |
| Output Low Voltage[2] (IO_VDD ≥ 2V) | | V | - | - | 0.4 |
| Output High Voltage | | V | 0.9 * IO_VDD | - | - |
| Input Low Voltage | | V | - | - | 0.3 * IO_VDD |
| Input High Voltage | | V | 0.7 * IO_VDD | - | - |
| I²C Communication Rate[3,4] | | kHz | 100 | 400 | 3400 |
| I²C Slave Address (7-bit) | | | | 0x0E  / 0x0F | |
| Output Data Rate (ODR) | | Hz | 0.781 | 100 | 1600 |
| Bandwidth (-3dB)[5] | RES 00,01 | Hz | | 400 | |
| | RES 10,11 | Hz | | ODR/2 | |
| Internal Oscillator Tolerance | | % | -10 | | 10 |
| Start Up Time[6] | | ms | 1 | | 1300 |

**Table 4:** Electrical Specifications

Notes:
1. See Figure 2 for other modes (RES = 00 or 01)
2. Assuming I²C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA
3. Assuming max bus capacitance load of 20pF
4. The I²C bus supports Standard-Mode, Fast-Mode, and High-Speed Mode.
5. User selectable via ODR control register setting
6. Start up time is from ACCEL_EN / MAG_EN set to valid outputs. Time varies with Output Data Rate (ODR) and mode setting (RES) (see Figure 1).

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**Start Up Time Profile**

Typical Start Up Time over selected ODR (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz)
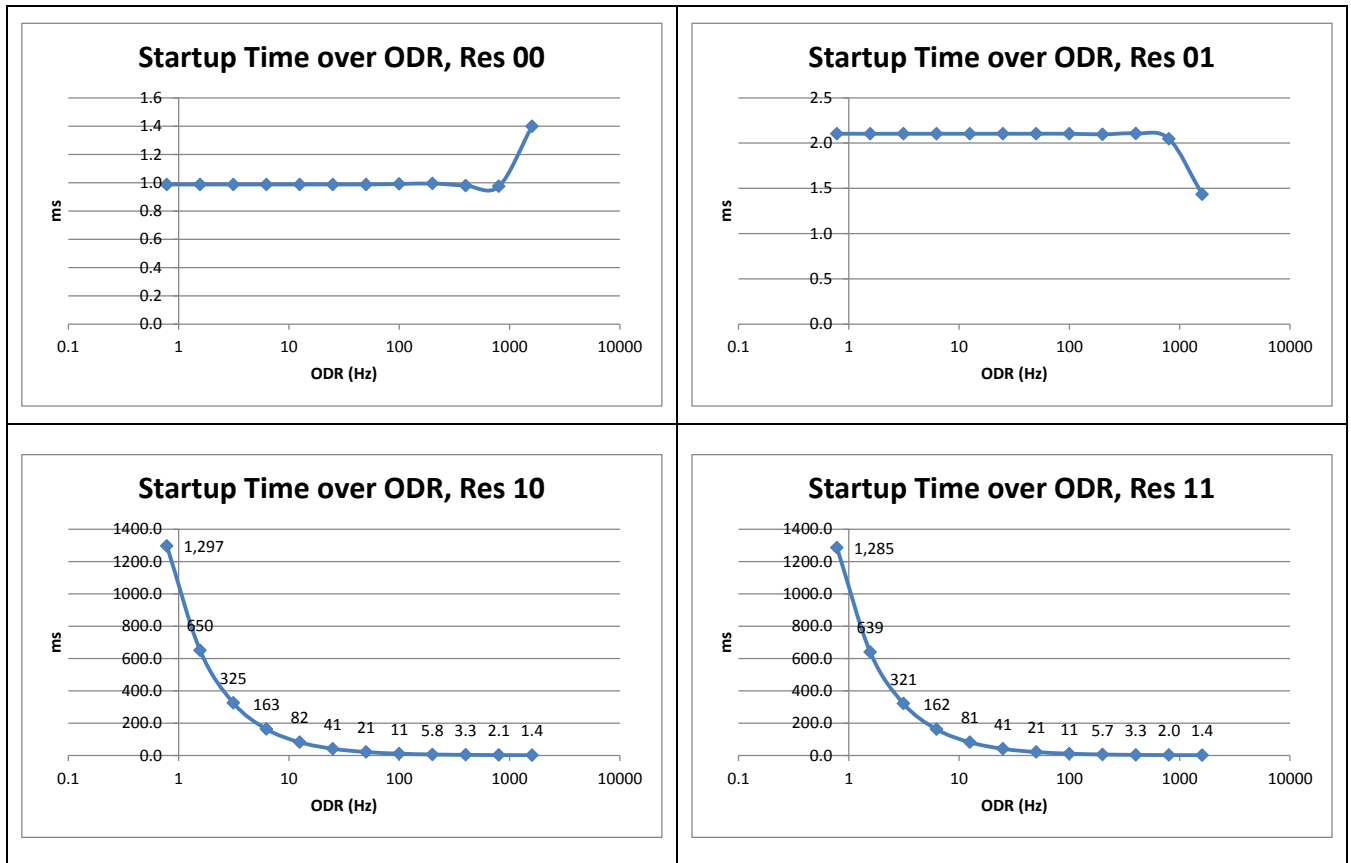


**Figure 1:** Start Up Time Diagram

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**Current Profile**

Typical current over selected ODR (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz) @ VDD = 2.5V and T = 25ºC
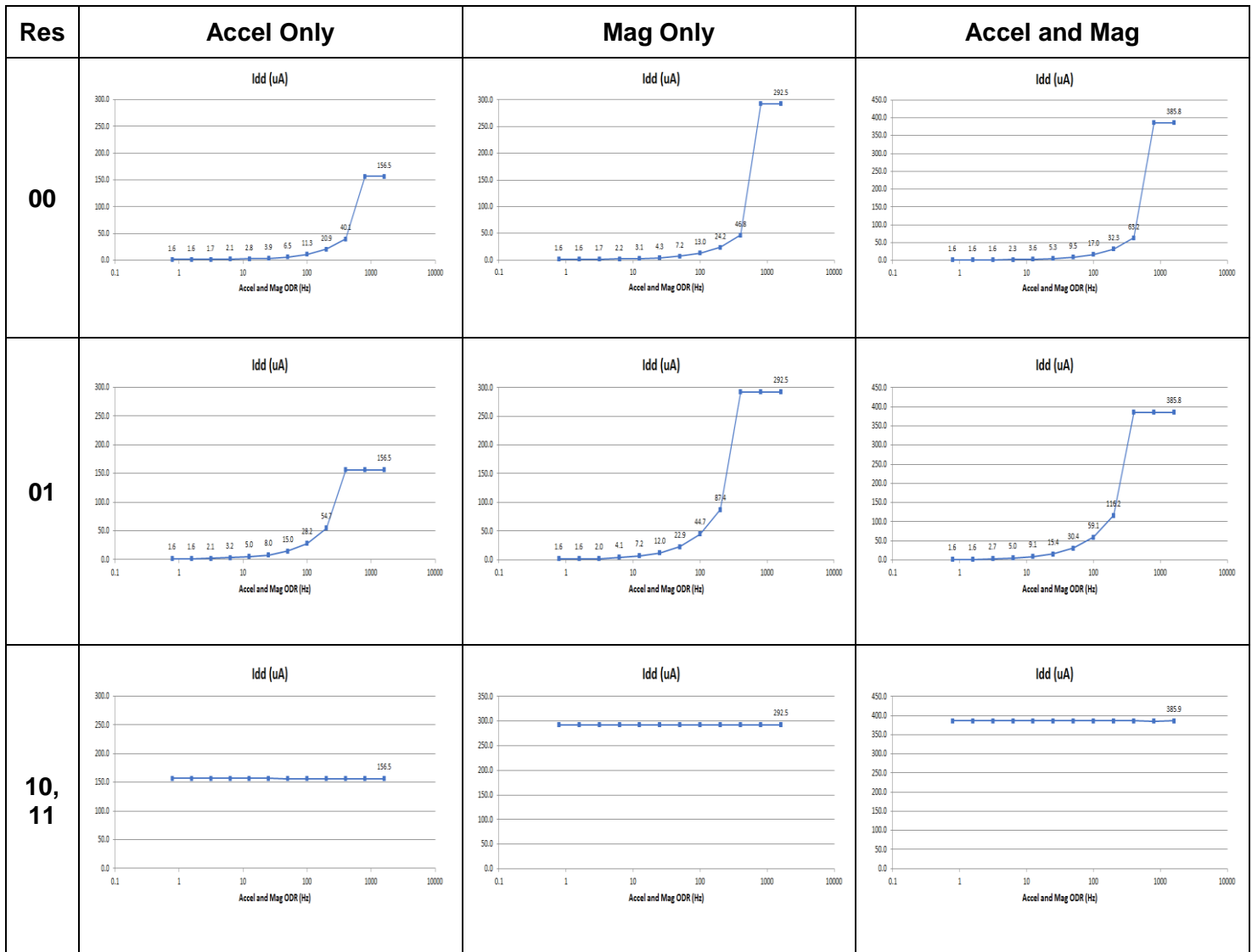


**Figure 2:** Current Consumption Diagram

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| | ± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications | PART NUMBER: KMX62-1031 Rev. 4.0 20-Dec-2017 |
|---|---|---|

## Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD$_{LOW}$, T$_{VDD}$** (rise time), and **T$_{VDD\_OFF}$** profile of individual applications. It is recommended to minimize **VDD$_{LOW}$**, and **T$_{VDD}$**, and maximize **T$_{VDD\_OFF}$**. It is also advised that the VDD ramp up time **T$_{VDD}$** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

**!** *To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD$_{LOW}$, T$_{VDD}$, T$_{VDD\_OFF}$ and temperature as POR performance can vary depending on these parameters.*

Please refer to Technical Note ***TN005 Power-On Procedure*** for more information.

## Environmental

| Parameters | | Units | Min | Typical | Max |
|---|---|---|---|---|---|
| Supply Voltage (VDD) | Absolute Limits | V | -0.3 | - | 3.6 |
| Operating Temperature Range | | °C | -40 | - | 85 |
| Storage Temperature Range | | °C | -55 | - | 150 |
| Mech. Shock (powered and unpowered) | | g | - | - | 5000 for 0.5ms<br>10000 for 0.2ms |
| ESD | HBM | V | - | - | 2000 |

**Table 5:** Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout". The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: *7C-I - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectric devices) or in a glass or ceramic matrix compound.*

These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-174) as identified by the European Chemicals Agency as of 12 July 2017.

HF This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

## Soldering

Soldering recommendations are available upon request or from www.kionix.com.

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## Application Schematic and Pin Description

### Application Schematic
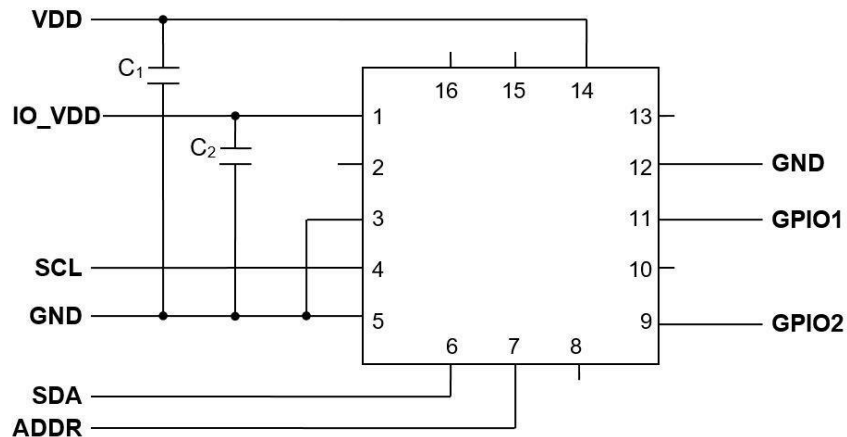


### Pin Description

| Pin | Name | Description |
|-----|------|-------------|
| 1 | IO_VDD | The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor. |
| 2 | CAP | Do not connect. Must be left floating. |
| 3 | GND | Ground |
| 4 | SCL | I2C Serial Clock |
| 5 | GND | Ground |
| 6 | SDA | I2C Serial Data |
| 7 | ADDR | I2C Address pin. This pin must be connected to IO_VDD or GND to determine the I2C Device Address. |
| 8 | NC | Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating. |
| 9 | GPIO2 | GPIO 2. Cannot float when configured as an input. |
| 10 | NC | Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating. |
| 11 | GPIO1 | GPIO 1. Cannot float when configured as an input. |
| 12 | GND | Ground |
| 13 | NC | Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating. |
| 14 | VDD | The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor. |
| 15 | NC | Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating. |
| 16 | NC | Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating. |

**Table 6:** Pin Description

Note: Pins 3, 5, and 12 (GND) are internally tied together.

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## Package Dimensions and Orientation

### Dimensions

3 x 3 x 0.9 mm LGA
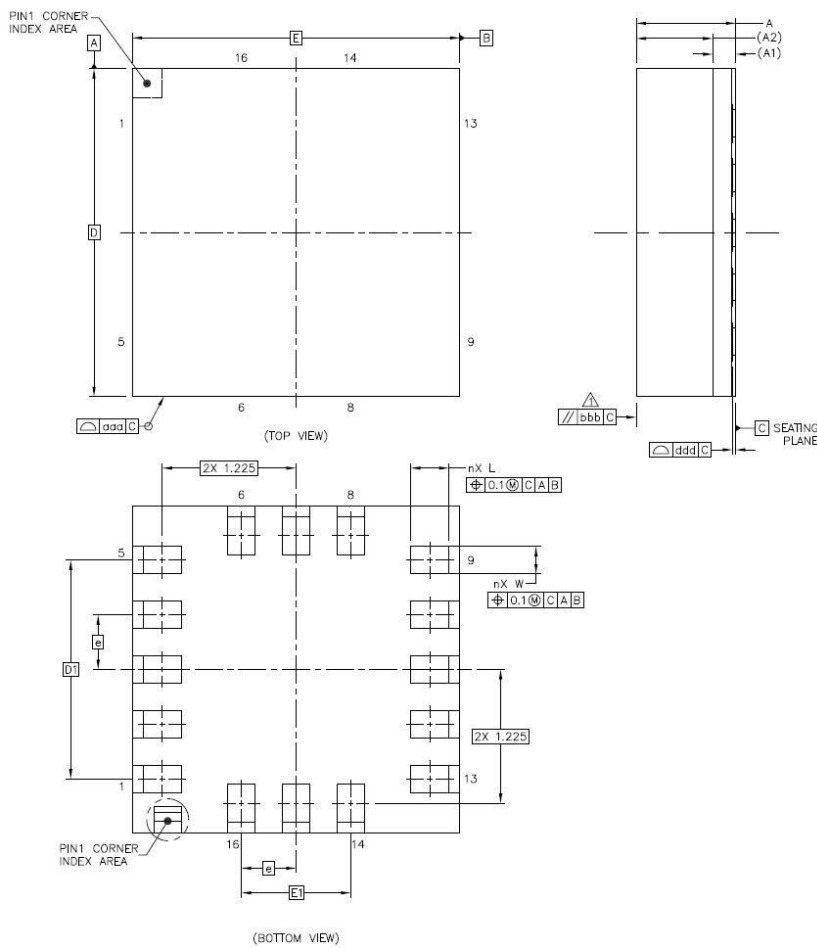


| | SYMBOL | COMMON DIMENSIONS | | |
|---|---|---|---|---|
| | | MIN. | NOR. | MAX. |
| TOTAL THICKNESS | A | ---- | ---- | 1 |
| SUBSTRATE THICKNESS | A1 | | 0.21 | REF |
| MOLD THICKNESS | A2 | | 0.7 | REF |
| BODY SIZE | D | | 3 | BSC |
| | E | | 3 | BSC |
| LEAD WIDTH | W | 0.2 | 0.25 | 0.3 |
| LEAD LENGTH | L | 0.3 | 0.35 | 0.4 |
| LEAD PITCH | e | | 0.5 | BSC |
| LEAD COUNT | n | | 16 | |
| EDGE BALL CENTER TO CENTER | D1 | | 2 | BSC |
| | E1 | | 1 | BSC |
| BODY CENTER TO CONTACT BALL | SD | | --- | BSC |
| | SE | | --- | BSC |
| BALL WIDTH | b | --- | --- | --- |
| BALL DIAMETER | | | --- | |
| BALL OPENING | | | --- | |
| BALL PICTH | e1 | | --- | |
| BALL COUNT | n1 | | --- | |
| PRE-SOLDER | | --- | --- | --- |
| PACKAGE EDGE TOLERANCE | aaa | | 0.1 | |
| MOLD FLATNESS | bbb | | 0.2 | |
| COPLANARITY | ddd | | 0.08 | |
| BALL OFFSET (PACKAGE) | eee | | --- | |
| BALL OFFSET (BALL) | fff | | --- | |
| | | | | |
| | | | | |

NOTES:

⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

All dimensions and tolerances conform to ASME Y14.5M-1994

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**Orientation**

When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase. When the +X, +Y, or +Z arrow is directed toward North, the output of that axis is positive.
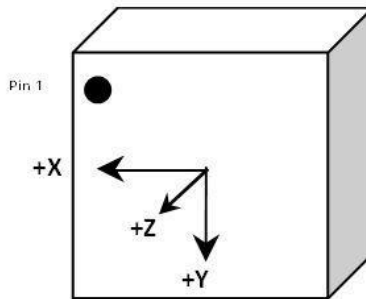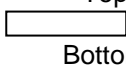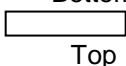


**Figure 3:** Accelerometer and Magnetometer Orientation

Please avoid mounting this product on the part in which magnetic field disturbance exists, such as near any parts containing ferrous materials.

**Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):**
GSEL1=0, GSEL0=0 (±2g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Diagram | | | | | Top / Bottom | Bottom / Top |
| Resolution (bits) | 16 | 16 | 16 | 16 | 16 | 16 |
| X (counts) | 0 | -16384 | 0 | +16384 | 0 | 0 |
| Y (counts) | -16384 | 0 | +16384 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | +16384 | -16384 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

(1g)

Earth's Surface

### Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):
GSEL1=0, GSEL0=1 (±4g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Diagram | | | | | Top / Bottom | Bottom / Top |
| Resolution (bits) | 16 | 16 | 16 | 16 | 16 | 16 |
| X (counts) | 0 | -8192 | 0 | +8192 | 0 | 0 |
| Y (counts) | -8192 | 0 | +8192 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | +8192 | -8192 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

↓(1g)

Earth's Surface

### Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):
GSEL1=1, GSEL0=0 (±8g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Diagram | | | | | Top / Bottom | Bottom / Top |
| Resolution (bits) | 16 | 16 | 16 | 16 | 16 | 16 |
| X (counts) | 0 | -4096 | 0 | +4096 | 0 | 0 |
| Y (counts) | -4096 | 0 | +4096 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | +4096 | -4096 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

↓(1g)

Earth's Surface

| | | PART NUMBER: |
|---|---|---|
| Kīonix® | ± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications | KMX62-1031 Rev. 4.0 20-Dec-2017 |

**Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):**
GSEL1=0, GSEL0=1 (±16g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Diagram | | | | | Top / Bottom | Bottom / Top |
| Resolution (bits) | 16 | 16 | 16 | 16 | 16 | 16 |
| X (counts) | 0 | -2048 | 0 | +2048 | 0 | 0 |
| Y (counts) | -2048 | 0 | +2048 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | +2048 | -2048 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

↓(1g)

Earth's Surface

## Digital Interface

The Kionix KMX62 digital sensor can communicate on the I$^2$C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system processors. The I$^2$C interface is compliant with high-speed mode, fast mode, and standard mode I$^2$C protocols.

The serial interface terms and descriptions as indicated in Table 7 below will be observed throughout this document.

| Term | Description |
| --- | --- |
| Transmitter | The device that transmits data to the bus. |
| Receiver | The device that receives data from the bus. |
| Master | The device that initiates a transfer, generates clock signals, and terminates a transfer. |
| Slave | The device addressed by the Master. |

**Table 7**: Serial Interface Terminologies

### I$^2$C Serial Interface

As previously mentioned, the KMX62 can communicate on an I$^2$C bus. I$^2$C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The system Master provides the serial clock signal and addresses Slave devices on the bus. The KMX62 always operates as a Slave device during standard Master-Slave I$^2$C operation.

I$^2$C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held LOW by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I$^2$C bus is considered free when both lines are HIGH.

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### I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KMX62 Slave Address is comprised of a user programmable part, a factory programmable part, and a fixed part, which allows for connection of multiple sensors to the same I²C bus. The Slave Address associated with the KMX62 is 00011YX, where the user programmable bit X, is determined by the assignment of ADDR (pin 7) to GND or IO_VDD. Also, the factory programmable bit Y is set at the factory. **For KMX62-1031, the factory programmable bit Y is fixed to 1** (contact your Kionix sales representative for list of available devices). Table 8 lists possible I²C addresses for KMX62-1031. It is possible to have up to four sensors on a shared I²C bus as shown in Figure 4 (i.e. two KMX62-1031 accelerometer/magnetometer and two additional accelerometer/magnetometer with the factory programmable bit Y set to **0**).

| | | | | | | | | | **Y** | **X** | |
| Description | Address Pad | 7-bit Address | Address | <7> | <6> | <5> | <4> | <3> | <2> | <1> | <0> |
|---|---|---|---|---|---|---|---|---|---|---|---|
| I2C Wr | GND | 0x0E | 0x1C | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| I2C Rd | GND | 0x0E | 0x1D | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| I2C Wr | IO_VDD | 0x0F | 0x1E | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| I2C Rd | IO_VDD | 0x0F | 0x1F | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**Table 8:** I²C Address

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line LOW so that it remains stable LOW during the HIGH period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from LOW to HIGH while SCL is HIGH. The I²C bus is now free. Note that if the KMX62 is accessed through I²C protocol before the startup is finished a NACK signal is sent.

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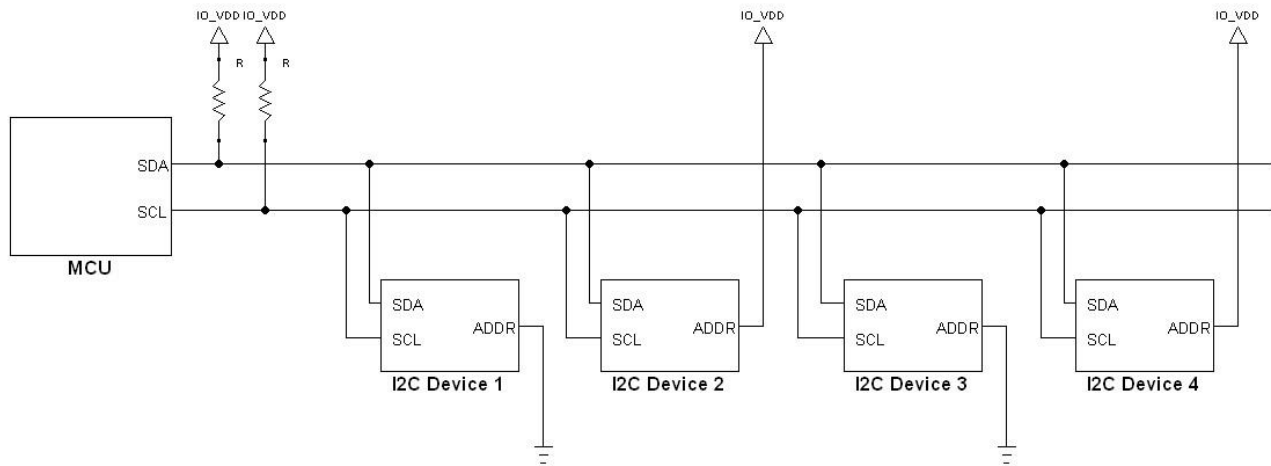
| I2C Device | Part Number | ADDR Pin | Slave Address | Bit Y (Bit 1 in 7-bit address) |
|---|---|---|---|---|
| 1 | KMX62-1031 | GND | 0x0E | Factory Set to 1 |
| 2 | KMX62-1031 | IO_VDD | 0x0F | Factory Set to 1 |
| 3 | *KXMMM | GND | 0x0C | Factory Set to 0 |
| 4 | *KXMMM | IO_VDD | 0x0D | Factory Set to 0 |

* KXMMM – contact Kionix sales representative for list of compatible devices

**Figure 4:** Multiple KMX62 I²C Connection

### Writing to an 8-bit Register

Upon power up, the Master must write to the KMX62's control registers to set its operational mode. Therefore, when writing to a control register on the I²C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KMX62 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KMX62 to which 8-bit register the Master will be writing the data. Since this is I²C mode, the MSB of the RA command should always be zero (0). The KMX62 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KMX62 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KMX62 is now stored in the appropriate register. The KMX62 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

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### Reading from an 8-bit Register

When reading data from a KMX62 8-bit register on the I$^2$C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KMX62 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KMX62 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KMX62 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. The KMX62 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.

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### Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I$^2$C bus and how the Master and Slave interact during these transfers. Table 9 defines the I$^2$C terms used during the data transfers.

| Term | Definition |
|------|------------|
| S | Start Condition |
| Sr | Repeated Start Condition |
| SAD | Slave Address |
| W | Write Bit |
| R | Read Bit |
| ACK | Acknowledge |
| NACK | Not Acknowledge |
| RA | Register Address |
| Data | Transmitted/Received Data |
| P | Stop Condition |

**Table 9:** I$^2$C Terms

**Sequence 1:** The Master is writing one byte to the Slave.

| Master | S | SAD + W | | RA | | DATA | | P |
|--------|---|---------|-----|----|-----|------|-----|---|
| Slave | | | ACK | | ACK | | ACK | |

**Sequence 2:** The Master is writing multiple bytes to the Slave.

| Master | S | SAD + W | | RA | | DATA | | DATA | | P |
|--------|---|---------|-----|----|-----|------|-----|------|-----|---|
| Slave | | | ACK | | ACK | | ACK | | ACK | |

**Sequence 3:** The Master is receiving one byte of data from the Slave.

| Master | S | SAD + W | | RA | | Sr | SAD + R | | | NACK | P |
|--------|---|---------|-----|----|-----|----|---------|-----|------|------|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | |

**Sequence 4:** The Master is receiving multiple bytes of data from the Slave.

| Master | S | SAD + W | | RA | | Sr | SAD + R | | | ACK | | NACK | P |
|--------|---|---------|-----|----|-----|----|---------|-----|------|-----|------|------|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | DATA | | |

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### HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: A Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

**Sequence 5:** HS-mode data transfer of the Master writing one byte to the Slave.

| Speed | FS-mode | | | HS-mode | | | | | | | | FS-mode |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Master | S | M-code | NACK | S | SAD + W | | RA | | DATA | | P | |
| Slave | | | | | | ACK | | ACK | | ACK | | |

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**± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications**

## I²C Timing Diagram
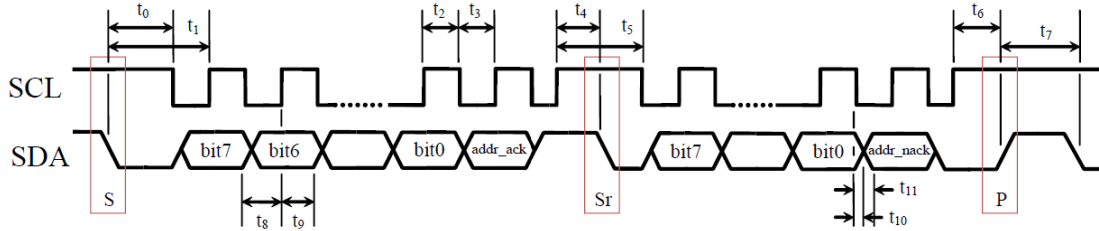


| Number | Description | MIN | MAX | Units |
|--------|-------------|-----|-----|-------|
| $t_0$ | SDA LOW to SCL LOW transition (Start event) | 50 | - | ns |
| $t_1$ | SDA LOW to first SCL rising edge | 100 | - | ns |
| $t_2$ | SCL pulse width: HIGH | 100 | - | ns |
| $t_3$ | SCL pulse width: LOW | 100 | - | ns |
| $t_4$ | SCL HIGH before SDA falling edge (Start Repeated) | 50 | - | ns |
| $t_5$ | SCL pulse width: HIGH during a S/Sr/P event | 100 | - | ns |
| $t_6$ | SCL HIGH before SDA rising edge (Stop) | 50 | - | ns |
| $t_7$ | SDA pulse width: HIGH | 25 | - | ns |
| $t_8$ | SDA valid to SCL rising edge | 50 | - | ns |
| $t_9$ | SCL rising edge to SDA invalid | 50 | - | ns |
| $t_{10}$ | SCL falling edge to SDA valid (when slave is transmitting) | - | 100 | ns |
| $t_{11}$ | SCL falling edge to SDA invalid (when slave is transmitting) | 0 | - | ns |
| Note | Recommended I²C CLK | 2.5 | - | µs |

**Table 10:** I²C Timing (Fast Mode)

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## Power Modes

The KMX62 has five power modes: Off, Stand-by, Sleep, Low Power (RES = 00, 01) and High Resolution (RES = 10, 11). The part exists in one of these five modes at any given time. Off and Stand-by modes have very low current consumptions.

| Power Mode | Bus State | IO_VDD | VDD | Function | Outputs |
| --- | --- | --- | --- | --- | --- |
| Off | - | OFF | OFF | No sensor activity | Not available |
| | | ON | OFF | | |
| | | OFF | ON | | |
| Stand-by | Active | ON | ON | Waiting activation command | Not available |
| Sleep | Active | ON | ON | Accelerometer active looking for motion wake up | Accel registers only – no buffer, no DRDY interrupt |
| <RES> = 00 or 01 | Active | ON | ON | All functionalities available | All sensors available |
| <RES> = 10 or 11 | Active | ON | ON | All functionalities available | All sensors available |

### Off mode

One or both power supplies (VDD or IO_VDD) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

### Initial Startup

The preferred startup sequence is to turn on IO_VDD before VDD, but if VDD is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. IO_VDD supply is valid
2. VDD power supply is going to valid level
   **OR**
1. IO_VDD power supply is going to valid level
2. VDD supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

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### Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command from the external application processor via the I$^2$C bus.

### Sleep mode

While in sleep mode, the accelerometer is periodically taking a measurement to detect if there is any motion. Data in the accelerometer registers is being updated, however, there is no data ready interrupt being reported. Also, no data is being sent to the buffer.

### Low Power (<RES> = 00 or 01) mode

Stand-by-mode can be changed to a Low Power mode by writing to register Control Register 2 or when a motion wake up event occurs.

Low power mode engages the full functionality of accelerometer and/or magnetometer measurements in a low power, low resolution mode (see *Table 15: Selected resolution range* for details). The host can change settings in the control register back to Stand-by mode for either or both the accelerometer and magnetometer. If enabled, the back to sleep function will put the part into the Sleep mode.

The host can also place the part into High Resolution (<RES> = 10 or 11) mode by writing to Control Register 2.

### High Resolution (<RES> = 10 or 11) mode

Stand-by-mode can be changed to High Resolution mode by writing to register Control Register 2.

High Resolution mode engages the full functionality of accelerometer and/or magnetometer measurements in a higher power, higher resolution mode (see *Table 15: Selected resolution range* for details). The host can change settings in the control register back to Stand-by mode for either or both the accelerometer and magnetometer. If enabled, the back to sleep function will put the part into the Sleep mode.

The host can also place the part into Low Power (<RES> = 00 or 01) mode by writing to Control Register 2.

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## Embedded Registers

The KMX62 has 45 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and describes bit functions of each register. Table 11 below provides a listing of the accessible 8-bit registers and their addresses.

| Register Name | I²C Address (Hex) | Type R/W | Register Name | I²C Address (Hex) | Type R/W |
|---|---|---|---|---|---|
| WHO_AM_I | 00h | R | AMI_CNTL1 | 2Fh | R/W |
| INS1 | 01h | R | AMI_CNTL2 | 30h | R/W |
| INS2 | 02h | R | AMI_CNTL3 | 31h | R/W |
| INS3 | 03h | R | MMI_CNTL1 | 32h | R/W |
| INL | 05h | R | MMI_CNTL2 | 33h | R/W |
| ACCEL_XOUT_L | 0Ah | R | MMI_CNTL3 | 34h | R/W |
| ACCEL_XOUT_H | 0Bh | R | FFI_CNTL1 | 35h | R/W |
| ACCEL_YOUT_L | 0Ch | R | FFI_CNTL2 | 36h | R/W |
| ACCEL_YOUT_H | 0Dh | R | FFI_CNTL3 | 37h | R/W |
| ACCEL_ZOUT_L | 0Eh | R | ODCNTL | 38h | R/W |
| ACCEL_ZOUT_H | 0Fh | R | CNTL1 | 39h | R/W |
| MAG_XOUT_L | 10h | R | CNTL2 | 3Ah | R/W |
| MAG_XOUT_H | 11h | R | COTR | 3Ch | R |
| MAG_YOUT_L | 12h | R | BUF_CTRL_1 | 77h | R/W |
| MAG_YOUT_H | 13h | R | BUF_CTRL_2 | 78h | R/W |
| MAG_ZOUT_L | 14h | R | BUF_CTRL_3 | 79h | R/W |
| MAG_ZOUT_H | 15h | R | BUF_CLEAR | 7Ah | W |
| TEMP_OUT_L | 16h | R | BUF_STATUS_1 | 7Bh | R |
| TEMP_OUT_H | 17h | R | BUF_STATUS_2 | 7Ch | R |
| INC1 | 2Ah | R/W | BUF_STATUS_3 | 7Dh | R |
| INC2 | 2Bh | R/W | BUF_READ | 7Eh | R |
| INC3 | 2Ch | R/W | | | |
| INC4 | 2Dh | R/W | | | |
| INC5 | 2Eh | R/W | | | |

**Table 11:** I²C Register Map

## Register Descriptions

### WHO_AM_I

This register is used for supplier recognition, as it is factory written to a known byte value. The default value is 0x18.

| R | R | R | R | R | R | R | R | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WAI_MIR7 | WAI_MIR6 | WAI_MIR5 | WAI_MIR4 | WAI_MIR3 | WAI_MIR2 | WAI_MIR1 | WAI_MIR0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00011000 |
| | | | | | Address: 0x00 | | | |

### INS1 - Interrupt Source Register 1

This register tells which function caused an interrupt.

| R | R | R | R | R | R | R | R | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INT | BFI | WMI | DRDY_A | DRDY_M | FFI | AMI | MMI | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x01 | | | |

*INT* reports the combined (OR) interrupt information of all enabled interrupt.
0= no interrupt event, 1= interrupt event has occurred.

*BFI* - indicates that the buffer is full. This bit is cleared when the data is read until the buffer is not full.
BFI = 0 – Buffer is not full
BFI = 1 – Buffer is full

*WMI* - indicates that user-defined buffer watermark has been reached. This bit is cleared when the data is read until the sample level in the buffer is smaller than the watermark threshold.
WMI = 0 – Buffer watermark not reached
WMI = 1 – Buffer watermark reached

*DRDY_A* - indicates that new acceleration data is available. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.
DRDY_A = 0 – New acceleration data not available
DRDY_A = 1 – New acceleration data available

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**DRDY_M** - indicates that new magnetometer data is available. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.
  DRDY_M = 0 – New magnetometer data not available
  DRDY_M = 1 – New magnetometer data available

**FFI** – Free fall, this bit is cleared when the interrupt source latch register (INL Register) is read.
  FFI = 1 – Free fall has activated the interrupt
  FFI = 0 – No free fall

**AMI** – Accelerometer motion interrupt. This bit is cleared when the interrupt source latch register (INL) is read.
  AMI = 1 – Accelerometer motion has activated the interrupt
  AMI = 0 – No motion

**MMI** – Magnetometer motion interrupt. This bit is cleared when the interrupt source latch register (INL Register) is read.
  MMI = 1 – Magnetometer motion has activated the interrupt
  MMI = 0 – No motion

## INS2 - Interrupt Source Register 2

This register reports axis and direction of the accelerometer motion that triggered the interrupt.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| X | X | AXNI | AXPI | AYNI | AYPI | AZNI | AZPI | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x02 | | | |

**AXNI** - x negative (x-)
**AXPI** - x positive (x+)
**AYNI** - y negative (y-)
**AYPI** - y positive (y+)
**AZNI** - z negative (z-)
**AZPI** - z positive (z+)

### INS3 - Interrupt Source Register 3

The Interrupt Source Register 3 reports the axis and direction of the magnetometer motion that triggered the interrupt.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| X | X | MXNI | MXPI | MYNI | MYPI | MZNI | MZPI | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x03 | | | |

*MXNI* - x negative (x-)
*MXPI* - x positive (x+)
*MYNI* - y negative (y-)
*MYPI* - y positive (y+)
*MZNI* - z negative (z-)
*MZPI* - z positive (z+)

### INL - Interrupt Latch Release

Latched interrupt source information (at INS1 and INS2) is cleared and physical interrupt latched pin is changed to its inactive state when this register is read. If an engine is configured as an unlatched interrupt and the current state is indicating an interrupt, this release will not clear the interrupt.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x05 | | | |

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### Accelerometer output

These registers contain 16-bits of valid acceleration data for each axis. The data is updated every user-defined ODR period as set by OSA<3:0> bits in ODCNTL register. The data is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Figure 5 below. The register acceleration output binary data is represented in 16-bit 2's complement format resulting in the count range from -32768 to 32767.

| 16-bit Register Data (2's complement) | Equivalent Counts in decimal | Range = ±2g | Range = ±4g | Range = ±8g | Range = ±16g |
| --- | --- | --- | --- | --- | --- |
| 0111 1111 1111 1111 | 32767 | +1.99994g | +3.99988g | +7.99976g | +15.99951g |
| 0111 1111 1111 1110 | 32766 | +1.99988g | +3.99976g | +7.99951g | +15.99902g |
| … | … | … | … | … | … |
| 0000 0000 0000 0001 | 1 | +0.00006g | +0.00012g | +0.00024g | +0.00049g |
| 0000 0000 0000 0000 | 0 | 0.00000g | 0.00000g | 0.00000g | 0.00000g |
| 1111 1111 1111 1111 | -1 | -0.00006g | -0.00012g | -0.00024g | -0.00049g |
| … | … | … | … | … | … |
| 1000 0000 0000 0001 | -32767 | -1.99994g | -3.99988g | -7.99976g | -15.99951g |
| 1000 0000 0000 0000 | -32768 | -2.00000g | -4.00000g | -8.00000g | -16.00000g |

**Figure 5:** Acceleration (g) Calculation

### ACCEL_XOUT_L
X-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ACC_X7 | ACC_X6 | ACC_X5 | ACC_X4 | ACC_X3 | ACC_X2 | ACC_X1 | ACC_X0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x0A | | |

### ACCEL_XOUT_H
X-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ACC_X15 | ACC_X14 | ACC_X13 | ACC_X12 | ACC_X11 | ACC_X10 | ACC_X9 | ACC_X8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x0B | | |

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### ACCEL_YOUT_L

Y-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| ACC_Y7 | ACC_Y6 | ACC_Y5 | ACC_Y4 | ACC_Y3 | ACC_Y2 | ACC_Y1 | ACC_Y0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x0C | | |

### ACCEL_YOUT_H

Y-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| ACC_Y15 | ACC_Y14 | ACC_Y13 | ACC_Y12 | ACC_Y11 | ACC_Y10 | ACC_Y9 | ACC_Y8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x0D | | |

### ACCEL_ZOUT_L

Z-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| ACC_Z7 | ACC_Z6 | ACC_Z5 | ACC_Z4 | ACC_Z3 | ACC_Z2 | ACC_Z1 | ACC_Z0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x0E | | |

### ACCEL_ZOUT_H

Z-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| ACC_Z15 | ACC_Z14 | ACC_Z13 | ACC_Z12 | ACC_Z11 | ACC_Z10 | ACC_Z9 | ACC_Z8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x0F | | |

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## Magnetometer output

These registers contain 16-bits of valid magnetic field data for each axis. The data is protected from overwrite during each read, and can be converted from digital counts to magnetic field strength ($\mu$T) per Figure 6 below.

| 16-bit Data | Magnetic field $\mu$T |
| --- | --- |
| 0111 1111 1111 1111 | +1199.96338 $\mu$T |
| 0111 1111 1111 1110 | +1199.92676 $\mu$T |
| … | … |
| … | … |
| 0000 0000 0000 0001 | +0.03662 $\mu$T |
| 0000 0000 0000 0000 | 0 $\mu$T |
| 1111 1111 1111 1111 | -0.03662 $\mu$T |
| … | … |
| … | … |
| 1000 0000 0000 0001 | -1199.96338 $\mu$T |
| 1000 0000 0000 0000 | -1200.00000 $\mu$T |

**Figure 6:** Magnetic field ($\mu$T) Calculation

### MAG_XOUT_L
X-axis magnetometer output least significant byte. Data is updated at the ODR frequency determined by OSM bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
| --- | --- | --- | --- | --- | --- | --- | --- |
| MAG _X7 | MAG _X6 | MAG _X5 | MAG _X4 | MAG _X3 | MAG _X2 | MAG _X1 | MAG _X0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | | | Address: 0x10 |

### MAG _XOUT_H
X-axis magnetometer output most significant byte. Data is updated at the ODR frequency determined by OSM bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
| --- | --- | --- | --- | --- | --- | --- | --- |
| MAG _X15 | MAG _X14 | MAG_X13 | MAG_X12 | MAG_X11 | MAG_X10 | MAG_X9 | MAG_X8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | | | Address: 0x11 |

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## MAG _YOUT_L
Y-axis magnetometer output least significant byte. Data is updated at the ODR frequency determined by OSM bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| MAG_Y7 | MAG_Y6 | MAG_Y5 | MAG_Y4 | MAG_Y3 | MAG_Y2 | MAG_Y1 | MAG_Y0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|  |  |  |  |  | Address: 0x12 | | |

## MAG _YOUT_H
Y-axis magnetometer output most significant byte. Data is updated at the ODR frequency determined by OSM bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| MAG_Y15 | MAG_Y14 | MAG_Y13 | MAG_Y12 | MAG_Y11 | MAG_Y10 | MAG_Y9 | MAG_Y8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|  |  |  |  |  | Address: 0x13 | | |

## MAG _ZOUT_L
Z-axis magnetometer output least significant byte. Data is updated at the ODR frequency determined by OSM bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| MAG_Z7 | MAG_Z6 | MAG_Z5 | MAG_Z4 | MAG_Z3 | MAG_Z2 | MAG_Z1 | MAG_Z0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|  |  |  |  |  | Address: 0x14 | | |

## MAG _ZOUT_H
Z-axis magnetometer output most significant byte. Data is updated at the ODR frequency determined by OSM bits in ODCNTL register.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| MAG_Z15 | MAG_Z14 | MAG_Z13 | MAG_Z12 | MAG_Z11 | MAG_Z10 | MAG_Z9 | MAG_Z8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|  |  |  |  |  | Address: 0x15 | | |

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| | PART NUMBER: |
|---|---|
| **± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications** | **KMX62-1031 Rev. 4.0 20-Dec-2017** |

## Temperature Output

The temperature registers contain 16-bits of temperature data. If only register TEMP_OUT_H is used (8 bits), then the sensitivity can be considered as 1 count/°C. If both registers TEMP_OUT_H and TEMP_OUT_L are used (16 bits), then sensitivity can be considered as 256 counts/°C.

| 8-bit Register Data TEMP_OUT_H (2's complement) | Equivalent Counts in decimal | Temperature (°C) |
|---|---|---|
| 0101 0101 | 85 | +85 °C |
| … | … | … |
| 0000 0001 | 1 | +1 °C |
| 0000 0000 | 0 | 0 °C |
| 1111 1111 | -1 | -1 °C |
| … | … | … |
| 1101 1000 | -40 | -40 °C |

| 16-bit Register Data (2's complement) | Equivalent Counts in decimal | Temperature (°C) |
|---|---|---|
| 0101 0101 0000 0000 | 21760 | +85.000 °C |
| … | … | … |
| 0000 0001 0000 0000 | 256 | +1.0000 °C |
| … | … | … |
| 0000 0000 0100 0000 | 64 | +0.2500 °C |
| … | … | … |
| 0000 0000 0000 0001 | 1 | +0.0039 °C |
| 0000 0000 0000 0000 | 0 | 0.0000 °C |
| 1111 1111 1111 1111 | -1 | -0.0039 °C |
| … | … | … |
| 1111 1111 1100 0000 | -64 | -0.2500 °C |
| … | … | … |
| 1111 1111 0000 0000 | -256 | -1.0000 °C |
| … | … | … |
| 1101 1000 0000 0000 | -10240 | -40.000 °C |

**Figure 7:** Temperature (°C) Calculation

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### TEMP _OUT_L

Temperature sensor output least significant byte.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| TEMP7 | TEMP6 | TEMP5 | TEMP4 | TEMP3 | TEMP2 | TEMP1 | TEMP0 | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| | | | | | Address: 0x16 | | | |

### TEMP _OUT_H

Temperature sensor output most significant byte.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| TEMP15 | TEMP14 | TEMP13 | TEMP12 | TEMP11 | TEMP10 | TEMP9 | TEMP8 | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| | | | | | Address: 0x17 | | | |

## INC1 - Interrupt Control 1

This register controls routing of an interrupt reporting to physical interrupt pin GPIO1.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| X | BFI1 | WMI1 | DRDY_A1 | DRDY_M1 | FFI1 | AMI1 | MMI1 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x2A | | | |

**BFI1 -** *Buffer full interrupt reported on GPIO1*
    *BFI1 = 0 – disable*
    *BFI1 = 1 – enable*
**WMI1** - *Watermark interrupt reported on GPIO1*
    *WMI1 = 0 – disable*
    *WMI1 = 1 – enable*
**DRDY_A1** - *Accelerometer Data ready reported on GPIO1*
    *DRDY_A1 = 0 – disable*
    *DRDY_A1 = 1 – enable*
**DRDY_M1** - *Magnetometer Data ready reported on GPIO1*
    *DRDY_M1 = 0 – disable*
    *DRDY_M1 = 1 – enable*
**FFI1** - *Accelerometer Free fall interrupt reported on GPIO1*
    *FFI1 = 0 – disable*
    *FFI1 = 1 – enable*

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*AMI1 - Accelerometer motion interrupt reported on GPIO1*
    *AMI1 = 0 – disable*
    *AMI1 = 1 – enable*
*MMI1 - Magnetometer motion interrupt reported on GPIO1*
    *MMI1 = 0 – disable*
    *MMI1 = 1 – enable*

## INC2 - Interrupt Control 2

This register controls routing of an interrupt reporting to physical interrupt pin GPIO2.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| X | BFI2 | WMI2 | DRDY_A2 | DRDY_M2 | FFI2 | AMI2 | MMI2 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x2B | | | |

*BFI2 - Buffer full interrupt reported on GPIO2*
    *BFI2 = 0 – disable*
    *BFI2 = 1 – enable*
*WMI2 - Watermark interrupt reported on GPIO2*
    *WMI2 = 0 – disable*
    *WMI2 = 1 – enable*
*DRDY_A2 - Accelerometer Data ready reported on GPIO2*
    *DRDY_A2 = 0 – disable*
    *DRDY_A2 = 1 – enable.*
*DRDY_M2 - Magnetometer Data ready reported on GPIO2*
    *DRDY_M2 = 0 – disable*
    *DRDY_M2 = 1 – enable*
*FFI2 - Accelerometer Free fall interrupt reported on GPIO2*
    *FFI2 = 0 – disable*
    *FFI2 = 1 – enable*
*AMI2 - Accelerometer motion interrupt reported on GPIO2*
    *AMI2 = 0 – disable*
    *AMI2 = 1 – enable*
*MMI2 - Magnetometer motion interrupt reported on GPIO2*
    *MMI2 = 0 – disable*
    *MMI2 = 1 – enable*

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### INC3 – Interrupt Control 3

This register controls the GPIO pin configuration.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| IED2 | IEA2 | IEL2<1> | IEL2<0> | IED1 | IEA1 | IEL1<1> | IEL1<0> | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 10001000 |
| | | | | | | Address: 0x2C | | |

**IED2** – *Interrupt pin drive options for GPIO2*
   *IED2 = 0 – push-pull*
   *IED2 = 1 – open-drain*
**IEA2** - *Interrupt active level control for interrupt GPIO2*
   *IEA2 = 0 – active LOW*
   *IEA2 = 1 – active HIGH*
**IEL2 <1:0>**- *Interrupt latch control for interrupt GPIO2*
   *IEL2 = 0,0 – latched/unlatched. Unlatched feature is available for FFI, MMI, and AMI.*
   *IEL2 = 0,1 – pulsed. In pulse mode, the pulse width is 50$\mu$s.*
   *IEL2 = 1, X – trigger input for FIFO*
**IED1** – *Interrupt pin drive options for GPIO1*
   *IED1 = 0 – push-pull*
   *IED1 = 1 – open-drain*
**IEA1** - *Interrupt active level control for interrupt GPIO1*
   *IEA1 = 0 – active LOW*
   *IEA1 = 1 – active HIGH*
**IEL1 <1:0>**- *Interrupt latch control for interrupt GPIO1*
   *IEL1 = 0,0 – latched/unlatched. Unlatched feature is available for FFI, MMI, and AMI.*
   *IEL1 = 0,1 – pulsed. In pulse mode, the pulse width is 50$\mu$s.*
   *IEL1 = 1, X – trigger input for FIFO*

| IED# | IEA# | IEL#<1:0> | BFI# | WMI# | DRDY_A# | DRDY_M# | FFI# | MMI# | AMI# | GPIO state |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0,0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is held HIGH |
| 0 | 0 | 0,1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is held HIGH |
| 0 | 1 | 0,0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is held LOW |
| 0 | 1 | 0,1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is held LOW |
| 1 | 0 | 0,0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is high impedance |
| 1 | 0 | 0,1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is high impedance |
| 1 | 1 | 0,0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is held LOW |
| 1 | 1 | 0,1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The GPIO pin is held LOW |
| X | X | 1,X | X | X | X | X | X | X | X | The GPIO pin is configured as an input for FIFO trigger. If both GPIO pins are trigger, the signals are OR'ed. |

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## INC4 - Interrupt Control 4

This register controls which accelerometer axis and direction of detected motion can cause an interrupt.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| X | X | AXNIE | AXPIE | AYNIE | AYPIE | AZNIE | AZPIE | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00111111 |
| | | | | | Address: 0x2D | | | |

**AXNIE** - x negative (x-) accelerometer mask for AMI, 0=disable, 1=enable.
**AXPIE** - x positive (x+) accelerometer mask for AMI, 0=disable, 1=enable.
**AYNIE** - y negative (y-) accelerometer mask for AMI, 0=disable, 1=enable.
**AYPIE** - y positive (y+) accelerometer mask for AMI, 0=disable, 1=enable.
**AZNIE** - z negative (z-) accelerometer mask for AMI, 0=disable, 1=enable.
**AZPIE** - z positive (z+) accelerometer mask for AMI, 0=disable, 1=enable.

## INC5 - Interrupt Control 5

This register controls which magnetometer axis and direction of detected motion can cause an interrupt.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| X | X | MXNIE | MXPIE | MYNIE | MYPIE | MZNIE | MZPIE | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00111111 |
| | | | | | Address: 0x2E | | | |

**MXNIE** - x negative (x-) magnetometer mask for MMI, 0=disable, 1=enable.
**MXPIE** - x positive (x+) magnetometer mask for MMI, 0=disable, 1=enable.
**MYNIE** - y negative (y-) magnetometer mask for MMI, 0=disable, 1=enable.
**MYPIE** - y positive (y+) magnetometer mask for MMI, 0=disable, 1=enable.
**MZNIE** - z negative (z-) magnetometer mask for MMI, 0=disable, 1=enable.
**MZPIE** - z positive (z+) magnetometer mask for MMI, 0=disable, 1=enable.

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## AMI_CNTL1 - Accelerometer Motion Control 1

This register controls the accelerometer motion interrupt threshold for the wake up engine.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| AMITH7 | AMITH6 | AMITH5 | AMITH4 | AMITH3 | AMITH2 | AMITH1 | AMITH0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x2F | | | |

*AMITH<7:0>* - *Accelerometer motion interrupt threshold. This value is compared to the top 8 bits of the accelerometer 8g output.*

## AMI_CNTL2 - Accelerometer Motion Control 2

This register controls the counter setting for the accelerometer motion wake up engine.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| AMICT7 | AMICT6 | AMICT5 | AMICT4 | AMICT3 | AMICT2 | AMICT1 | AMICT0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x30 | | | |

*AMICT<7:0>* - *Accelerometer motion interrupt counter. Every count is calculated as 1/ODR delay period, where the Motion Interrupt ODR is user-defined per the OAMI bits in AMI_CNTL3. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the accelerometer should be in standby.*

### AMI_CNTL3 - Accelerometer Motion Control 3

This register has control settings for the accelerometer motion interrupt function.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| AMI_EN | AMIUL | X | X | X | OAMI2 | OAMI1 | OAMI0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | | Address: 0x31 | |

**AMI_EN** - *Accelerometer motion interrupt engine enable*
>>> *AMI_EN = 0 – disabled*
>>> *AMI_EN = 1 – enabled*

**AMIUL** - *Accelerometer Motion Interrupt latch/un-latch control for interrupt GPIO1/2*
>>> *AMIUL = 0 – latched*
>>> *AMIUL = 1 – un-latched*

**OAMI<2:0>** - *Output Data Rate at which the accelerometer motion detection performs its function.*

| OAMI<2> | OAMI <1> | OAMI <0> | Output Data Rate (Hz) |
|---|---|---|---|
| 0 | 0 | 0 | 0.781 |
| 0 | 0 | 1 | 1.563 |
| 0 | 1 | 0 | 3.125 |
| 0 | 1 | 1 | 6.25 |
| 1 | 0 | 0 | 12.5 |
| 1 | 0 | 1 | 25 |
| 1 | 1 | 0 | 50 |
| 1 | 1 | 1 | 100 |

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## MMI_CNTL1 - Magnetometer Motion Control 1

This register controls the magnetometer motion interrupt threshold for the wake up engine.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| MMITH7 | MMITH6 | MMITH5 | MMITH4 | MMITH3 | MMITH2 | MMITH1 | MMITH0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x32 | | | |

*MMITH<7:0>* - *Magnetometer motion interrupt threshold. This value is compared to the top 8 bits of the magnetometer 1200µT output.*

## MMI_CNTL2 - Magnetometer Motion Control 2

This register controls the counter setting for the magnetometer motion wake up engine.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| MMICT7 | MMICT6 | MMICT5 | MMICT4 | MMICT3 | MMICT2 | MMICT1 | MMICT0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x33 | | | |

*MMICT<7:0>* - *Magnetometer motion interrupt counter. Every count is calculated as 1/ODR delay period where the ODR is user-defined per the OMMI bits in MMI_CNTL3.*

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## MMI_CNTL3 - Magnetometer Motion Control 3

This register has control settings for the magnetometer motion interrupt function.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| MMI_EN | MMIUL | X | X | X | OMMI2 | OMMI1 | OMMI0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | | Address: 0x34 | |

**MMI_EN** - *Magnetometer motion interrupt engine enable*
> *MMI_EN = 0 – disabled*
> *MMI_EN = 1 – enabled*

**MMIUL** - *Magnetometer Motion Interrupt latch/un-latch control for interrupt GPIO1/2*
> *MMIUL = 0 – latched*
> *MMIUL = 1 – un-latched*

**OMMI<2:0>** - *Output Data Rate at which the magnetometer motion detection performs its function.*

| OMMI<2> | OMMI <1> | OMMI <0> | Output Data Rate (Hz) |
|---|---|---|---|
| 0 | 0 | 0 | 0.781 |
| 0 | 0 | 1 | 1.563 |
| 0 | 1 | 0 | 3.125 |
| 0 | 1 | 1 | 6.25 |
| 1 | 0 | 0 | 12.5 |
| 1 | 0 | 1 | 25 |
| 1 | 1 | 0 | 50 |
| 1 | 1 | 1 | 100 |

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### FFI_CNTL1 - Free Fall Control 1

This register has control settings for the free fall interrupt function.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |
|--------|--------|--------|--------|--------|--------|--------|--------|-------------|
| FFITH7 | FFITH6 | FFITH5 | FFITH4 | FFITH3 | FFITH2 | FFITH1 | FFITH0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
|  |  |  |  |  | Address: 0x35 | | | |

*FFITH<7:0>* - *Accelerometer free fall interrupt threshold. This value is compared to the top 8 bits of the accelerometer 8g output.*

### FFI_CNTL2 - Free Fall Control 2

This register has control settings for the free fall interrupt function.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |
|--------|--------|--------|--------|--------|--------|--------|--------|-------------|
| FFICT7 | FFICT6 | FFICT5 | FFICT4 | FFICT3 | FFICT2 | FFICT1 | FFICT0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
|  |  |  |  |  | Address: 0x36 | | | |

*FFICT<7:0>* - *Accelerometer free fall interrupt counter. Every count is calculated as 1/ODR delay period.*

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### FFI_CNTL3 - Free Fall Control 3

This register has control settings for the free fall interrupt function.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| FFI_EN | FFIUL | X | X | DCRM | OFFI2 | OFFI1 | OFFI0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | | Address: 0x37 | |

**FFI_EN** - *Accelerometer free fall engine enable*
> *FFI_EN = 0 – disabled*
> *FFI_EN = 1 – enabled*

**FFIUL** - *Accelerometer Free Fall Interrupt latch/un-latch control for interrupt GPIO1/2*
> *FFIUL = 0 – latched*
> *FFIUL = 1 – un-latched*

**DCRM** – *Debounce methodology control*
> *DCRM = 0 - count up/down*
> *DCRM = 1- count up/reset.*

**OFFI<2:0>** - *Output Data Rate at which the free fall detection performs its function*

| OFFI<2> | OFFI <1> | OFFI <0> | Output Data Rate (Hz) |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 12.5 |
| 0 | 0 | 1 | 25 |
| 0 | 1 | 0 | 50 |
| 0 | 1 | 1 | 100 |
| 1 | 0 | 0 | 200 |
| 1 | 0 | 1 | 400 |
| 1 | 1 | 0 | 800 |
| 1 | 1 | 1 | 1600 |

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## ODCNTL - Output Data Control Register

Output data control register

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|------|------|------|------|------|------|------|------|-------------|
| OSM3 | OSM2 | OSM1 | OSM0 | OSA3 | OSA2 | OSA1 | OSA0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00100010 |
| | | | | | | | Address: 0x38 | |

*OSM<3:0>* - *Rate at which data samples from the magnetometer (and temperature sensor if enabled) will be updated in the output data registers.*

| OSM<3> | OSM<2> | OSM<1> | OSM<0> | Output Data Rate (Hz) |
|--------|--------|--------|--------|-----------------------|
| 0 | 0 | 0 | 0 | 12.5** |
| 0 | 0 | 0 | 1 | 25** |
| 0 | 0 | 1 | 0 | 50** |
| 0 | 0 | 1 | 1 | 100** |
| 0 | 1 | 0 | 0 | 200** |
| 0 | 1 | 0 | 1 | 400* |
| 0 | 1 | 1 | 0 | 800 |
| 0 | 1 | 1 | 1 | 1600 |
| 1 | 0 | 0 | 0 | 0.781** |
| 1 | 0 | 0 | 1 | 1.563** |
| 1 | 0 | 1 | 0 | 3.125** |
| 1 | 0 | 1 | 1 | 6.25** |

**Table 12:** Magnetometer Output Data Rates (ODR)

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| | ± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications | PART NUMBER: KMX62-1031 Rev. 4.0 20-Dec-2017 |
|---|---|---|

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*OSA<3:0>* - *Rate at which data samples from the accelerometer will be updated in the output data registers.*

| OSA<3> | OSA<2> | OSA<1> | OSA<0> | Output Data Rate (Hz) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 12.5** |
| 0 | 0 | 0 | 1 | 25** |
| 0 | 0 | 1 | 0 | 50** |
| 0 | 0 | 1 | 1 | 100** |
| 0 | 1 | 0 | 0 | 200** |
| 0 | 1 | 0 | 1 | 400* |
| 0 | 1 | 1 | 0 | 800 |
| 0 | 1 | 1 | 1 | 1600 |
| 1 | 0 | 0 | 0 | 0.781** |
| 1 | 0 | 0 | 1 | 1.563** |
| 1 | 0 | 1 | 0 | 3.125** |
| 1 | 0 | 1 | 1 | 6.25** |

**Table 13:** Accelerometer Output Data Rates (ODR)

**Note:** The FIFO buffer will be updated at the faster of the two output data rates (OSM or OSA).
\* RES<0,0> available, all others will default to full power mode.
\*\* RES<0,0> and RES<0,1> available, all others will default to full power mode.

Before changing the ODR of a sensor, both sensors should be in stand-by. Write the new ODR value(s) to ODCNTL, and then enable the sensor(s).

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### CNTL1 - Control Register 1

Control register that controls the main feature set.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|------|------|-------|----------|------|----------|------|------|-------------|
| SRST | STEN | STPOL | RESERVED | COTC | RESERVED | X | X | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x39 | | | |

**SRST** – *The Software Reset bit initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished. Please refer to Technical Note TN005 Power-On Procedure for more information on software reset.*
*SRST = 0 – no action*
*SRST = 1 – start RAM reboot routine*

**STEN** - *ST enable. This bit enables the self-test mode that will produce a change in both the accelerometer and magnetometer transducers and can be measured in the output registers.*
*STEN = 0 – ST is disabled*
*STEN = 1 – ST is enabled*

**STPOL** – *Accelerometer and Magnetometer ST polarity.*
*STPOL = 0 – ST polarity is positive*
*STPOL = 1 – ST polarity is negative*

**COTC** – *The Command Test Control bit is used to verify proper ASIC functionality.*
*COTC = 0 – no action*
*COTC = 1 – sets COTR register to 0xAA. When COTR register is then read, sets COTC bit to 0 and sets COTR register to 0x55.*

**RESERVED** – *the setting of reserved bits should not be altered.*

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### CNTL2 - Control Register 2

This register is used to enable and disable the sensors as well as to set their operation ranges.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| X | TEMP_EN | GSEL1 | GSEL0 | RES1 | RES0 | MAG_EN | ACCEL_EN | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | Address: 0x3A | | |

**TEMP_EN** controls the operating mode of the KMX62's temperature sensors. MAG_EN must also be enabled for temperature data to be converted. Output data rate is locked to the magnetometer's Output Data Rate as set by OSM<3:0> bits in ODCNTL register.

TEMP_EN = 0 – stand-by mode
TEMP_EN = 1 – operating mode. Magnetometer and temperature output registers are updated at the selected output data rate.

**GSEL<1, 0>** selects the acceleration range of the accelerometer outputs.

| GSEL<1> | GSEL<0> | Range |
|---|---|---|
| 0 | 0 | ±2g |
| 0 | 1 | ±4g |
| 1 | 0 | ±8g |
| 1 | 1 | ±16g |

**Table 14**: Selected Acceleration Range

**RES<1, 0>** selects the resolution of both sensors.

| RES<1> | RES<0> | Accelerometer over sample | Magnetometer over sample |
|---|---|---|---|
| 0 | 0 | 4 | 2 |
| 0 | 1 | 32 | 16 |
| 1 | 0 | maximum | maximum |
| 1 | 1 | maximum | maximum |

**Table 15:** Selected resolution range

**MAG_EN** controls the operating mode of the KMX62's magnetometer sensor.
MAG_EN = 0 – stand-by mode.
MAG_EN = 1 – operating mode. Magnetometer output registers are updated at the selected output data rate.

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*ACCEL_EN* controls the operating mode of the KMX62's accelerometer
  *ACCEL_EN = 0 – stand-by mode.*
  *ACCEL_EN = 1 – operating mode. Accelerometer output registers are updated at the selected output data rate.*

## COTR - Command Test Response

The Command Test Response (COTR) register is used to verify proper integrated circuit functionality. The value of this register will change from a default value of 0x55 to 0xAA when COTC bit in CNTL1 register is set. After reading 0xAA from this register, the byte value returns to the default value of 0x55 and COTC bit in CNTL1 register is cleared.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| COTR7 | COTR6 | COTR5 | COTR4 | COTR3 | COTR2 | COTR1 | COTR0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 01010101 |
| | | | | | | | | Address: 0x3C |

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### BUF_CTRL_1,2,3

These registers control the buffer sample buffer operation.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| SMT_TH7 | SMT_TH6 | SMT_TH5 | SMT_TH4 | SMT_TH3 | SMT_TH2 | SMT_TH1 | SMT_TH0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | Address: 0x77 | | **BUF_CTRL_1** |

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | BUF_M1 | BUF_M0 | SMT_TH8 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | Address: 0x78 | | **BUF_CTRL_2** |

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---|---|---|---|---|---|---|---|---|
| BFI_EN | BUF_AX | BUF_AY | BUF_AZ | BUF_MX | BUF_MY | BUF_MZ | BUF_TEMP | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | Address: 0x79 | | **BUF_CTRL_3** |

*SMP_TH<8:0> Sample Threshold* - *determines the number of <u>data bytes</u> that will trigger a watermark interrupt or will be saved prior to a trigger event. The maximum number of data bytes is 384 (example - 32 samples of 3 axes of accel and 3 axes of mag by 2 bytes per axis).*

*BUF_M<1:0>* - *selects the operating mode of the sample buffer*

| BUF_M<1> | BUF_M<0> | Mode | Description | Sample Threshold Operation |
|---|---|---|---|---|
| 0 | 0 | FIFO | The buffer collects 384 bytes of data until full, collecting new data only when the buffer is not full. | Specifies how many buffer samples are needed to trigger a watermark interrupt. |
| 0 | 1 | Stream | The buffer holds the last 384 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data. | Specifies how many buffer samples are needed to trigger a watermark interrupt. |
| 1 | 0 | Trigger | When a trigger event occurs (interrupt is caused by one of the digital engines or when a logic HIGH signal occurs on the TRIG pin), the buffer holds the last data set of SMP_TH[8:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full. | Specifies how many buffer samples before the trigger event are retained in the buffer. |
| 1 | 1 | FILO | The buffer holds the last 384 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first. | Specifies how many buffer samples are needed to trigger a watermark interrupt. |

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*BFI_EN* controls the buffer full interrupt
  *BFI_EN = 0 – the buffer full interrupt (BFI) is disabled*
  *BFI_EN = 1 – the buffer full interrupt (BFI) will be triggered when the buffer is full*

*BUF_(AX, AY, AZ, MX, MY, MZ, TEMP)* controls the data to be buffered.
  *BUF_(AX, AY,AZ, MX, MY, MZ, TEMP) = 0 – indicates data is not buffered*
  *BUF_(AX, AY,AZ, MX, MY, MZ, TEMP)= 1 – indicates data is buffered*

## BUF_CLEAR

Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

| W | W | W | W | W | W | W | W |
|---|---|---|---|---|---|---|---|
| BUFCLR7 | BUFCLR6 | BUFCLR5 | BUFCLR4 | BUFCLR3 | BUFCLR2 | BUFCLR1 | BUFCLR0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | Address: 0x7A | | |

## BUF_STATUS_1,2,3

This register reports the status of the sample buffer.

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| SMP_LEV7 | SMP_LEV6 | SMP_LEV5 | SMP_LEV4 | SMP_LEV3 | SMP_LEV2 | SMP_LEV1 | SMP_LEV0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x7B | | | **BUF_STATUS_1** |

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| SMP_PAST5 | SMP_PAST4 | SMP_PAST3 | SMP_PAST2 | SMP_PAST1 | SMP_PAST0 | BUF_TRIG | SMP_LEV8 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x7C | | | **BUF_ STATUS _2** |

| R | R | R | R | R | R | R | R | |
|---|---|---|---|---|---|---|---|---|
| SMP_PAST13 | SMP_PAST12 | SMP_PAST11 | SMP_PAST10 | SMP_PAST9 | SMP_PAST8 | SMP_PAST7 | SMP_PAST6 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | Address: 0x7D | | | **BUF_ STATUS _3** |

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*SMP_LEV<8:0> Sample Level*; reports the number of <u>data bytes</u> that have been stored in the sample buffer. If this register reads 0, no data has been stored in the buffer. If the buffer data is read past this level the part will return 32,767 (maximum value).

| Buffered Outputs (e.g. AX, AY, AZ, MX, MY, MZ, TEMP) | Maximum sets | Maximum bytes |
|---|---|---|
| 1 | 192 | 384 |
| 2 | 96 | 384 |
| 3 | 64 | 384 |
| 4 | 48 | 384 |
| 5 | 38 | 380 |
| 6 | 32 | 384 |
| 7 | 27 | 378 |

*BUF_TRIG* reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.

*SMP_PAST<13:0> Sample overflow*; reports the number of <u>data bytes</u> that have been missed since the sample buffer was filled. If this register reads 0, the buffer has not overflowed. This is cleared for "BUF_CLEAR" command and when the data is read from "BUF_READ"

## BUF_READ

Data in the buffer can be read according to the BUF_M settings in BUF_CTRL2. More samples can be retrieved by continuing to toggle SCL after the read command is executed. Data should be read using an auto-increment. Additional samples cannot be written to the buffer while data is being read from the buffer using an auto-increment mode. Output data is in 2's Complement format.

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| BUF7 | BUF6 | BUF5 | BUF4 | BUF3 | BUF2 | BUF1 | BUF0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | | Address: 0x7E | |

**Embedded Applications**

### Accelerometer Motion Interrupt Feature

The Accelerometer Motion Interrupt feature of the KMX62 reports qualified changes in the high-pass filtered acceleration based on the Accelerometer Motion Interrupt Threshold (AMITH). If the high-pass filtered acceleration on any axis is greater than the user-defined Accelerometer Motion Interrupt Threshold (AMITH), the device has transitioned from an inactive state to an active state. Equation 1 shows how to calculate the AMITH register value for a desired wake-up threshold. The wake-up engine function is independent of the user selected g-range and resolution.

$$AMITH \text{ (counts)} = \text{Wake-Up Threshold (g)} \times 16 \text{ (counts/g)}$$

**Equation 1:** Accelerometer Wake-Up Threshold

An 8-bit raw unsigned value represents a counter that permits the user to qualify each active/inactive state change. Note that Accelerometer Motion Interrupt Counter (AMICT) count value qualifies 1 (one) user-defined Wake-up Function ODR period as set by OAMI<2:0> bits in AMI_CNTL3 register. Equation 2 shows how to calculate the AMICT value for a desired wake-up delay time.

$$AMICT \text{ (counts)} = \text{Wake-Up Delay Time (sec)} \times \text{Wake-up Function ODR (Hz)}$$

**Equation 2:** Accelerometer Wake-Up Delay Time

The latched accelerometer motion interrupt response algorithm works as following: while the part is in inactive state, the algorithm evaluates differential measurement between each new acceleration data point with the preceding one and evaluates it against the Activity Threshold (AMITH). When the differential measurement is greater than AMITH, the Accelerometer Motion Interrupt Counter (AMICT) starts the count. Differential measurements are now calculated based on the difference between the current acceleration and the acceleration when the counter started. The part will report that motion has occurred at the end of the count assuming each differential measurement has remained above the threshold. If at any moment during the count the differential measurement falls below the threshold, the counter will stop the count and the part will remain in inactive state.

To illustrate how the algorithm works, consider the Figure 8 below that shows the latched response of the motion detection algorithm with the Accelerometer Motion Interrupt Counter (AMICT) set to 10 counts. Note how the difference between the acceleration sample marked in red and the one marked in green resulted in a differential measurement represented with orange bar being above the Activity Threshold (AMITH). At this point, the Accelerometer Motion Interrupt Counter (AMICT) begins to count number of counts stored in AMI_CNTL2 register and the wake-up algorithm will evaluate the difference between each new acceleration measurement and the measurement marked in green that will remain a reference measurement for the duration of the counter count. At the end of the count, assuming all differential measurements were larger than Activity Threshold (AMITH), as is the case in the example showed in Figure 8 a motion event will be reported.

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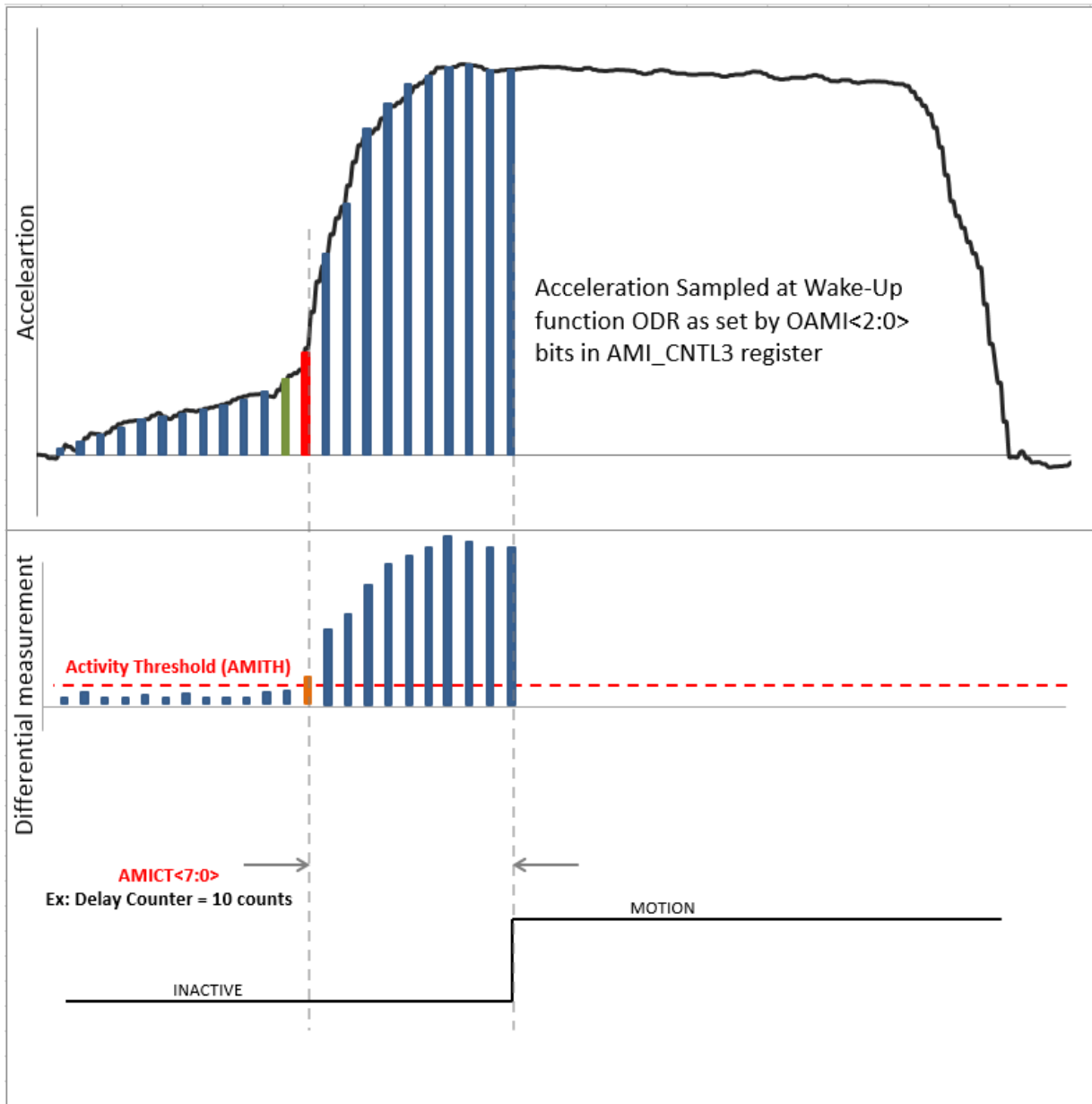| | **± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications** | **PART NUMBER:** **KMX62-1031** **Rev. 4.0** **20-Dec-2017** |
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**Figure 8:** Latched Motion Interrupt Response

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## Magnetometer Motion Interrupt Feature

The Magnetometer Motion Interrupt feature of the KMX62 reports qualified changes in the high-pass filtered magnetometer output based on the Magnetometer Motion Interrupt Threshold (MMITH). If the high-pass filtered magnetometer output on any axis is greater than the user-defined Magnetometer Motion Interrupt Threshold (MMITH), the device has transitioned from an inactive state to an active state. Equation 3 shows how to calculate the MMITH register value for a desired wake-up threshold.

$$\text{MMITH (counts)} = \text{Wake-Up Threshold (µT)} \times 0.107 \text{ (counts/µT)}$$

**Equation 3:** Magnetometer Wake-Up Threshold

An 8-bit raw unsigned value represents a counter that permits the user to qualify each active/inactive state change. Note that Magnetometer Motion Interrupt Counter (MMICT) count value qualifies 1 (one) user-defined Wake-up Function ODR period as set by OMMI<2:0> bits in MMI_CNTL3 register. Equation 4 shows how to calculate the MMICT value for a desired wake-up delay time.

$$\text{MMICT (counts)} = \text{Wake-Up Delay Time (sec)} \times \text{Wake-up Function ODR (Hz)}$$

**Equation 4:** Magnetometer Wake-Up Delay Time

The latched Magnetometer Motion Interrupt response algorithm works as following: while the part is in inactive state, the algorithm evaluates differential measurement between each new acceleration data point with the preceding one and evaluates it against the Activity Threshold (MMITH). When the differential measurement is greater than MMITH, the Magnetometer Motion Interrupt Counter (MMICT) starts the count. Differential measurements are now calculated based on the difference between the current acceleration and the acceleration when the counter started. The part will report that motion has occurred at the end of the count assuming each differential measurement has remained above the threshold. If at any moment during the count the differential measurement falls below the threshold, the counter will stop the count and the part will remain in inactive state.

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### Free fall Detect

The KMX62 features a Free fall interrupt that sends a flag through the GPIO1 or the GPIO2 output pins when the accelerometer senses a Free fall event. The interrupt event is also reflected on the INT (bit 7) and FFI (bit 2) of the INS1 registers. A Free fall event is evident when all three accelerometer axes simultaneously fall below a certain acceleration threshold for a set amount of time. The KMX62 gives the user the option to define the acceleration threshold value through the FFI_CNTL1 8-bit register where 256 counts cover the g range of the accelerometer. This value is compared to the top 8 bits of the accelerometer 8g output value (independent of the actual g-range setting of the device). Equation 5 shows how to calculate the FFITH register value for a desired Free fall threshold. The threshold of 0.5g is a good starting point.

$$FFITH \text{ (counts)} = Free \text{ fall Threshold (g) x 16 (counts/g)}$$

**Equation 5:** Free fall Threshold

Through the Free Fall Counter (FFICT), the user can set the amount of time all three accelerometer axes must simultaneously remain below the FFITH acceleration threshold before the Free fall interrupt flag is sent through the GPIO1 or the GPIO2 output pins. This delay/debounce time is defined by the available 0 to 255 counts, which represent accelerometer samples taken at the Free fall ODR defined by OFFI<2:0> bits in the FFI_CNTL3 register. Every count is calculated as 1/ODR delay period. Equation 6 shows how to calculate the FFC register value for a desired Free fall delay. The delay of 0.32 sec is a good starting point.

$$FFICT \text{ (counts)} = Free \text{ fall delay (sec) x Free fall ODR (Hz)}$$

**Equation 6:** Free fall Threshold

When the Free fall interrupt is enabled the part must not be in a physical state that would trigger the Free fall interrupt or the delay will not be correct for the present Free fall.

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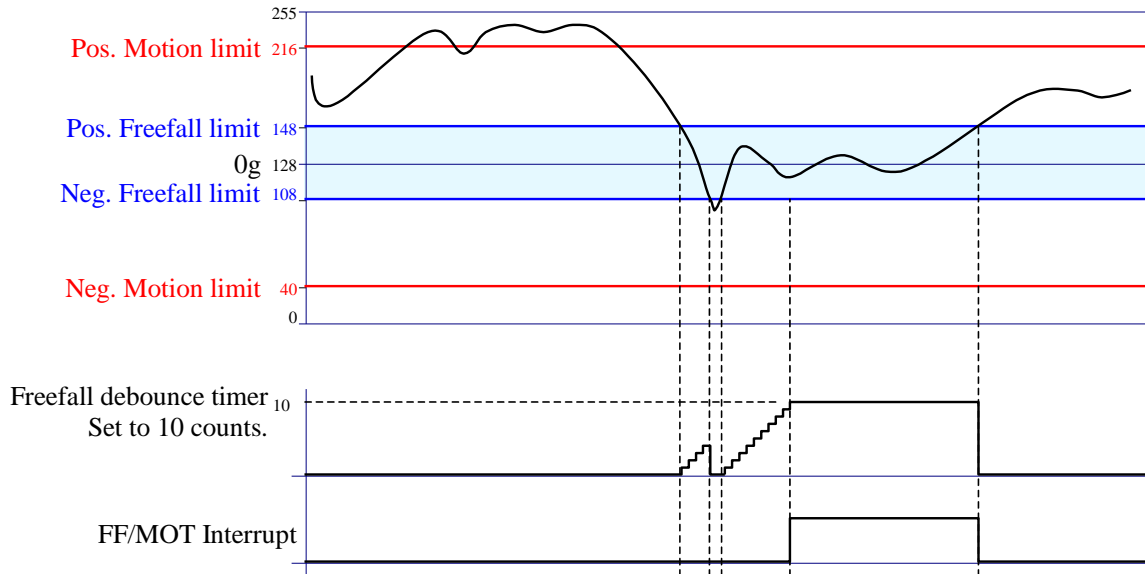## Typical Freefall Interrupt Example (nonLatching)



**Figure 9:** Typical Free Fall Interrupt Example (FFI_CNTL3 FFIUL = 1)
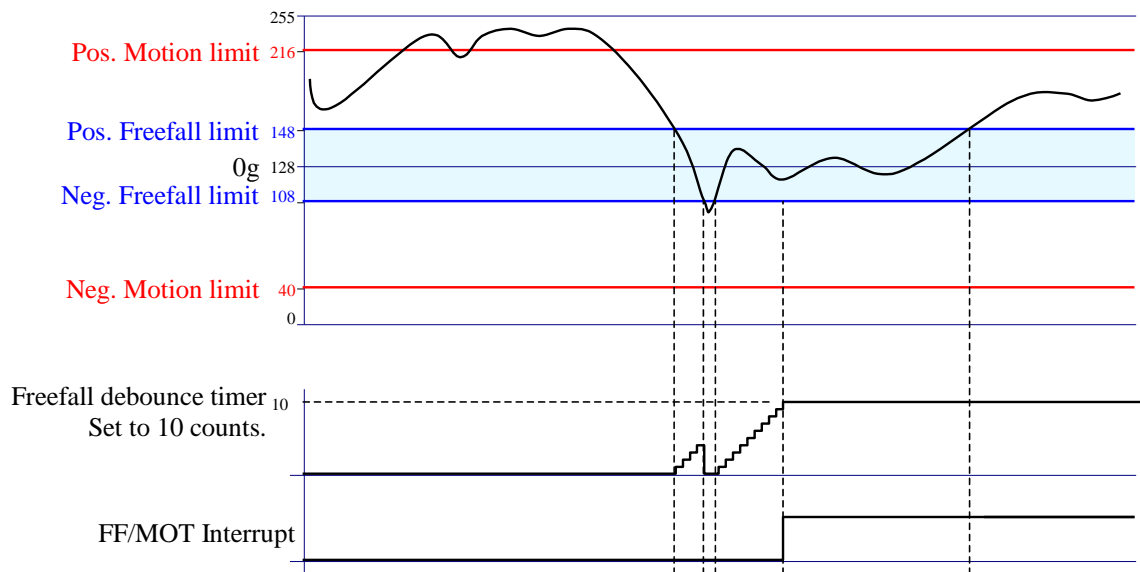
## Typical Freefall Interrupt Example (Latching)



**Figure 10:** Typical Free Fall Interrupt Example (FFI_CNTL3 FFIUL = 0)

## Sample Buffer Feature Description

The sample buffer feature of the KMX62 accumulates and outputs data based on how it is configured. There are 4 buffer modes available. Data is collected at the highest ODR specified by OSA[3:0] and OSM[3:0] in the ODCNTL (Output Data Control) Register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

### FIFO Mode

Data Accumulation
> Sample collection stops when the buffer is full.

Data Reporting
> Data is reported with the <u>oldest</u> byte of the <u>oldest</u> sample first.

Status Indicators
> A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or reading greater than SMPX.

$$SMPX = SMP\_LEV[8:0] - SMP\_TH[8:0]$$

Equation 7: Samples Above Sample Threshold

### Stream Mode

Data Accumulation
> Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting
> Data is reported with the <u>oldest</u> sample first (uses FIFO read pointer).

Status Indicators
> A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 7).

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**Trigger Mode**

Data Accumulation

When a physical interrupt is caused by one of the digital engines or when a logic HIGH signal occurs on the TRIG pin, the trigger event is asserted and SMP_TH[8:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs and there are at least SMP_TH[8:0] samples in the buffer, BUF_TRIG in BUF_STATUS_2 is asserted.

**FILO Mode**

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the newest byte of the newest sample first.

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 7).

**Buffer Operation**

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Regardless of the selected mode, the buffer fills sequentially, two-byte at a time and one set count number of bytes at the highest ODR. Figure 11 shows one 14-byte data sample with all devices (accelerometer, temp sensor and magnetometer) enabled. Note the location of the FILO read pointer versus that of the FIFO read pointer. Figure 12 shows one 12-byte data sample with accelerometer and magnetometer enabled and temperature sensor disabled. Figure 12 - Figure 21 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Note: When a write to BUF_CLEAR register is made, the buffer read pointer is moved to the location of the buffer write pointer.

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Note: If the buffer control states that a sensor's data should be buffered, but that sensor is not enabled, then all buffer entries for that sensor will be that sensor's last ADC conversion prior to it being disabled.

| Index | Byte | |
|---|---|---|
| 0 | ACCEL X_L | <---- FIFO read pointer |
| 1 | ACCEL X_H | |
| 2 | ACCEL Y_L | |
| 3 | ACCEL Y_H | |
| 4 | ACCEL Z_L | |
| 5 | ACCEL Z_H | |
| 6 | MAG X_L | |
| 7 | MAG X_H | |
| 8 | MAG Y_L | |
| 9 | MAG Y_H | |
| 10 | MAG Z_L | |
| 11 | MAG Z_H | |
| 12 | TEMP_L | |
| 13 | TEMP_H | <---- FILO read pointer |
| 14 | | |

buffer write pointer (Sample Level) ----> (Index 14)

**Figure 11:** One Buffer Sample with accelerometer, temperature sensor and magnetometer all enabled

| Index | Byte | |
|---|---|---|
| 0 | ACCEL X_L | <---- FIFO read pointer |
| 1 | ACCEL X_H | |
| 2 | ACCEL Y_L | |
| 3 | ACCEL Y_H | |
| 4 | ACCEL Z_L | |
| 5 | ACCEL Z_H | |
| 6 | MAG X_L | |
| 7 | MAG X_H | |
| 8 | MAG Y_L | |
| 9 | MAG Y_H | |
| 10 | MAG Z_L | |
| 11 | MAG Z_H | <---- FILO read pointer |
| 12 | | |

buffer write pointer (Sample Level) ----> (Index 12)

**Figure 12**: One Buffer Sample with accelerometer and magnetometer enabled and temperature sensor disabled

Note in Figure 13 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.
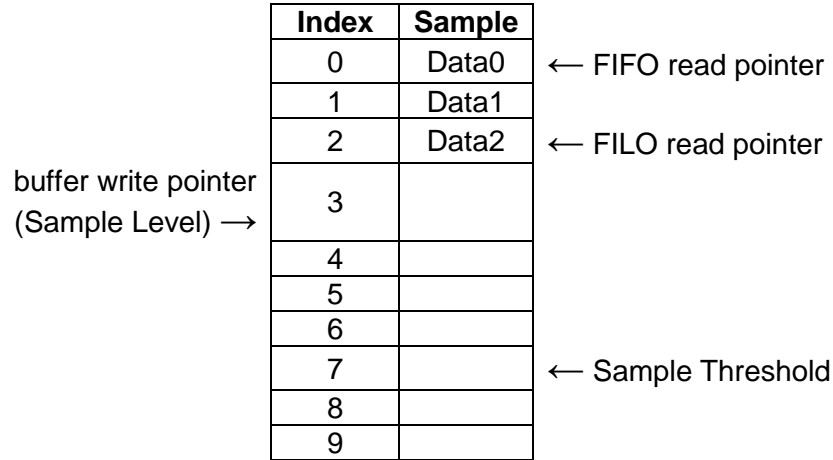
| Index | Sample |
|-------|--------|
| 0 | Data0 | ← FIFO read pointer |
| 1 | Data1 | |
| 2 | Data2 | ← FILO read pointer |
| 3 | | buffer write pointer (Sample Level) → |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | ← Sample Threshold |
| 8 | | |
| 9 | | |

**Figure 13:** Buffer Filling

The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 14 the location of the FILO read pointer versus that of the FIFO read pointer.
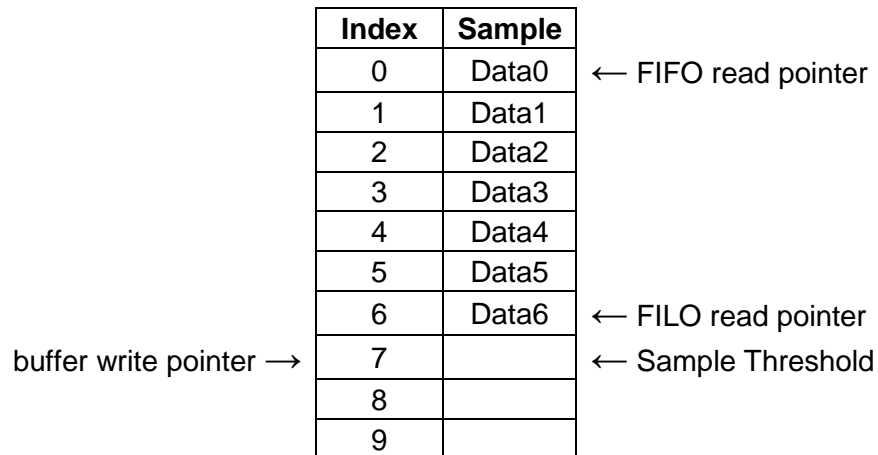
| Index | Sample |
|-------|--------|
| 0 | Data0 | ← FIFO read pointer |
| 1 | Data1 | |
| 2 | Data2 | |
| 3 | Data3 | |
| 4 | Data4 | |
| 5 | Data5 | |
| 6 | Data6 | ← FILO read pointer |
| 7 | | ← Sample Threshold   (buffer write pointer →) |
| 8 | | |
| 9 | | |

**Figure 14:** Buffer Approaching Sample Threshold

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In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.
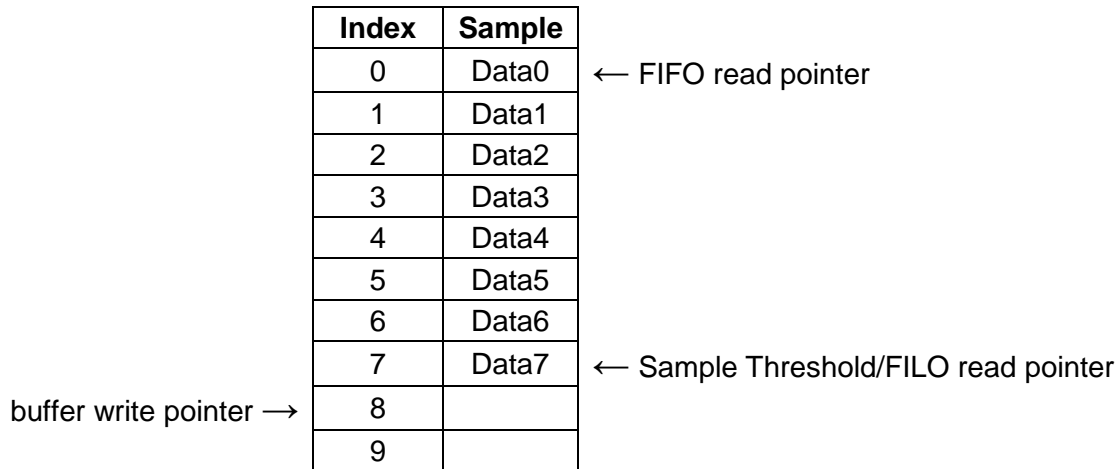
| Index | Sample | |
| --- | --- | --- |
| 0 | Data0 | ← FIFO read pointer |
| 1 | Data1 | |
| 2 | Data2 | |
| 3 | Data3 | |
| 4 | Data4 | |
| 5 | Data5 | |
| 6 | Data6 | |
| 7 | Data7 | ← Sample Threshold/FILO read pointer |
| 8 | | buffer write pointer → |
| 9 | | |

**Figure 15**: Buffer at Sample Threshold

In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 16 how Data0 was thrown out to make room for Data8.
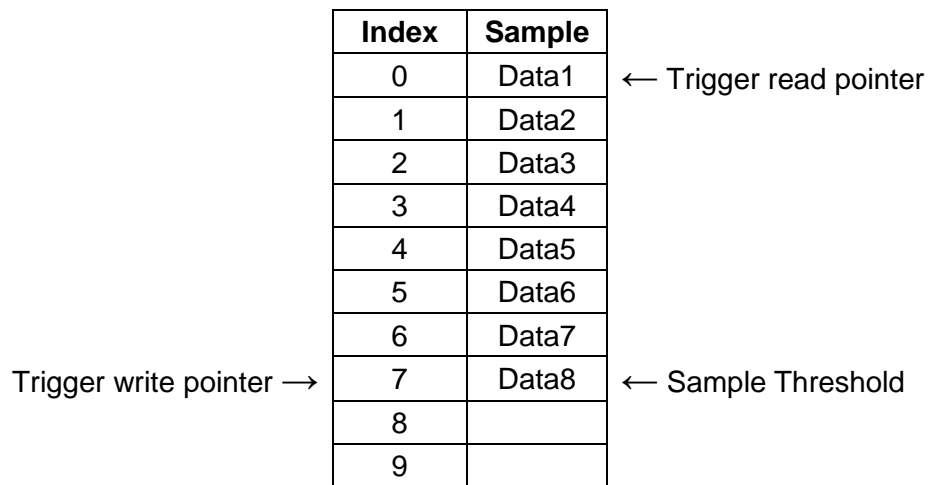
| Index | Sample | |
| --- | --- | --- |
| 0 | Data1 | ← Trigger read pointer |
| 1 | Data2 | |
| 2 | Data3 | |
| 3 | Data4 | |
| 4 | Data5 | |
| 5 | Data6 | |
| 6 | Data7 | |
| 7 | Data8 | Trigger write pointer → / ← Sample Threshold |
| 8 | | |
| 9 | | |

**Figure 16:** Additional Data Prior to Trigger Event

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After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 17. This results in the buffer holding SMP_TH[8:0] samples prior to the trigger event, and SMPX samples after the trigger event.

| Index | Sample | |
|---|---|---|
| 0 | Data1 | ← Trigger read pointer |
| 1 | Data2 | |
| 2 | Data3 | |
| 3 | Data4 | |
| 4 | Data5 | |
| 5 | Data6 | |
| 6 | Data7 | |
| 7 | Data8 | ← Sample Threshold |
| 8 | Data9 | |
| 9 | Data10 | |

**Figure 17:** Additional Data After Trigger Event

In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

| Index | Sample | |
|---|---|---|
| 0 | Data0 | ← FIFO read pointer |
| 1 | Data1 | |
| 2 | Data2 | |
| 3 | Data3 | |
| 4 | Data4 | |
| 5 | Data5 | |
| 6 | Data6 | |
| 7 | Data7 | ← Sample Threshold |
| 8 | Data8 | |
| 9 | Data9 | ← FILO read pointer |

**Figure 18:** Buffer Full

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After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 19 how Data0 was thrown out to make room for Data10.

| Index | Sample | |
|---|---|---|
| 0 | Data1 | ← FIFO read pointer |
| 1 | Data2 | |
| 2 | Data3 | |
| 3 | Data4 | |
| 4 | Data5 | |
| 5 | Data6 | |
| 6 | Data7 | |
| 7 | Data8 | ← Sample Threshold |
| 8 | Data9 | |
| 9 | Data10 | ← FILO read pointer |

**Figure 19:** Buffer Full – Additional Sample Accumulation in Stream or FILO Mode

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 20.

| Index | Sample | |
|---|---|---|
| 0 | Data1 | ← FIFO read pointer |
| 1 | Data2 | |
| 2 | Data3 | |
| 3 | Data4 | |
| 4 | Data5 | |
| 5 | Data6 | |
| 6 | Data7 | |
| 7 | Data8 | ← Sample Threshold |
| 8 | Data9 | ← FILO read pointer |
| 9 | | buffer write pointer → |

**Figure 20:** FIFO Read from Full Buffer

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In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 21.
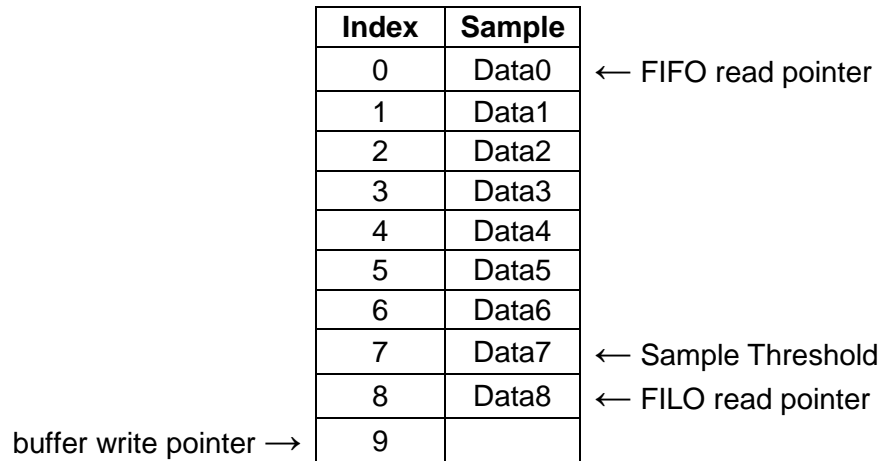
| Index | Sample | |
|:-----:|:------:|---|
| 0 | Data0 | ← FIFO read pointer |
| 1 | Data1 | |
| 2 | Data2 | |
| 3 | Data3 | |
| 4 | Data4 | |
| 5 | Data5 | |
| 6 | Data6 | |
| 7 | Data7 | ← Sample Threshold |
| 8 | Data8 | ← FILO read pointer |
| 9 | | buffer write pointer → |

**Figure 21:** FILO Read from Full Buffer

## Revision History

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial Release. | 29-May-2015 |
| 2.0 | Updated Writing/Reading Description in I2C.<br>Updated current consumption diagrams.<br>Updated pin description table.<br>Added Notice.<br>Revised environmental spec (RoHS + REACH). | 20-Oct-2015 |
| 3.0 | Updated Temperature (°C) Calculation 256counts/C for 16bit.<br>Updated Trigger Buffer Description. | 01-Mar-2016 |
| 4.0 | Updated Filter -3dB cutoff value in RES = 00, 01.<br>Updated maximum start up time.<br>Updated I2C Description Sections.<br>Added note in Pin Descriptions to indicate that pins 3, 5, and 12 (GND) are internally tied together.<br>Updated sensitivity format to counts/g and counts/uT.<br>Fixed temperature sensor sensetivity in 16-bit mode.<br>Added noise density.<br>Removed Noise plots.<br>Removed negative self test specifications.<br>Added Wake Up and Free Fall engine descriptions.<br>Updated orientation and product outline drawings.<br>Added accel orientation tables.<br>Revised and improved register descriptions.<br>Product Notice section is appended at the end of the document. | 20-Dec-2017 |

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## Appendix

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|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

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