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### **KSB596**

#### **Power Amplifier Applications**

• Complement to KSD526



1.Base 2.Collector 3.Emitter

## **PNP Epitaxial Silicon Transistor**

### Absolute Maximum Ratings $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Value	Units
$V_{CBO}$	Collector-Base Voltage	- 80	V
V <sub>CEO</sub>	Collector-Emitter Voltage	- 80	V
V <sub>EBO</sub>	Emitter-Base Voltage	- 5	V
I <sub>C</sub>	Collector Current(DC)	- 4	Α
I <sub>B</sub>	Base Current	- 0.4	Α
P <sub>C</sub>	Collector Dissipation (T <sub>C</sub> =25°C)	30	W
TJ	Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature	- 55 ~ 150	°C

### Electrical Characteristics $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage	$I_C = -50 \text{mA}, I_B = 0$	- 80			V
BV <sub>EBO</sub>	Emitter-Base Breakdown Voltage	I <sub>E</sub> = - 10mA, I <sub>C</sub> = 0	- 5			V
I <sub>CBO</sub>	Collector Cut-off Current	$V_{CB} = -80V, I_{E} = 0$			- 70	μΑ
I <sub>EBO</sub>	Emitter Cut-off Current	$V_{EB} = -5V, I_{C} = 0$			- 100	μΑ
h <sub>FE1</sub>	DC Current Gain	$V_{CE} = -5V, I_{C} = -0.5A$	40		240	
h <sub>FE2</sub>		$V_{CE} = -5V, I_{C} = -3A$	15			
V <sub>CE</sub> (sat)	Collector-Emitter Saturation Voltage	$I_C = -3A, I_B = -0.3A$		- 1	- 1.7	V
V <sub>BE</sub> (on)	Base-Emitter ON Voltage	$V_{CE} = -5V, I_{C} = -3A$		- 1	- 1.5	V
f <sub>T</sub>	Current Gain Bandwidth Product	$V_{CE} = -5V, I_{C} = -0.5A$	3			MHz
C <sub>ob</sub>	Output Capacitance	$V_{CB} = -10V, I_{E} = 0$ f = 1MHz		130		pF

### **h**<sub>FE</sub> Classification

Classification	R	0	Υ
h <sub>FE1</sub>	40 ~ 80	70 ~ 140	120 ~ 240

## **Typical Characteristics**

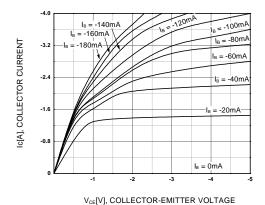


Figure 1. Static Characteristic

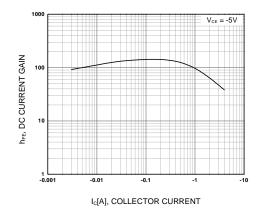


Figure 2. DC current Gain

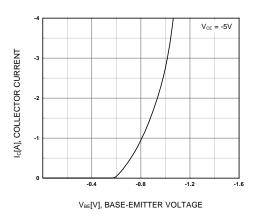


Figure 3. Base-Emitter Saturation Voltage

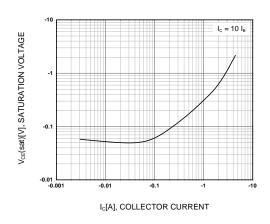


Figure 4. Collector-Emitter Saturation Voltage

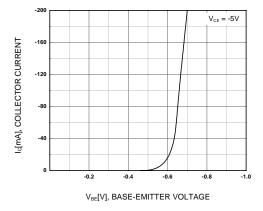


Figure 5. Base-Emitter On Voltage

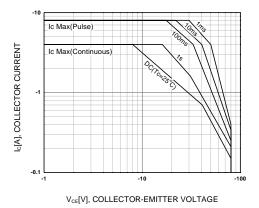


Figure 6. Safe Operating Area

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# Typical Characteristics (Continued)

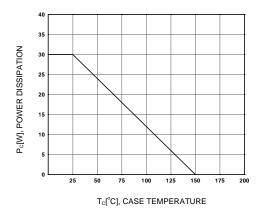


Figure 1. Power Derating

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