KSZ8863MLL/FLL/RLL
Evaluation Board User's Guide

KSZ8863MLL/FLL/RLL Integrated 3-Port 10/100 Managed Switch with PHYs

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Revision History

Revision	Date	Summary of Changes
1.0	07/15/09	Initial Release
1.1	01/11/11	Update description.

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1.0 Introduction

The KSZ8863MLL/FLL/RLL is Micrel's third generation fully integrated 3-port switch. The two PHY units of KSZ8863MLL/RLL support 10BASE-T and 100BASE-TX. The KSZ8863FLL supports 100BASE-FX. The devices have been designed for cost sensitive systems, however, still offer a multitude of features, such as switch management, port and tag based VLAN, QoS priority, one MII interfaces and CPU control and data interfaces.

The KSZ8863MLL/FLL/RLL is an excellent choice for VoIP Phone, Set-top/Game Box, SOHO Residential Gateway, industrial Ethernet systems and as a standalone 3-port switch.

The KSZ8863MLL/FLL/RLL Evaluation Board provides a convenient means to evaluate the KSZ8863MLL/FLL/RLL's rich feature set. Easy access is provided to all of the KSZ8863MLL/FLL/RLL pins, with jumpers and interface connectors allowing quick configuration and re-configuration of the board. MIIM, EEPROM programming, SPI emulation software are also provided to access the more extensive features of the KSZ8863MLL/FLL/RLL, via a PC USB port.

2.0 Board Features

- Micrel's KSZ8863MLL/FLL/RLL Integrated 3-Port 10/100 Managed Ethernet Switch
- Two RJ-45 Jacks for Ethernet LAN Interfaces with corresponding Isolation Magnetics (KSZ98863MLL/RLL)
- Auto MDI/MDI-X on the PHY port
- 1 PHY Mode and 1 MAC Mode MII Connector for the Switch RMII/MII Interface
- 2 100Base-FX fiber interface(KSZ8863FLL)
- 1 USB port to emulate an MIIM, EEPROM, SPI Interface
- On board EEPROM
- 2 LEDs per port to Indicate the Status and Activity of the RJ45 port
- 1 power jack for 5VDC Universal Power Supply

3.0 Evaluation Kit Contents

The KSZ8863MLL/FLL/RLL Evaluation kit includes the following:

- KSZ8863MLL/FLL/RLL Evaluation Board Revision 1.0
- KSZ8863MLL/FLL/RLL Evaluation Board User's Guide
- Micrel Switch Configuration Software Version 1.0.5
- Micrel Switch Configuration Software User Guide
- KSZ8863MLL/FLL/RLL Evaluation Board Schematic Revision 1.0
  (Contact your Micrel FAE for the latest schematic)

Note: USB cable and 5V DC Wall Power Supply is not included in the design kit (the dimension of the output plug of 5V DC wall power supply is 2.5x5.5x9.5mm or 0.1x0.218x0.375inch)

4.0 Hardware Description

The KSZ8863MLL/FLL/RLL Evaluation Board is in a compact form factor and can sit on a bench near a computer. There are three options for configuration: strap in mode, EEPROM mode, and SPI mode. Strap in mode configuration is easily done with on board jumper options. EEPROM mode and SPI mode are accomplished through a built in USB port interface. With the Micrel software and your PC, you can use the USB port to reprogram the EEPROM on board, or use the SPI interface to access the KSZ8863MLL/FLL/RLL's full feature set. The board also features one

MII connector for the Switch MII interface. It is to facilitate connection from the switch to either the external CPU or the external PHY.

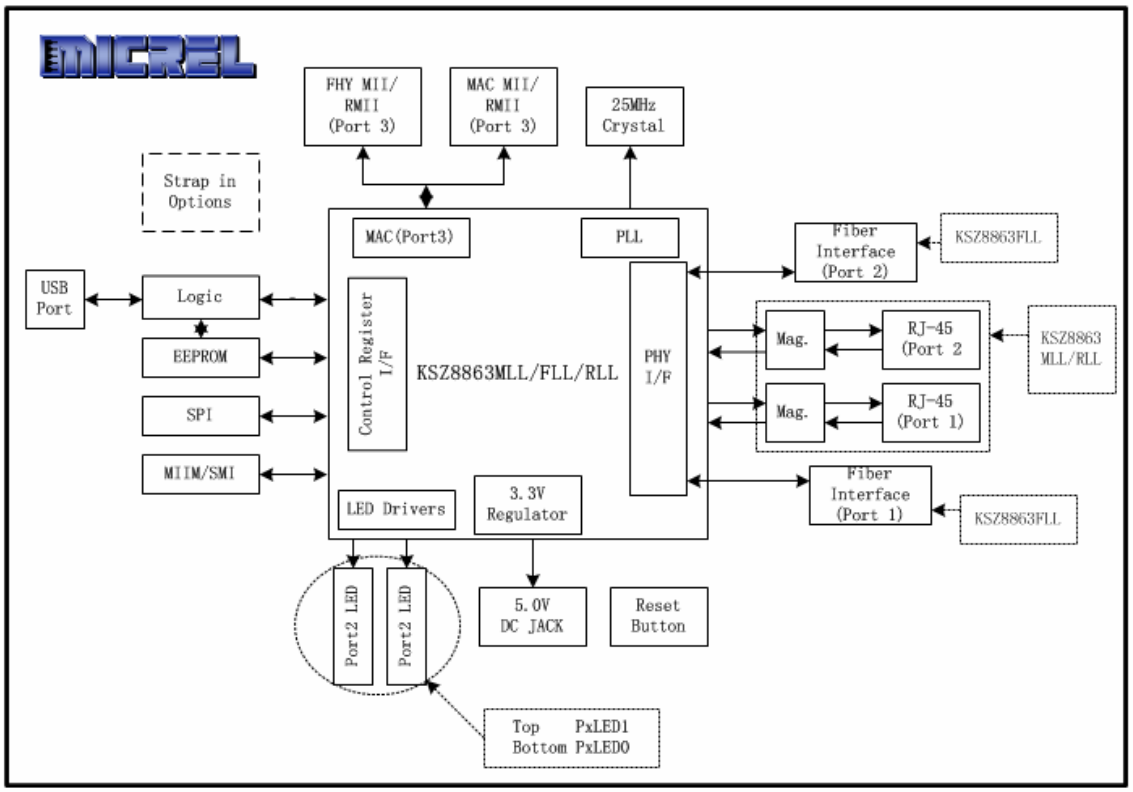

Figure 1: KSZ8863MLL/FLL/RLL Evaluation Board Block Diagram

The KSZ8863MLL/FLL/RLL evaluation board is easy to use. There are programmable LED indicators for link and activity on the PHY ports and a power LED. A manual reset button allows the user to reset the board without removing the power plug. The 5V power on the board can be supplied by a standard 5VDC power supply (close pin 1-2 of JP400 jumper) or by the USB cable (close pin 2-3 of JP400 jumper) which is used to access the registers in SPI mode. A standard 5VDC power supply is included so that the user can supply power from any 110 Volt AC wall or bench socket. Before to start to use the evaluation board, make sure the power connectors JP403, JP404, JP405, JP406 and JP31 are connected, and close pin 1-2 of J14.

4.1 Strap in Mode

Strap in configuration mode is the quickest and easiest way to get started. In this mode, the KSZ8863MLL/FLL/RLL acts as a standalone 3-port switch. Simply set the board's configuration jumpers to the desired settings and apply power to the board. The configuration can be changed while power is applied to the board by changing the jumper settings and pressing the convenient manual reset button for the new settings to take effect. Note that even if no external strap in values are set, internal pull up and pull down resistors will set the KSZ8863MLL/FLL/RLL default configuration. Section 4.1.1 covers each jumper on the board and describes its function. To start in strap in configuration mode, make sure that the USB cable is unplugged, JP34, JP35, JP3 and JP9 are connected, JP21, JP25 have jumpers fitted between pins 2 to 3.

4.1.1 Feature Setting Jumpers

The evaluation board provides jumpers to allow easy setting of strap in configurations for the KSZ8863MLL/FLL/RLL. Table 1 describes the jumpers and their functionalities.

Table 1: Feature Setting Jumpers

JUMPER	KSZ8863MLL/FLL/RLL SIGNAL	OPEN	CLOSED
JP3	SPIQ	SPI	EEPROM
JP25	P2LED0	EEPROM/SPI Setting. See Section 4.2 and 4.3	
JP21	P2LED1	EEPROM/SPI Setting. See Section 4.2 and 4.3	
JP78	FXSD1	Pins 1-2 closed : Disable FEF feature of FX. Pins 5-6 closed : Force port 1 TX mode For KSZ8863MLL/RLL, close 5-6 since this device doesn't support FX mode. For KSZ8863FLL, open JP77	
JP77	FXSD2	Pins 1-2 closed : Disable FEF feature of FX. Pins 5-6 closed : Force port 1 TX mode For KSZ8863MLL/RLL, close 5-6 since this device doesn't support FX mode. For KSZ8863FLL, open JP77	
JP2	PWRDN	Normal Operation	KSZ8863MLL/FLL/RLL Chip Power Down
JP101	SPIQ (P1FFC)	Pull Down = Disable Pull Up(default) = Enable	
JP102	SMRXDV3(P1DPX)	Pull Down = Half Duplex Pull Up(default) = Full Duplex	
JP103	P1LED1(P1SPD)	Pull Down = 10BT Pull Up(default) = 100BT	
JP104	P1LED0(P1ANEN)	Pull Down(default) = Disable Pull Up = Enable	
JP201	SMRXD30(P2FFC)	Pull Down = Disable Pull Up(default) = Enable	
JP202	SMRXD31(P2DPX)	Pull Down = Half Duplex Pull Up(default) = Full Duplex	
JP203	SMRXD32(P2SPD)	Pull Down = 10BT Pull Up(default) = 100BT	
JP204	SMRXD33(P2ANEN)	Pull Down = Disable Pull Up(default) = Enable	

Note: JP101, JP102, JP103, JP201, JP202, JP203 are only valid if Auto-Negotiation is disabled.

The following table shows the recommended settings for the evaluation board reserved jumpers.

Table 2: Reserved Jumpers

JUMPER	Description	Recommended Setting
JP79	MDC_PHY,MDIO_PHY	Open
JP27	P3 MII configuration (For test only)	Open

JUMPER	Description	Recommended Setting
JP30	3.3V Biased of transformer Center (For test only)	Open
JP11	Power for Fiber Module. (Port 2)	KSZ8863MLL/RLL: Open For KSZ8863FLL: Close pin 1-2 for 3.3V Fiber Module. Close pin 3-2 for 5.0V Fiber Module.
JP10	Power for Fiber Module. (Port 1)	KSZ8863MLL/RLL: Open For KSZ8863FLL: Close pin 1-2 for 3.3V Fiber Module. Close pin 3-2 for 5.0V Fiber Module.
JP28	REFCLKO3 enable.	KSZ8863MLL/FLL: Open KSZ8863RLL: Close pin 1-2: Enable REFCLKO Close pin 2-3: Disable REFCLKO

4.2 I2C Master (EEPROM) Mode

The evaluation board has an EEPROM to allow the user to explore more extensive capabilities of the KSZ8863MLL/FLL/RLL. The user can conveniently program the EEPROM on board using the USB port from any computer with a WIN 2000/XP environment and the Micrel provided software. This makes it easy for the user to evaluate features like "broadcast storm protection" and "rate control".

To prepare the KSZ8863MLL/FLL/RLL evaluation board for EEPROM configuration follow these steps:

1. Install the Micrel Switch Configuration Software to your computer.
2. Set JP3, JP9, JP21, JP25, JP34 and JP35 as specified in Table 3 for EEPROM mode configuration. Make sure that the EEPROM is installed on the board.
3. Connect the computer's USB port to the KSZ8863MLL/FLL/RLL board with a USB port cable.
4. There are two way to power up the evaluation board:
   a). Connect the 5 VDC power supply to the KSZ8863MLL/FLL/RLL when JP400 pin1-2 is closed.
   b). 5 VDC power source from the USB port when JP400 pin 2-3 is closed.
5. The KSZ8863MLL/FLL/RLL will power up in its default configuration if there is no information in the EEPROM.
6. Click the software icon to invoke the software to program the desired settings into the EEPROM. See the Micrel Switch Configuration Software User Guide for details.
7. Press the manual reset button. The KSZ8863MLL/FLL/RLL will reset and read the new configuration in the EEPROM. After reset, the KSZ8863MLL/FLL/RLL is ready for normal operation.

Table 3: EEPROM Mode Settings

Jumper	Description	Setting
JP9	SPIQ	Closed
JP3	SCL_MDC_SW	Closed
JP34	SCL_MDC	Closed
JP35	SDA_MDIO	Closed
JP25	Serial Bus Config. (P2LED0)	Pins 2-3 closed
JP21	Serial Bus Config. (P2LED1)	Pins 2-3 closed

4.3 SPI Slave Mode

From SPI interface to the KSZ8863MLL/FLL/RLL, use a USB to SPI converter that allows accessing all of the KSZ8863MLL/FLL/RLL features and registers. The user can easily access the SPI interface using a computer connected to the evaluation board's USB port interface. Micrel provides a Windows 2000/XP based program for the user to evaluate the KSZ8863MLL/FLL/RLL's full feature set. In addition to all the registers available via EEPROM programming, a host CPU connected to the KSZ8863MLL/FLL/RLL's SPI interface will be able to access all static MAC entries, the VLAN table, dynamic MAC address table and the MIB counters.

To prepare the KSZ8863MLL/FLL/RLL evaluation board for SPI mode configuration follow these steps:

1. Install the Micrel Switch Configuration Software on your computer.
2. Set JP3, JP9, JP21, JP25, JP34 and JP35 as specified in Table 4 for SPI mode configuration.

Table 4: SPI Slave Mode Settings

Jumper	Description	Setting
JP9	SPIQ	Open
JP3	SCL_MDC_SW	Open
JP34	SCL_MDC	Closed
JP35	SDA_MDIO	Closed
JP25	Serial Bus Config. (P2LED0)	Pins 2-3 closed
JP21	Serial Bus Config. (P2LED1)	Pins 1-2 closed

3. Connect the computer's USB port to the KSZ8863MLL/FLL/RLL board with a USB port cable.
4. There are two way to power up the evaluation board:
   a). Connect the 5 VDC power supply to the KSZ8863MLL/FLL/RLL when JP400 pin1-2 is closed.
   b). 5 VDC power source from the USB port when JP400 pin 2-3 is closed.
5. The KSZ8863MLL/FLL/RLL will power up in its default configuration
6. Click the software icon to invoke the software to program the desired settings.

See the Micrel Switch Configuration Software User Guide for details.

4.4 10/100 Ethernet PHY Ports (KSZ8863MLL/RLL)

There are two 10/100 Ethernet PHY ports on the KSZ8863MLL/RLL evaluation board. The ports can be connected to an Ethernet traffic generator or analyzer via standard RJ-45 connectors using CAT-5 cables. Each port can be used as either an uplink or downlink. Both ports support auto MDI/MDI-X, eliminating the need for cross over cables.

4.5 100FX Fiber Port (KSZ8863FLL)

There are two 100FX PHY ports on the KSZ8863FLL evaluation board. The ports can be connected to an Ethernet traffic generator or analyzer via fiber transceiver and fiber cable. The fiber signal threshold can be set by register 192 bit 6(Port1) and bit 7(Port2). If the bits are 1, the threshold will be set to 2.0V, Otherwise it is 1.25V.The resister R76 also need to be adjusted if the FXSD signal value from the fiber module doesn't meet the fiber signal threshold spec.

4.6 LED Indicators

There is one column of LED indicator for one column for port 2. The LED indicators are programmable to three different modes. LED mode is selected through register 195 bit [5:4] setting. The LED mode definitions are specified in Table 5. See Figure 1 for the LEDs' orientation on the KSZ8863MLL/FLL/RLL evaluation board.

Table 5: LED Modes

Register 195 Bit[5:4]			
00	**01**	**10**	**11**
PxLED1 = Speed	PxLED1 = Active	PxLED1 = Duplex	PxLED1 = Duplex
PxLED0 = Link/Active	PxLED0 = Link	PxLED0 = Link/Active	PxLED0 = Link

The KSZ8863MLL/FLL/RLL evaluation board provides two LEDs (PxLED1, PxLED0) for each PHY port.

The KSZ8863MLL/FLL/RLL evaluation board also has a power LED (D3) for the 3.3V power supply. When D3 is lit, the board's 3.3V power supply is "on".

4.7 MII Port Configuration (KSZ8863MLL/FLL)

The evaluation board provides access to the KSZ8863MLL/FLL/RLL's third MAC via the MII port interfaces. The MAC can be configured to MII PHY mode and MII MAC mode via register 53 bit 7. The default of the bit is 0 for MII PHY mode.

In MII PHY mode, the MII transmit and receive signals will be on J3, the male MII port connectors. This mode is usually used to connect the KSZ8863MLL/FLL/RLL to an external MAC processor. In MII MAC mode, the MII transmit and receive signals will be on J4, the female MII port connector. This interface is normally used to connect the KSZ8863MLL/FLL/RLL to an external PHY, for example the Micrel KSZ8041NL.

4.8 RMII Port Configuration (KSZ8863RLL)

In RMII interface, the 50MHz reference clock can be provide by the KSZ8863RLL or by the link partner. When pin 1-2 of JP28 is closed, the reference clock will be output from REFCLKO on

KSZ8863RLL. Register 198 bit[3] is used to select internal or external reference clock for the KSZ8863RLL RMII interface. If pin 2-3 of JP28 is closed, the REFCLKO disable.

Table 6: RMII Clock Setting

Reg198[3]	EN_REFCLKO_3	Clock Source	Note
0	0	External 50MHz OSC input to REFCLKI_3	EN_REFCLKO_3 = 0 to Disable REFCLKO_3 for better EMI
0	1	REFCLKO_3 Output Is Feedback to REFCLKI_3	EN_REFCLKO_3 = 1 to Enable REFCLKO_3
1	1	Internal Clock Source REFCLKI_3 is unconnected	EN_REFCLKO_3 = 1 to Enable REFCLKO_3
1	0		Not suggest

5.0 Reference Documents

KSZ8863MLL/FLL/RLL Datasheet Rev. 1.1 (Contact Micrel for latest Datasheet)
KSZ8863MLL/FLL/RLL Evaluation Board Schematic Rev. 1.0 (Contact Micrel for latest Schematic)
KSZ8863MLL/FLL/RLL Evaluation Board Gerber files
Micrel Switch Configuration Software User Guide