μPower, 3V, 16-Bit, 150ksps 1- and 2-Channel ADCs in MSOP

FEATURES

- **16-Bit 150ksps ADCs in MSOP Package**
- Single 3V Supply
- Low Supply Current: 450μA (Typ)
- Auto Shutdown Reduces Supply Current to 10μA at 1ksps
- True Differential Inputs
- 1-Channel (LTC1864L) or 2-Channel (LTC1865L) Versions
- SPI/MICROWIRE™ Compatible Serial I/O
- 16-Bit Upgrade to 12-Bit LTC1285/LTC1288
- Pin Compatible with 12-Bit LTC1860L/LTC1861L
- No Minimum Data Transfer Rate

APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

DESCRIPTION

The LTC®1864L/LTC1865L are 16-bit A/D converters that are offered in MSOP and SO-8 packages and operate on a single 3V supply. At 150ksps, the supply current is only 450μA. The supply current drops at lower speeds because the LTC1864L/LTC1865L automatically power down between conversions. These 16-bit switched capacitor successive approximation ADCs include sample-and-holds. The LTC1864L has a differential analog input with an external reference pin. The LTC1865L offers a software-selectable 2-channel MUX and an external reference pin on the MSOP version.

The 3-wire, serial I/O, small MSOP or SO-8 package and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

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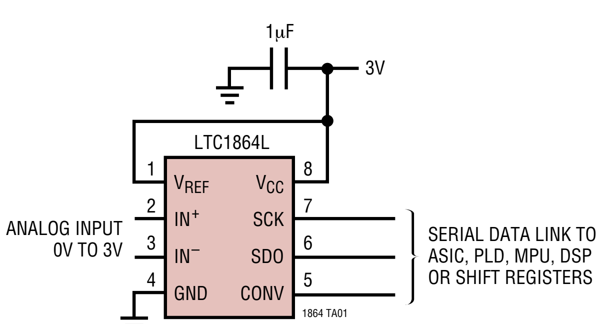
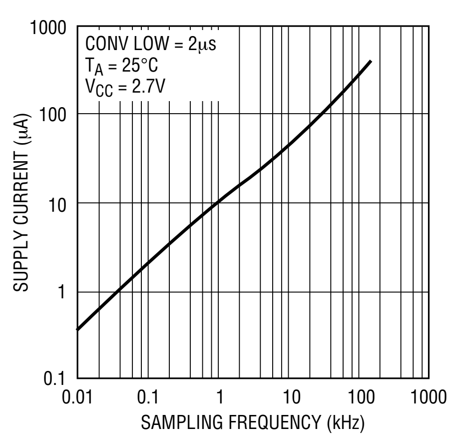
MICROWIRE is a trademark of National Semiconductor Corporation.

TYPICAL APPLICATION

Single 3V Supply, 150ksps, 16-Bit Sampling ADC



Supply Current vs Sampling Frequency



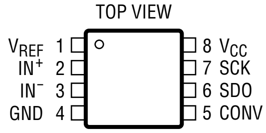
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Ground Voltage Difference
AGND, DGND LTC1865L MSOP Package .... ±0.3V
Analog Input .... (GND – 0.3V) to (V_{CC} + 0.3V)
Digital Input .... (GND – 0.3V) to 7V
Digital Output .... (GND – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 400mW

Operating Temperature Range
LTC1864LC/LTC1865LC/
LTC1864LAC/LTC1865LAC .... 0°C to 70°C
LTC1864LI/LTC1865LI/
LTC1864LAI/LTC1865LAI .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

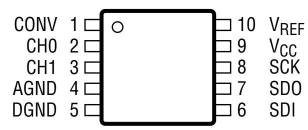
TOP VIEW



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 210°C/W

ORDER PART NUMBER
LTC1864LCMS8
LTC1864LIMS8
LTC1864LACMS8
LTC1864LAIMS8
MS8 PART MARKING
LTC7

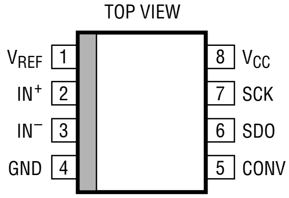
TOP VIEW



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 210°C/W

ORDER PART NUMBER
LTC1865LCMS
LTC1865LIMS
LTC1865LACMS
LTC1865LAIMS
MS PART MARKING
LTJ4

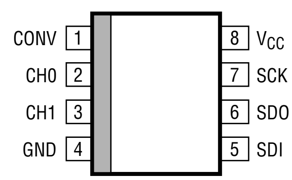
TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER	
LTC1864LCS8	
LTC1864LIS8	
LTC1864LACS8	
LTC1864LAIS8	
S8 PART MARKING	
1864L	1864LA
1864LI	864LAI

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER	
LTC1865LCS8	
LTC1865LIS8	
LTC1865LACS8	
LTC1865LAIS8	
S8 PART MARKING	
1865L	1865LA
1865LI	865LAI

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1864L/LTC1865L MIN	TYP	MAX	LTC1864LA/LTC1865LA MIN	TYP	MAX	UNITS
Resolution		●	16			16			Bits
No Missing Codes Resolution		●	14			15			Bits
INL	(Note 3)	●			±8			±6	LSB
Transition Noise				2			2		LSB_{RMS}
Gain Error		●			±20			±20	mV

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1864L/LTC1865L MIN	TYP	MAX	LTC1864LA/LTC1865LA MIN	TYP	MAX	UNITS
Offset Error		●		±2	±5		±2	±5	mV
Input Differential Voltage Range	V_{IN} = $IN^+ – IN^–$	●	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	IN^+ Input $IN^–$ Input		–0.05 –0.05		V_{CC} + 0.05 $V_{CC}/2$	–0.05 –0.05		V_{CC} + 0.05 $V_{CC}/2$	V V
V_{REF} Input Range	LTC1864L SO-8 and MSOP, LTC1865L MSOP		1		V_{CC}	1		V_{CC}	V
Analog Input Leakage Current	(Note 4)	●			±1			±1	µA
C_{IN} Input Capacitance	In Sample Mode During Conversion			12 5			12 5		pF pF

DYNAMIC ACCURACY

T_A = 25°C. V_{CC} = 3V, V_{REF} = 3V, f_{SAMPLE} = 150kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1864L/LTC1865L MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio			82		dB
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		82		dB
THD	Total Hamonic Distortion Up to 5th Harmonic	1kHz Input Signal		92		dB
	Full Power Bandwidth			10		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 75dB		20		kHz

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITION		LTC1864L/LTC1865L MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.45	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.3 2.1	2.6 2.45		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage	CONV = V_{CC}	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–6.5		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			6.5		mA
I_{REF}	Reference Current (LTC1864L SO-8 and MSOP, LTC1865L MSOP)	CONV = V_{CC} f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.001 0.01	3 0.1	µA mA
I_{CC}	Supply Current	CONV = V_{CC} After Conversion f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.5 0.45	10 1.0	µA mA
P_D	Power Dissipation	f_{SMPL} = $f_{SMPL(MAX)}$			1.22		mW

RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC1864L/LTC1865L MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7		3.6	V
f_{SCK}	Clock Frequency		●	DC		8	MHz
t_{CYC}	Total Cycle Time			16 • SCK + t_{CONV}			µs
t_{SMPL}	Analog Input Sampling Time (Note 5)	LTC1864L LTC1865L		16 14			SCK SCK
t_{suCONV}	Setup Time CONV↓ Before First SCK↑ (See Figure 1)			60			ns
t_{hDI}	Hold Time SDI After SCK↑	LTC1865L		30			ns
t_{suDI}	Setup Time SDI Stable Before SCK↑	LTC1865L		30			ns
t_{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$		45%			$1/f_{SCK}$
t_{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$		45%			$1/f_{SCK}$
t_{WHCONV}	CONV High Time Between Data Transfer Cycles			t_{CONV}			µs
t_{WLCONV}	CONV Low Time During Data Transfer			16			SCK
t_{hCONV}	Hold Time CONV Low After Last SCK↑			26			ns

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, $f_{SCK} = f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1864L/LTC1865L MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time (See Figure 1)		●		3.7	4.66	µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	150			kHz
t_{dDO}	Delay Time, SCK↓ to SDO Data Valid	C_{LOAD} = 20pF	 ●		45	55 60	ns ns
t_{dis}	Delay Time, CONV↑ to SDO Hi-Z		●		55	120	ns
t_{en}	Delay Time, CONV↓ to SDO Enabled	C_{LOAD} = 20pF	●		35	120	ns
t_{hDO}	Time Output Data Remains Valid After SCK↓	C_{LOAD} = 20pF	●	5	15		ns
t_r	SDO Rise Time	C_{LOAD} = 20pF			25		ns
t_f	SDO Fall Time	C_{LOAD} = 20pF			12		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

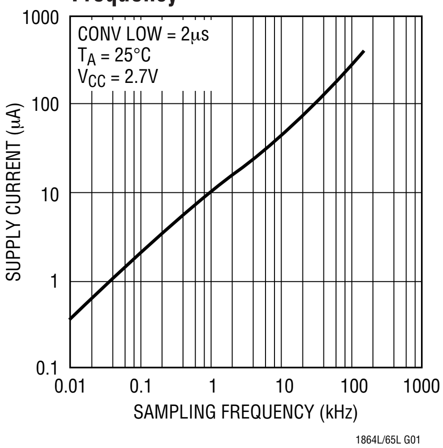
Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Channel leakage current is measured while the part is in sample mode.

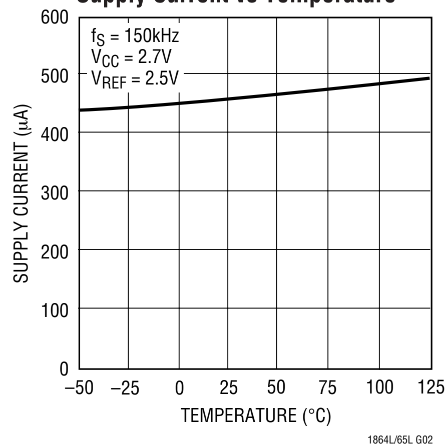
Note 5: Assumes $f_{SCK} = f_{SCK(MAX)}$ In the case of the LTC1864L SCK does not have to be clocked during this time if the SDO data word is not desired. In the case of the LTC1865L a minimum of 2 clocks are required on the SCK input after CONV falls to configure the MUX during this time.

TYPICAL PERFORMANCE CHARACTERISTICS

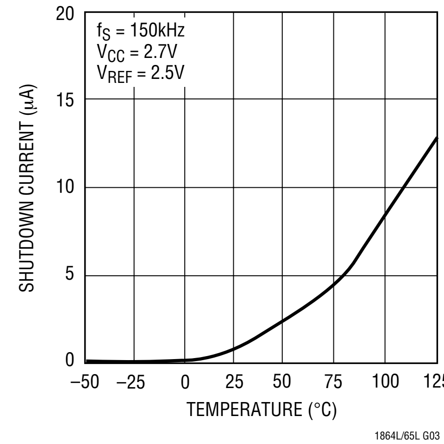
Supply Current vs Sampling Frequency



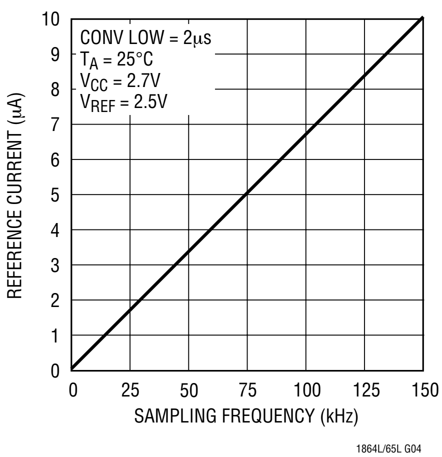
Supply Current vs Temperature



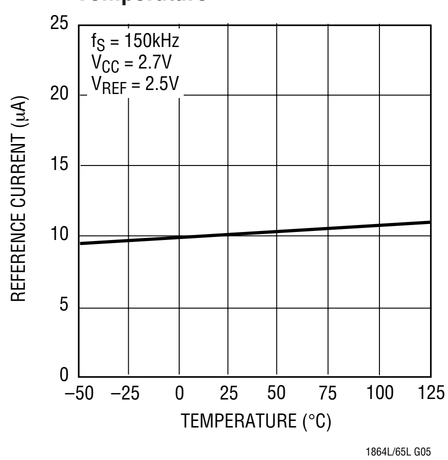
Sleep Current vs Temperature



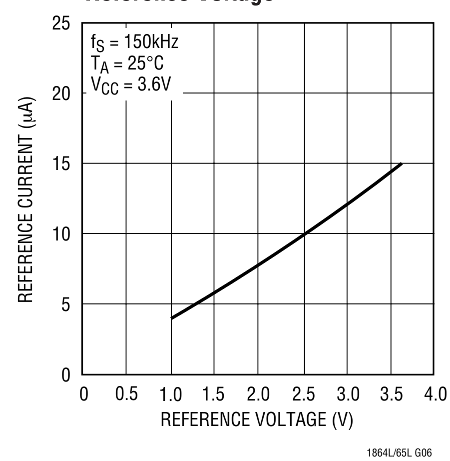
Reference Current vs Sampling Rate



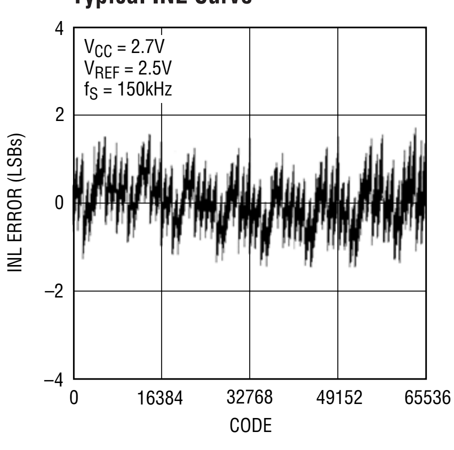
Reference Current vs Temperature



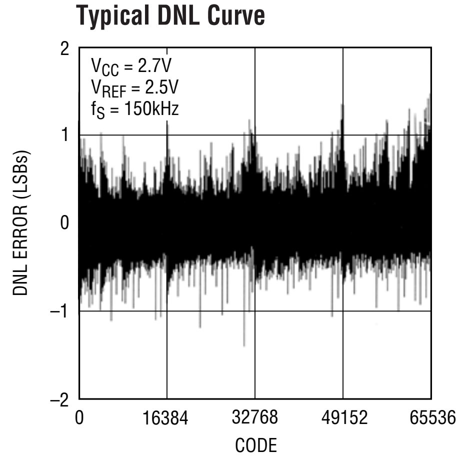
Reference Current vs Reference Voltage



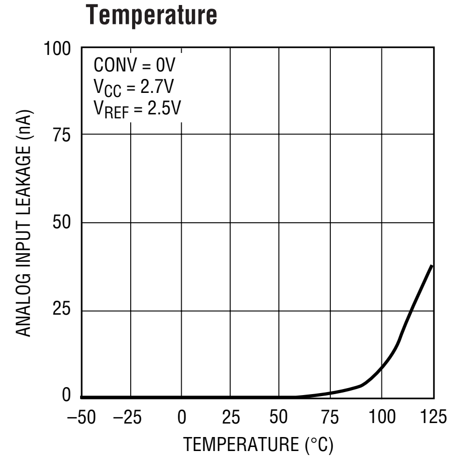
Typical INL Curve



Typical DNL Curve

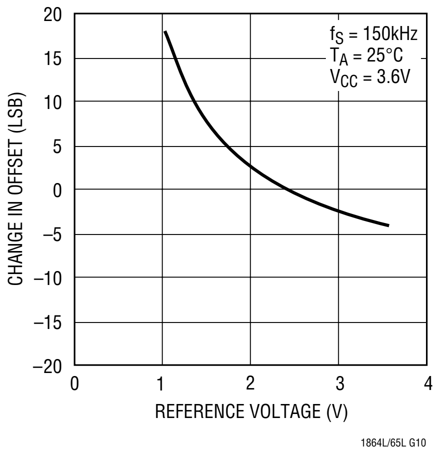


Analog Input Leakage Current vs Temperature

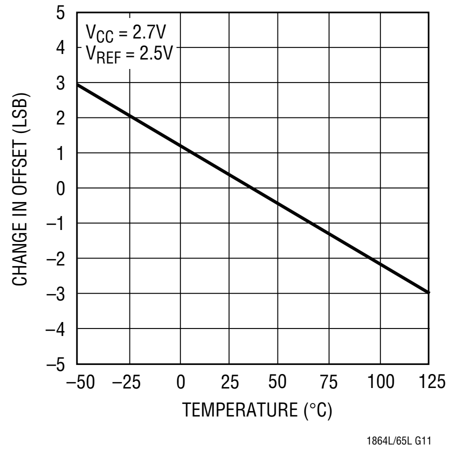


TYPICAL PERFORMANCE CHARACTERISTICS

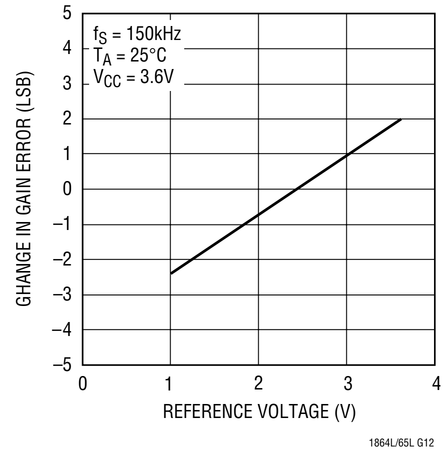
Change in Offset vs Reference Voltage



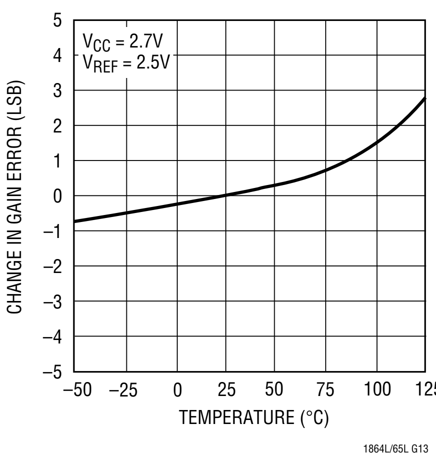
Change in Offset vs Temperature



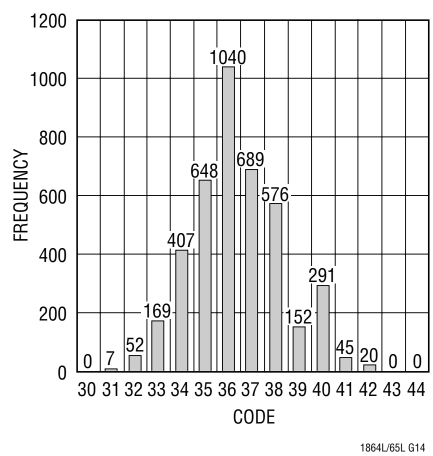
Change in Gain Error vs Reference Voltage



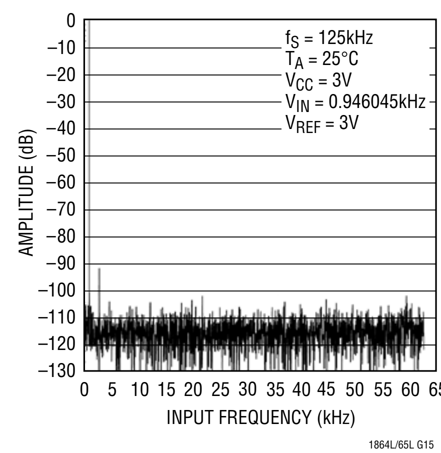
Change in Gain Error vs Temperature



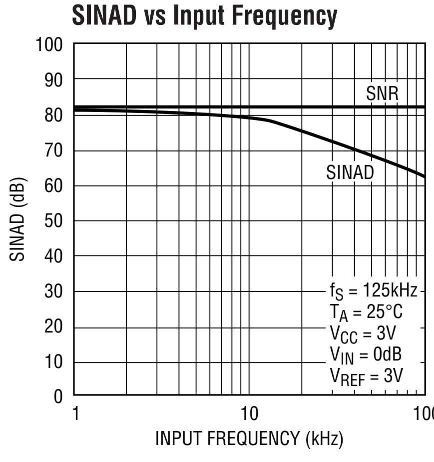
Histogram of 4096 Conversions of a DC Input Voltage



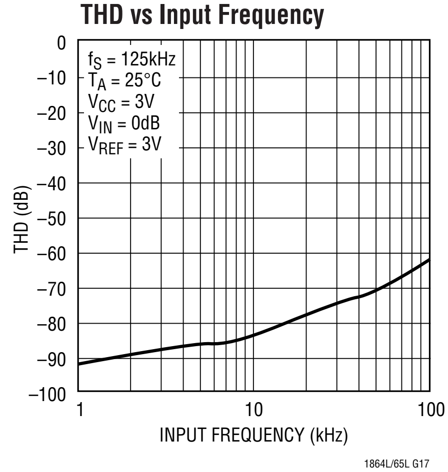
4096 Point FFT Nonaveraged



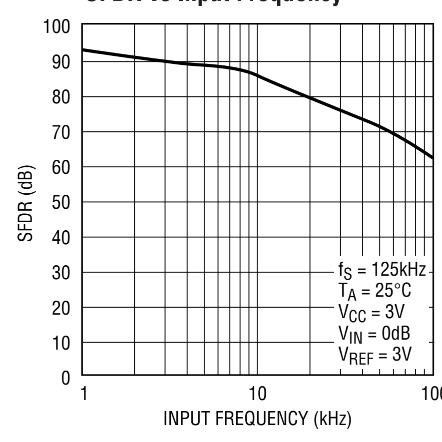
SINAD vs Input Frequency



THD vs Input Frequency



SFDR vs Input Frequency



PIN FUNCTIONS

LTC1864L

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN^+, IN^- (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1865L (MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{REF} (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

LTC1865L (SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

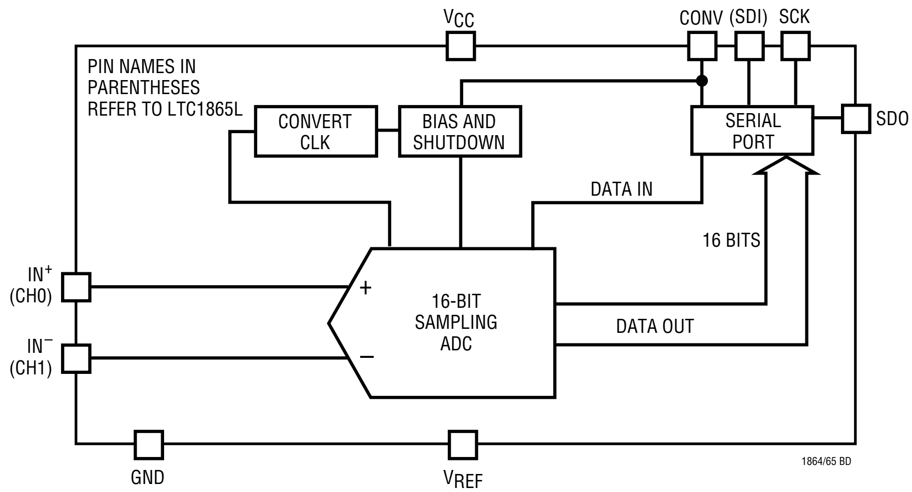
SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

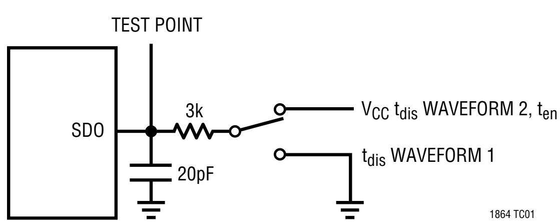
V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V_{REF} is tied internally to this pin.

FUNCTIONAL BLOCK DIAGRAM

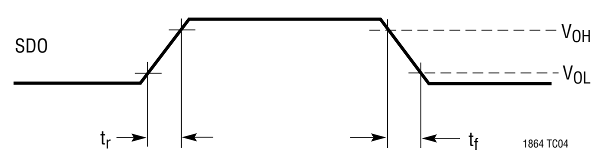


TEST CIRCUITS

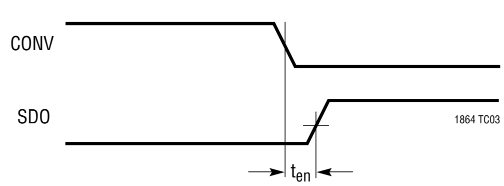
Load Circuit for t_{dDO}, t_r, t_f, t_{dis} and t_{en}



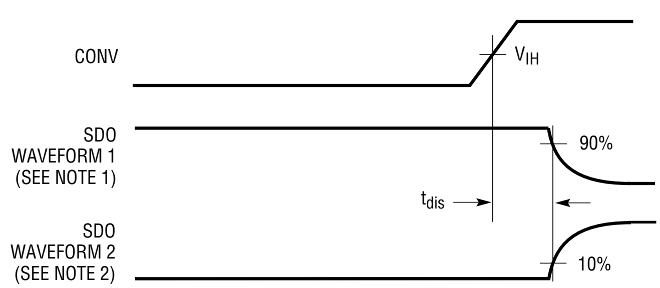
Voltage Waveforms for SDO Rise and Fall Times, t_r, t_f



Voltage Waveforms for t_{en}



Voltage Waveforms for t_{dis}

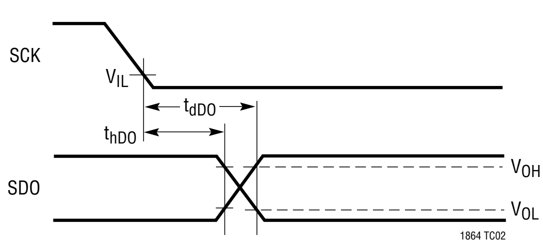


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

1864 TC05

Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



APPLICATIONS INFORMATION

LTC1864L OPERATION

Operating Sequence

The LTC1864L conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1864L goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1864L goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1864L has a unipolar differential analog input. The converter will measure the voltage between the "IN^+" and "IN^-" inputs. A zero code will occur when IN^+ minus IN^- equals zero. Full scale occurs when IN^+ minus IN^- equals V_{REF} minus 1LSB. See Figure 2. Both the "IN^+" and "IN^-" inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If "IN^-" is grounded and V_{REF} is tied to V_{CC}, a rail-to-rail input span will result on "IN^+" as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1864L defines the full-scale range of the A/D converter. The LTC1864L can operate with reference voltages from V_{CC} to 1V.

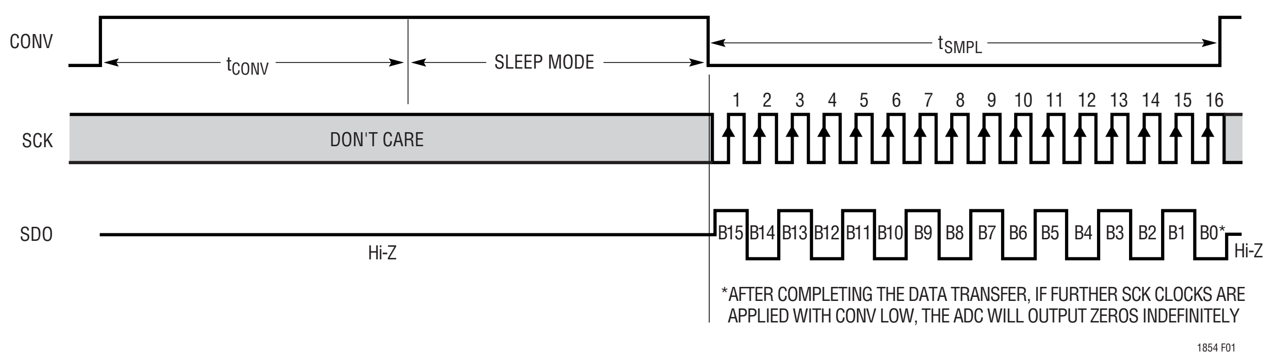


Figure 1. LTC1864L Operating Sequence

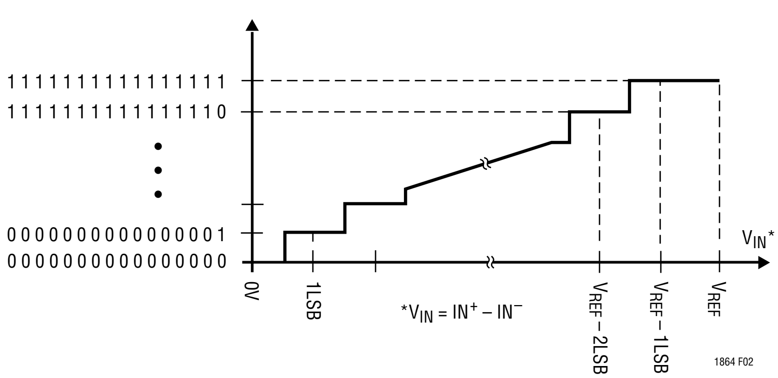


Figure 2. LTC1864L Transfer Curve

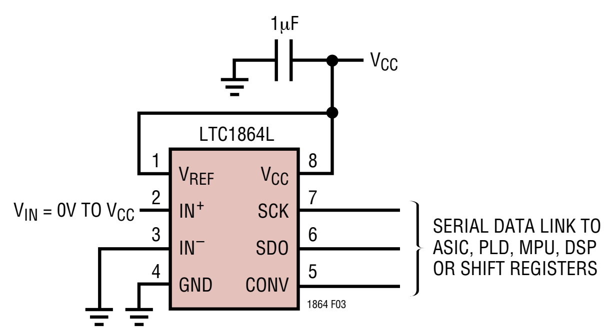


Figure 3. LTC1864L with Rail-to-Rail Input Span

APPLICATIONS INFORMATION

LTC1865L OPERATION

Operating Sequence

The LTC1865L conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1865L goes into sleep mode drawing only leakage current. The LTC1865L's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of Table 1. In single-ended mode, all input channels are measured with respect to GND. A zero code will occur when the "+" input minus the "–" input equals zero. Full scale occurs when the "+" input minus the "–" input equals V_{REF} minus 1LSB. See Figure 5. Both the "+" and "–" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at $V_{REF} = V_{CC}$. If the "–" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

Reference Input

The reference input of the LTC1865L SO-8 package is internally tied to V_{CC}. The span of the A/D converter is therefore equal to V_{CC}. The voltage on the reference input of the LTC1865L MSOP package defines the span of the A/D converter. The LTC1865L MSOP package can operate with reference voltages from 1V to V_{CC}.

Table 1. Multiplexer Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

1864 TBL1

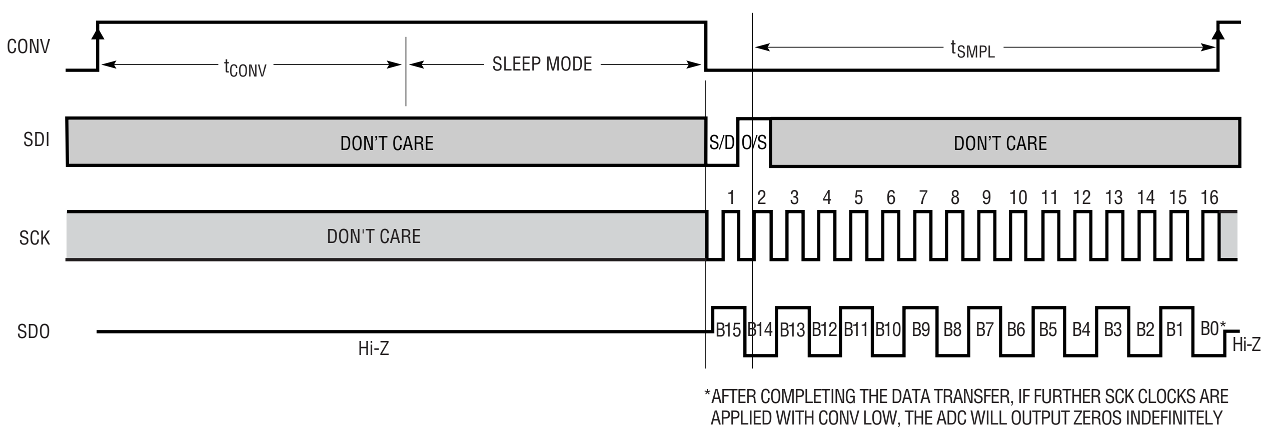


Figure 4. LTC1865L Operating Sequence

APPLICATIONS INFORMATION

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1864L/LTC1865L should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1865L MSOP package and GND for the LTC1864L and LTC1865L SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of 1μF tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1864L/LTC1865L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200Ω or high speed op amps are used (e.g., the LT®1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

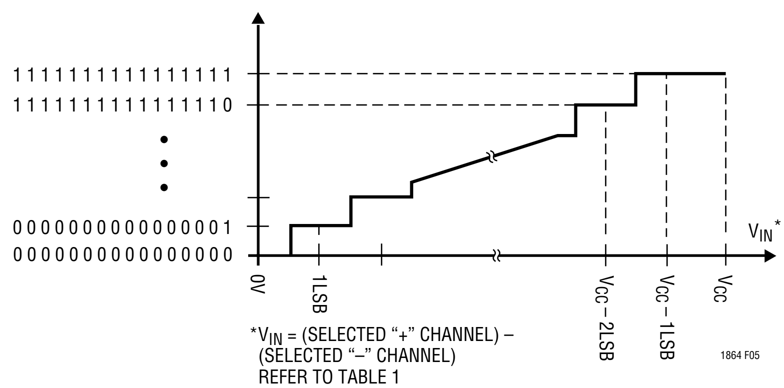
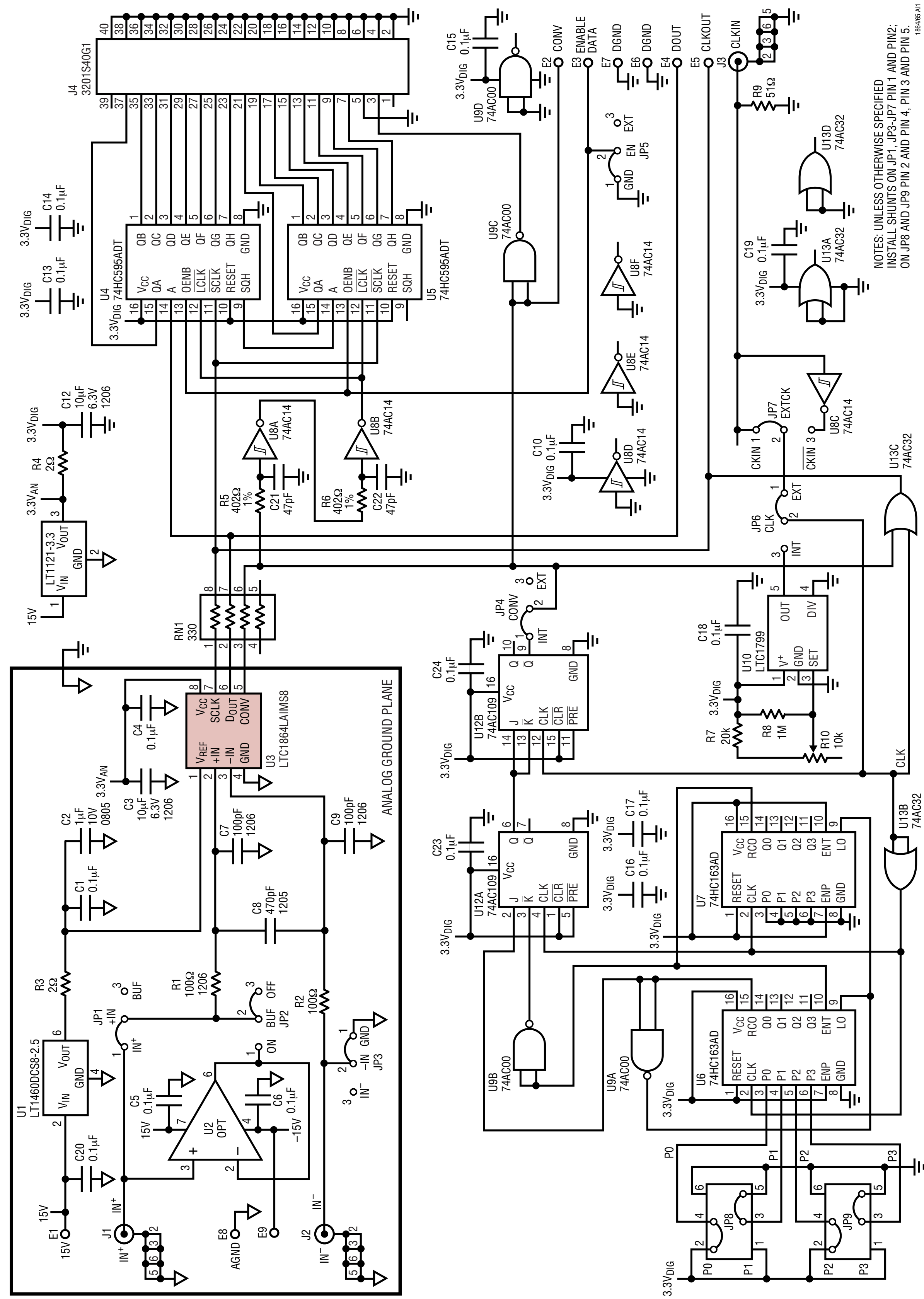


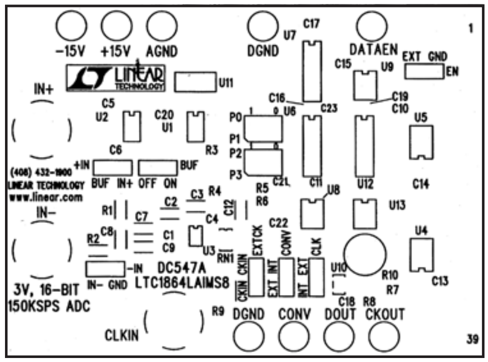
Figure 5. LTC1865L Transfer Curve

APPLICATIONS INFORMATION

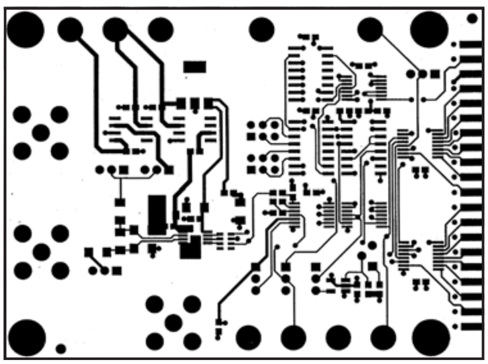
LTC1864L Evaluation Circuit Schematic



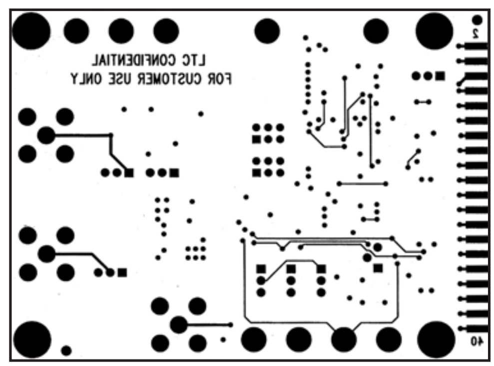
APPLICATIONS INFORMATION



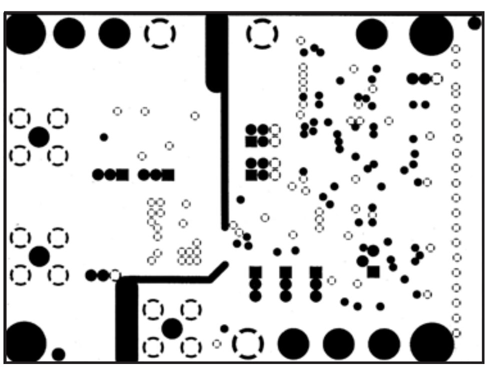
Component Side Silk Screen for LTC1864L Evaluation Circuit



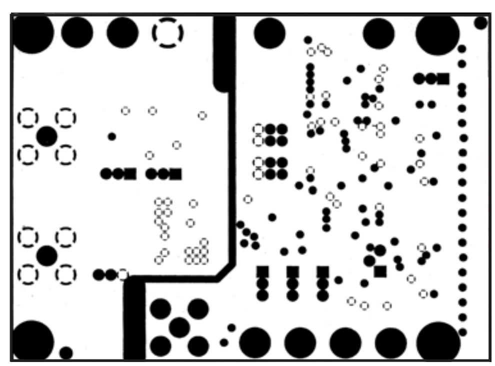
Component Side Showing Traces
(Note Wider Traces on Analog Side)



Bottom Side Showing Traces
(Note Almost No Analog Traces on Board Bottom)



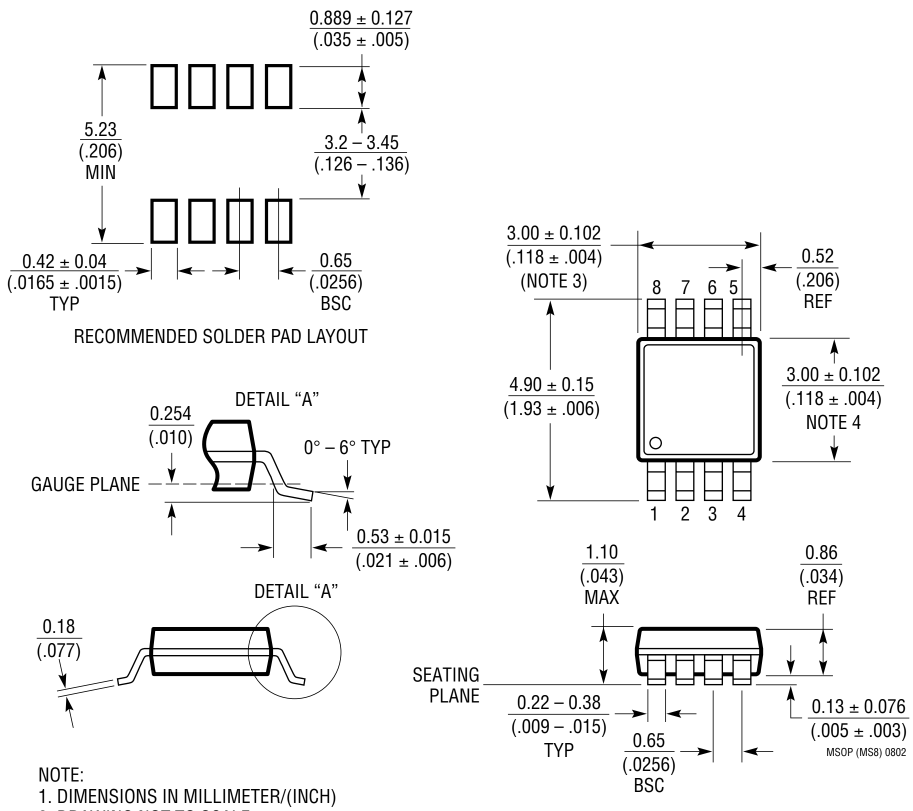
Ground Layer with Separate Analog and Digital Grounds



Supply Layer with 5V Digital Supply and Analog Ground Repeated

PACKAGE DESCRIPTION

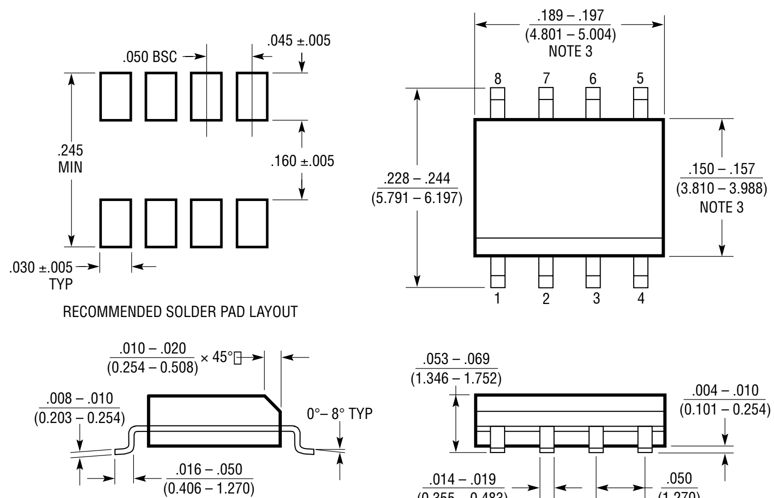
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

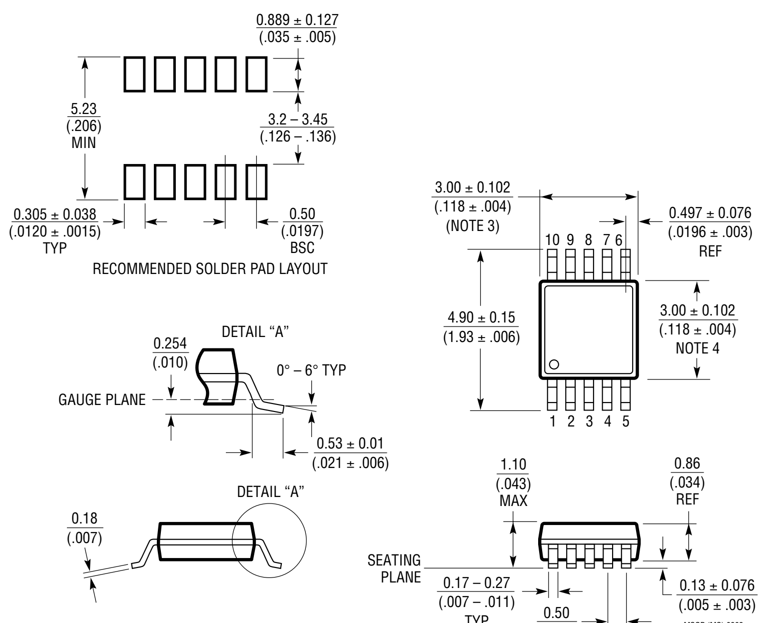
S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)

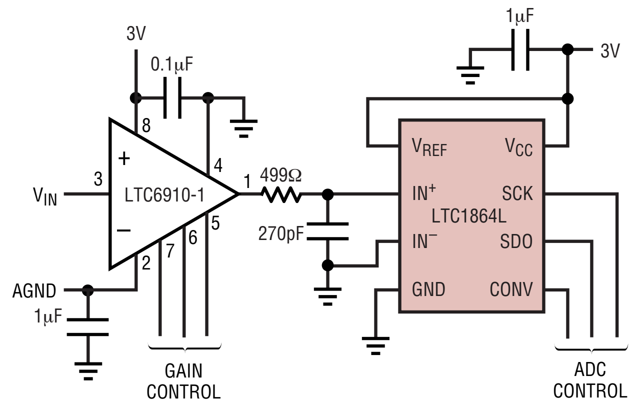


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Tiny 2-Chip Data Acquisition System



LTC6910-1 (IN TSOT-23 PACKAGE) COMPACTLY ADDS 40dB OF INPUT GAIN RANGE TO THE LTC1864L (IN MSOP 8-PIN PACKAGE). SINGLE 3V SUPPLY

1864L/65L TA03

RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
12-Bit Serial I/O ADCs			
LTC1860L/LTC1861L	150ksps	1.22mW	Pin Compatible with LTC1864L/LTC1865L
LTC1860/LTC1861	250ksps	4.25mW	Pin Compatible with LTC1864/LTC1865
14-Bit Serial I/O ADCs			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V or ±5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V or ±5V
16-Bit Serial I/O ADCs			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
LTC1864/LTC1865	250ksps	4.25mW	MSOP, SO-8, 1- and 2-Channel, 5V Supply
References			
LT1460	Micropower Precision Series Reference		Bandgap, 130μA Supply Current, 10ppm/°C, Available in SOT-23
LT1790	Micropower Low Dropout Reference		60μA Supply Current, 10ppm/°C, SOT-23
Op Amps			
LT1468/LT1469	Single/Dual 90MHz, 16-Bit Accurate Op Amps		22V/μs Slew Rate, 75μV/125μV Offset
LT1806/LT1807	Single/Dual 325MHz Low Noise Op Amps		140V/μs Slew Rate, 3.5nV/$\sqrt{Hz}$ Noise, −80dBc Distortion
LT1809/LT1810	Single/Dual 180MHz Low Distortion Op Amps		350V/μs Slew Rate, −90dBc Distortion at 5MHz

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