

MC74VHC1G125

Noninverting 3-State Buffer

The MC74VHC1G125 is an advanced high speed CMOS noninverting 3-state buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered 3-state output which provides high noise immunity and stable output.

The MC74VHC1G125 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1G125 to be used to interface 5 V circuits to 3 V circuits.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 58; Equivalent Gates = 15
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

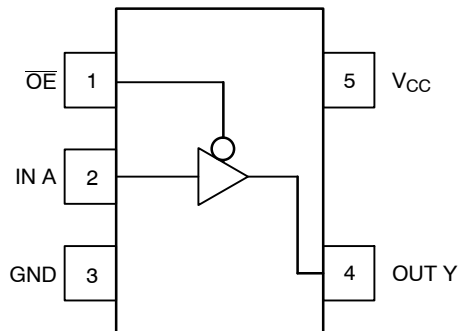


Figure 1. Pinout (Top View)

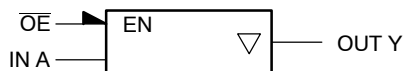


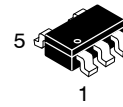
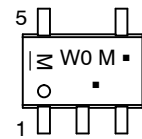
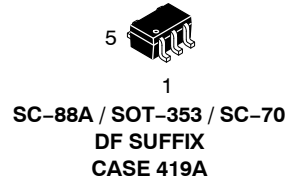
Figure 2. Logic Symbol



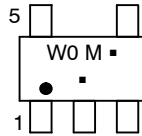
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MARKING DIAGRAMS



TSOP-5 / SOT-23 / SC-59
DT SUFFIX
CASE 483



WO = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

| Pin | Function |
|-----|----------|
| 1 | OE |
| 2 | IN A |
| 3 | GND |
| 4 | OUT Y |
| 5 | VCC |

FUNCTION TABLE

| A Input | OE Input | Y Output |
|---------|----------|----------|
| L | L | L |
| H | L | H |
| X | H | Z |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1G125

MAXIMUM RATINGS

| Symbol | Characteristics | Value | Unit |
|---------------|---|---------------------------------------|------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage | -0.5 to +7.0 | V |
| V_{OUT} | DC Output Voltage $V_{CC} = 0$ High or Low State | -0.5 to 7.0 -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | Input Diode Current | -20 | mA |
| I_{OK} | Output Diode Current $V_{OUT} < GND; V_{OUT} > V_{CC}$ | +20 | mA |
| I_{OUT} | DC Output Current, per Pin | +25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND | +50 | mA |
| P_D | Power Dissipation in Still Air SC-88A, TSOP-5 | 200 | mW |
| θ_{JA} | Thermal Resistance SC-88A, TSOP-5 | 333 | °C/W |
| T_L | Lead Temperature, 1 mm from Case for 10 secs | 260 | °C |
| T_J | Junction Temperature Under Bias | +150 | °C |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| V_{ESD} | ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3) | > 2000 > 200 N/A | V |
| $I_{Latchup}$ | Latchup Performance Above V_{CC} and Below GND at 125°C (Note 4) | ± 500 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|------------|--|-----|-----------|------|
| V_{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V_{IN} | DC Input Voltage | 0.0 | 5.5 | V |
| V_{OUT} | DC Output Voltage | 0.0 | V_{CC} | V |
| T_A | Operating Temperature Range | -55 | +125 | °C |
| t_r, t_f | Input Rise and Fall Time $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$ | 0 | 100 20 | ns/V |

Device Junction Temperature versus Time to 0.1% Bond Failures

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

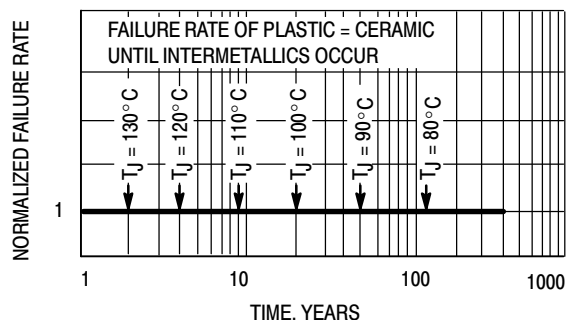


Figure 3. Failure Rate vs. Time Junction Temperature

MC74VHC1G125

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|-----------------|---|--|--------------------------|----------------------------|-------------------|----------------------------|----------------------------|----------------------------|------------------------------|----------------------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 2.0 3.0 4.5 5.5 | 1.5 2.1 3.15 3.85 | | | 1.5 2.1 3.15 3.85 | | 1.5 2.1 3.15 3.85 | V | |
| V _{IL} | Maximum Low-Level Input Voltage | | 2.0 3.0 4.5 5.5 | | | 0.5 0.9 1.35 1.65 | | 0.5 0.9 1.35 1.65 | | 0.5 0.9 1.35 1.65 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | 1.9 2.9 4.4 | V | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | V | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 3.0 4.5 | | 0.0 0.0 0.0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | V |
| I _{OZ} | Maximum 3-State Leakage Current | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | 5.5 | | | ±0.2 5 | | ±2.5 | | ±2.5 | μA |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 1.0 | | 20 | | 40 | μA |

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|--|---|--|-----------------------|------------|-------------|-----------------------|--------------|------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Y (Figures 3 and 4) | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 4.5 6.4 | 8.0 11.5 | | 9.5 13.0 | | 12.0 16.0 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 3.5 4.5 | 5.5 7.5 | | 6.5 8.5 | | 8.5 10.5 | |
| t _{PZL} , t _{PZH} | Maximum Output Enable Time, Input OE to Y (Figures 4 and 5) | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF | | 4.5 6.4 | 8.0 11.5 | | 9.5 13.0 | | 11.5 15.0 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF | | 3.5 4.5 | 5.1 7.1 | | 6.0 8.0 | | 8.5 10.5 | |
| t _{PLZ} , t _{PHZ} | Maximum Output Disable Time, Input OE to Y (Figures 4 and 5) | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF | | 6.5 8.0 | 9.7 13.2 | | 11.5 15.0 | | 14.5 18.0 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF | | 4.8 7.0 | 6.8 8.8 | | 8.0 10.0 | | 10.0 12.0 | |
| C _{IN} | Maximum Input Capacitance | | | 4.0 | 10 | | 10 | | 10 | pF |
| C _{OUT} | Maximum 3-State Output Capacitance (Output in High Impedance State) | | | 6.0 | | | | | | pF |
| C _{PD} | Power Dissipation Capacitance (Note 5) | Typical @ 25°C, V_{CC} = 5.0 V | | | | | | | | pF |
| | | 8.0 | | | | | | | | |

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC1G125

SWITCHING WAVEFORMS

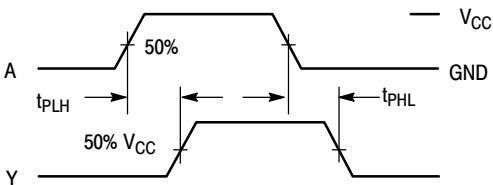


Figure 4. Switching Wave Forms

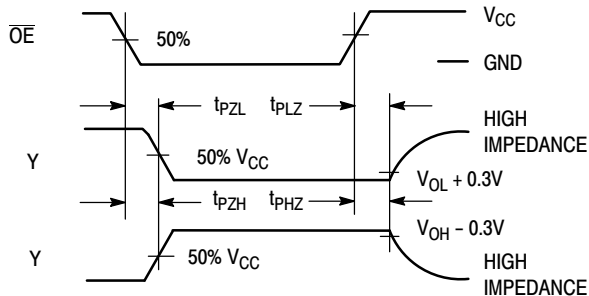
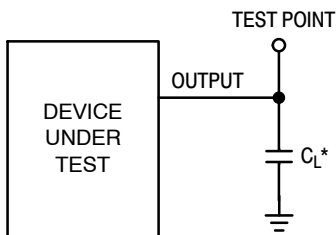
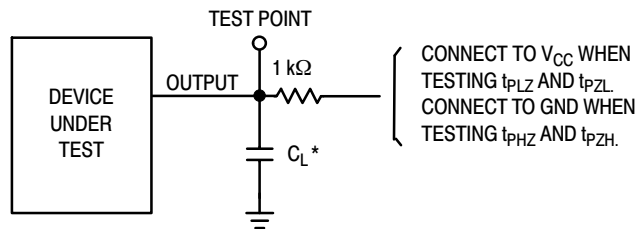


Figure 5.



*Includes all probe and jig capacitance

Figure 6. Test Circuit



*Includes all probe and jig capacitance

Figure 7. Test Circuit

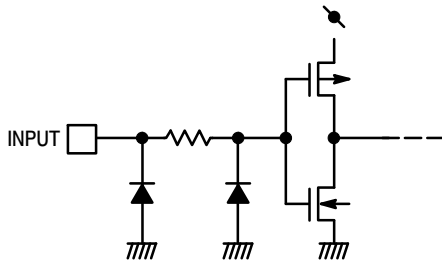


Figure 8. Input Equivalent Circuit

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------------|-----------------------------------|--------------------------|
| M74VHC1G125DFT1G | SC-88A/SOT-353/SC-70 (Pb-Free) | 3000 Units / Tape & Reel |
| M74VHC1G125DFT2G | | |
| NLVVHC1G125DFT1G* | | |
| M74VHC1G125DTT1G | TSOP-5/SOT-23/SC-59 (Pb-Free) | |

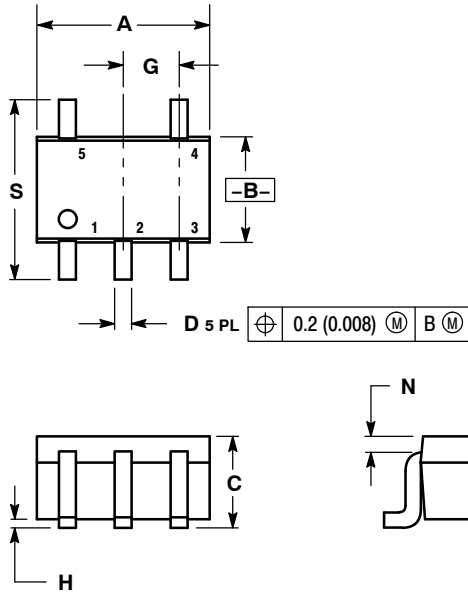
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC74VHC1G125

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
 CASE 419A-02
 ISSUE K



NOTES:

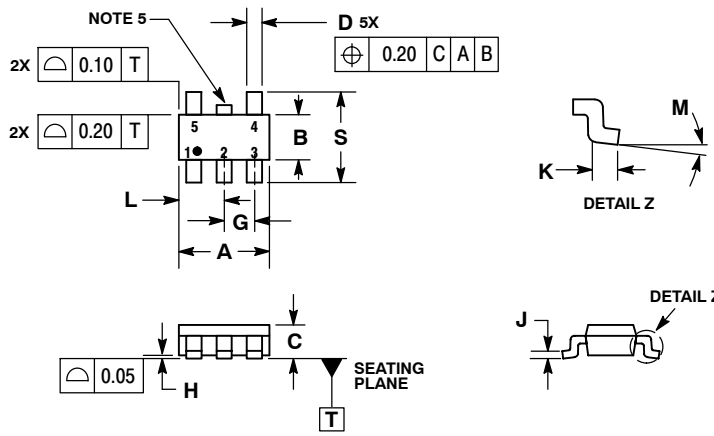
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

MC74VHC1G125

PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE H

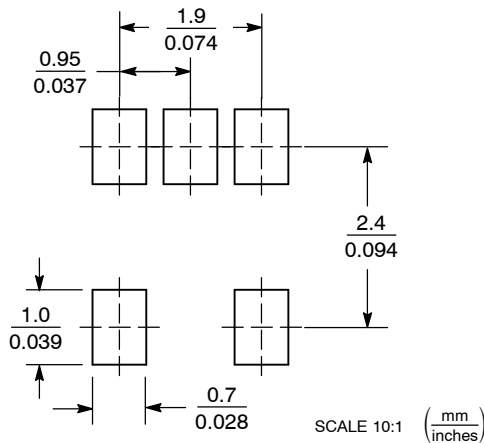


NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 3.00 | BSC |
| B | 1.50 | BSC |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 | BSC |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| L | 1.25 | 1.55 |
| M | 0° | 10° |
| S | 2.50 | 3.00 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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