MP2617H

Wide input Voltage, 3A, Switching Charger With NVDC Power Path Management For Single Cell Li+ Battery

The Future of Analog IC Technology

DESCRIPTION

The MP2617H is a monolithic, switch-mode, battery charger with power path management for single-cell Li-ion batteries in a wide range of tablets and other portable devices. The MP2617H integrates a synchronous buck regulator that provides regulated voltage to power the system output and charge the battery simultaneously. The MP2617H supports both USB and high-power DC adapter inputs. In USB mode, the input current limit can be programmed to 450mA or 825mA via the logic pins to cover USB2.0 and USB3.0 specifications. When the adapter input is present, the input current can also be limited to avoid overloading the DC adapter. The input current limit can be programmed up to 3A.

Smart power path management allows the MP2617H to regulate the system voltage for powering an external load and charging the battery independently and simultaneously. This allows for immediate system operation, even under missing or deeply discharged battery conditions. When the input current limit is reached, the system load is satisfied first, and then the charger uses the remaining current to charge the battery. Additionally, the smart power path control allows for an internal connection from the battery to the system to supplement additional power to the load in the event the system power demand increases over the input-limited power or the input is removed.

The MP2617H features high integration with all power switches integrated internally. No external MOSFET, blocking diode, or current sense resistor is required.

Two status monitor output pins are provided to indicate the battery's charge status and power source status. Other features include trickle charge, battery temperature monitoring, and timer and thermal limiting regulation on the chip.

The MP2617H is available in a QFN-20 (3mmx4mm) package.

FEATURES

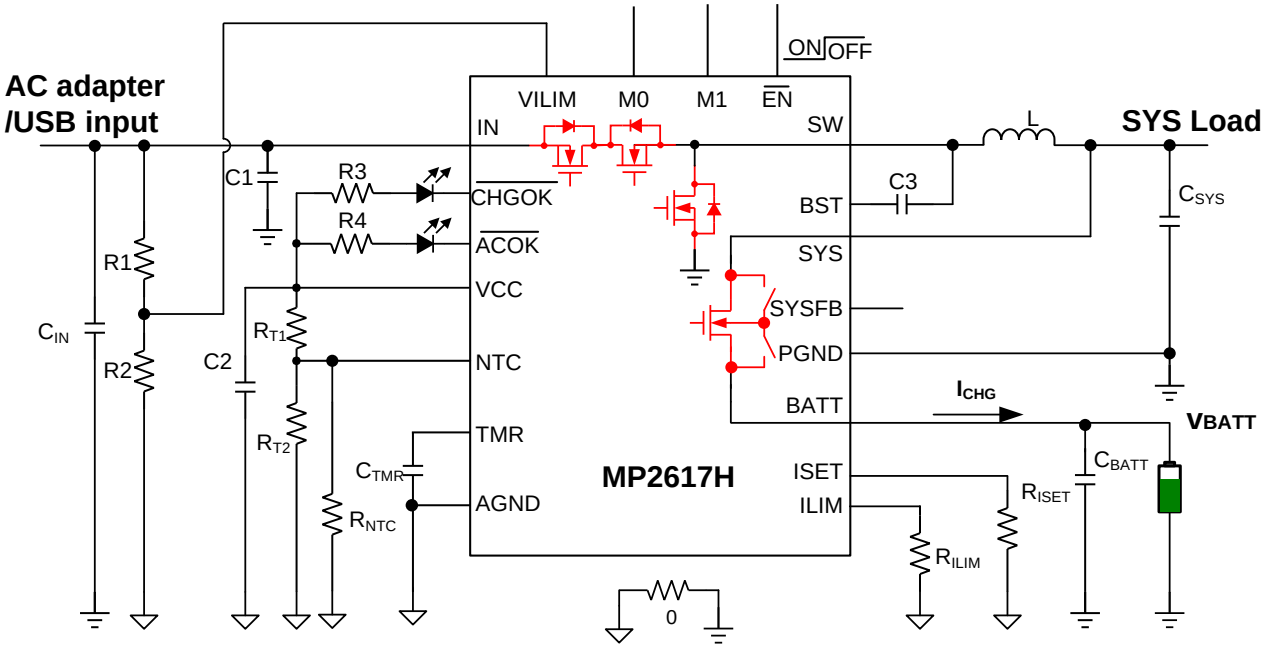
- 4V to 14V Operating Input Voltage
- Smart Power Path Management
- Five Control Loops: Input Current Limit, Input Voltage Limit, Constant Charge Current, Terminal Battery Control, and Thermal Foldback
- 1.6MHz Switching Frequency
- Programmable Input Current Limit
- Programmable Charge Current
- Single Input for USB and AC Adapter
- Covers USB2.0 and USB3.0 Input Specifications
- Fully Integrated Power Switches
- No External Blocking Diode or Sense Resistor Required
- Charging Operation Indicator
- Built-In Programmable Charging Timer
- Thermal Limiting Regulation on Chip
- Battery Temperature Monitor
- Available in a QFN-20 (3mmx4mm) Package

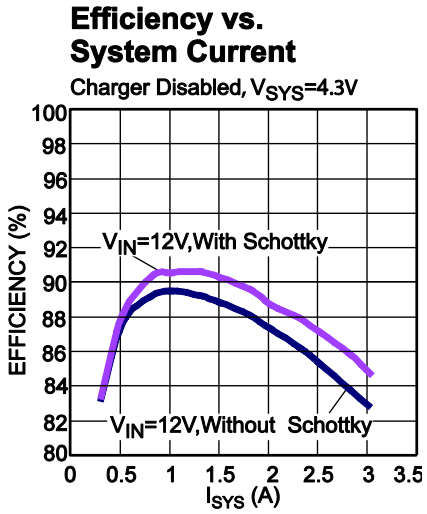
APPLICATIONS

- Smartphones
- E-Books
- GPS
- Portable Media Players
- Portable Handheld Solutions
- Tablet PCs

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking
MP2617HGL*	QFN-20 (3mmx4mm)	MP2617H

* For Tape & Reel, add suffix –Z (e.g. MP2617HGL–Z)

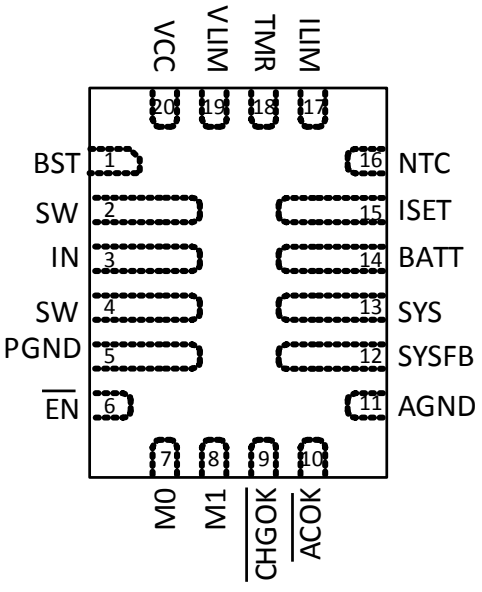
TOP MARKING

MPYW
2617
HLLL

MP: MPS prefix
Y: Year code
W: Week code
2617H: Product code of MP2617HGL
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-20 (3mmx4mm)

PIN FUNCTIONS

Package Pin #	Name	Description
1	BST	**Bootstrap.** A capacitor is connected between SW and BST to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage.
2, 4	SW	**Switch output.** Add an external 30V/1A Schottky diode from SW to GND when V_{IN} is higher or equal to12V and the output power include system load and battery charging is over 10W.
3	IN	**Power input of the IC from adapter or USB.**
5	PGND	**Power ground.**
6	$\overline{EN}$	**Function logic control of the IC.** Drive $\overline{EN}$ to logic low to enable the part. Drive $\overline{EN}$ to logic high to disable the part.
7	M0	**Mode select input.** M0 sets the input current limit mode in combination with M1.
8	M1	**Mode select input.** M1 sets the input current limit mode in combination with M0.
9	$\overline{CHGOK}$	**Open-drain output.** $\overline{CHGOK}$ is pulled low during charging. $\overline{CHGOK}$ is pulled high through an external resistor to VCC to indicate that the charge is complete.
10	$\overline{ACOK}$	**Open-drain output.** $\overline{ACOK}$ is pulled low to indicate the presence of a valid input power supply. $\overline{ACOK}$ is pulled high through an external resistor to VCC to indicate an invalid or removed input.
11	AGND	**Analog ground.**
12	SYSFB	**SYS voltage program.** Connect a resistor divider from SYSFB to SYS and AGND to program the system output voltage. Leave SYSFB floating to disable the function.
13	SYS	**DC/DC regulator output to power the system load and charge the battery.**
14	BATT	**Positive battery terminal.**
15	ISET	**Charge current program.** A resistor from ISET to AGND can program the charge current during CC charging. Float ISET to disable the charge function.
16	NTC	**Thermistor input.** Connect a resistor from NTC to VCC and the thermistor from NTC to ground. The thermistor is inside the battery pack.
17	ILIM	**Input current limit program.** A resistor from ILIM to AGND can program the input current limit with the adapter input.
18	TMR	**Set timer-out period.** Connect TMR to AGND to disable the internal timer.
19	VLIM	**Input voltage limit program.**
20	VCC	**Supply voltage of the IC.**

ABSOLUTE MAXIMUM RATINGS (1)

IN, SW ..... -0.3V to +20V
BATT, SYS ..... -0.3V to +6V
BST ..... -0.3V to +26V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = +25°C) **(2)**
QFN-20 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (IN) ..... 4.0V to 14V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (3mmx4mm) ..... 48 ..... 11 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Power (IN)						
IN operating range	V_{IN}		4.0		14 (5)	V
IN under voltage lockout threshold		Rising	3.65	3.8	3.95	V
		Falling	3.35	3.5	3.65	V
IN vs. BATT threshold		Rising	240	280	320	mV
		Falling	40	70	120	mV
BST voltage threshold	V_{BST}-V_{SW}	Rising	2.7	2.9	3.1	V
		Falling	2.55	2.75	2.95	V
Switching frequency			1.4	1.6	1.8	MHz
Input current limit	I_{IN}	USB2.0 mode	400	450	500	mA
		USB3.0 mode	750	825	900	mA
		Default mode	1840	2000	2160	mA
		Programmable mode, R_{ILIM} = 23kΩ	1840	2000	2160	mA
Input current limit reference voltage	V_{ILIM}		1.1	1.14	1.18	V
High-side NMOS on resistance	$R_{H\_DS(ON)}$	Include the block MOSFET		120	130	mΩ
Low-side NMOS on resistance	$R_{L\_DS(ON)}$			80	100	mΩ
High-side NMOS peak current limit			3.8	4.8	5.8	A
Input voltage clamp threshold	V_{VLIM}	Voltage on VLIM	1.49	1.52	1.55	V
Input quiescent current	I_{IN}	Charger enabled, USB2.0 mode		2.4	5	mA
		Charger enabled, USB3.0 mode		2.8	5	mA
		Charger enable, programmable mode		3.8	5	mA
		Charger enabled, default mode		3.8	5	mA
		Disabled, EN = 0V		3	5	µA
SYS to IN reverse current blocking		SYS = SW = 4.5V, V_{IN} = 0V, monitor V_{IN} leakage		0.01	0.2	µA
SYS Output						
Minimum SYS regulation voltage	V_{SYS}	SYS voltage at V_{BATT} ≤ 3.4V, SYSFB float	3.45	3.6	3.75	V
SYS regulation voltage	V_{SYS}	3.4V < V_{BATT} ≤ 4.2V, SYSFB float, BATT float	3.5	V_{BATT} + 0.2V	4.5	V
		Programmed by SYSFB	4.08		4.4	V
SYS reference voltage	V_{SYS_REF}		1.135	1.152	1.170	V
Battery Discharge						
BATT to SYS resistance		V_{IN} = 0V, I_{SYS} = 200mA, V_{BATT} = 4.2V		40	50	mΩ
BATT to SYS current limit		V_{SYS} > V_{BATT} - 800mV, V_{BATT} = 4.2V	5	6.2	7.4	A
		SYS short		230		mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Battery Charger Voltage Spec						
Terminal battery voltage	V_{BATT}	$V_{BATT} > V_{RECH}$, $I_{CHG} \le I_{BF}$, SYSFB float	4.179	4.2	4.221	V
		V_{SYS} < 4.2V, programmed by SYSFB		V_{SYS} - 0.04 x I_{BF}		V
Recharge threshold at V_{BATT}	V_{RECH}	SYSFB float	3.9	4.0	4.1	V
		SYSFB programmed	3.85	3.95	4.05	V
Recharge hysteresis				85		mV
Trickle charge threshold			2.9	3	3.1	V
Trickle charger hysteresis				200		mV
Battery Charger Current Spec						
Trickle charge current	$I_{TRICKLE}$			10%		I_{CC}
Termination charger current	I_{BF}		5%	10%	15%	I_{CC}
I_{BF} maximum limit				150	200	mA
Constant current mode charge current	I_{CC}	R_{ISET} = 760Ω	2.475	2.75	3.025	A
		R_{ISET} = 1.53kΩ	1.26	1.4	1.54	A
		R_{ISET} = 4.6kΩ	0.405	0.450	0.495	A
ISET reference voltage			1.1	1.15	1.2	V
Battery UVLO		Rising	2.4	2.6	2.8	V
		Falling	2.2	2.4	2.6	V
Idea diode regulation voltage	V_{SYS}	Supplement mode		V_{BATT} - 65mV		mV
BATT leakage current	I_{BATT}	V_{BATT} = 4.2V, SYS float, V_{IN} = PGND		20	30	µA
$\overline{ACOK}$, $\overline{CHGOK}$						
$\overline{ACOK}$, $\overline{CHGOK}$ output low voltage		Sinking 5mA		270	350	mV
$\overline{ACOK}$,$\overline{CHGOK}$ leakage current		Connected to 3.3V		0.1	0.5	µA
Timer						
Trickle charge time		C_{TMR} = 0.1µF, I_{CHG} = 1A		45		Min
Total charge time		C_{TMR} = 0.1µF, I_{CHG} = 1A		6.5		Hour
Negative Temperature Coefficient (NTC) Control						
NTC low temp rising threshold	V_{THL}	R_{NTC} = NCP18XH103F, 0°C	63	65	67	%V_{CC}
Hysteresis on low temp threshold				35		mV
NTC high temp falling threshold	V_{THH}	R_{NTC} = NCP18XH103F, 50°C	32	33.5	35	%V_{CC}
Hysteresis on high temp threshold				70		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Supply						
VCC UVLO		Rising	3.15	3.35	3.55	V
		Falling	2.8	3	3.2	V
VCC output voltage		0mA < I_{VCC} < 25mA, V_{IN} = 6V	4.3	4.5	4.6	V
VCC output current limit				40		mA
Logic						
$\overline{EN}$ input low voltage					0.4	V
$\overline{EN}$ input high voltage			1.5			V
$\overline{EN}$ input current		$\overline{EN}$ = 4V		4	8	μA
		$\overline{EN}$ = 0V	-0.5	-0.1		
M0, M1		Logic high	1.5			V
		Logic low			0.4	V
Protection						
Thermal limit temperature				120		°C
Thermal shutdown				150		°C

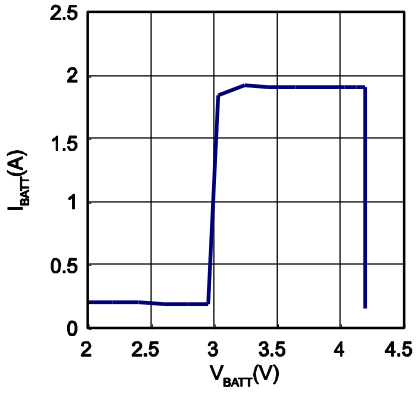
NOTE:

5) A Schottky diode is required from SW to GND when Pout is higher than 10W and VIN is over 12V.

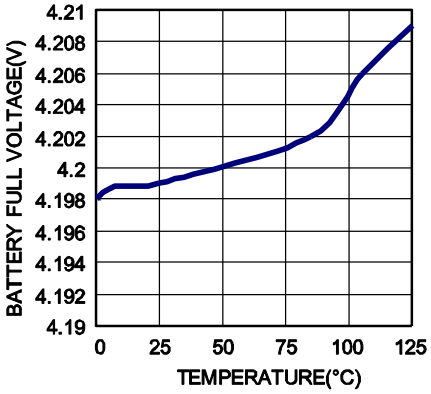
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = full range, default mode, I_{IN} limit = 2A, V_{SYS} = 4.4V, R6 and R7 are floating, I_{CHG} = 2A, V_{IN} clamp = 4.5V, L = 1.2 µH, T_A = +25°C, unless otherwise noted.

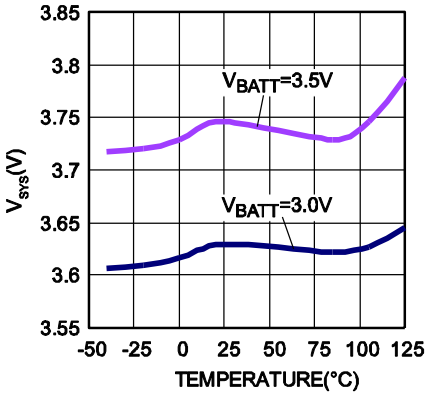
Charge Current vs. Battery Voltage



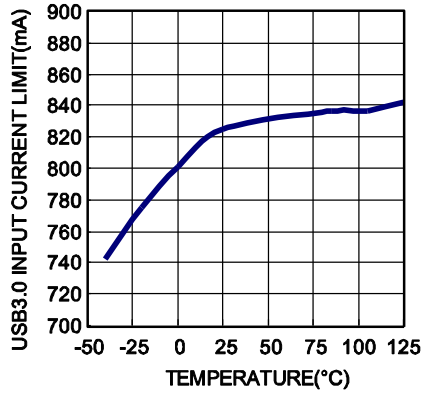
Battery Regulation vs. Temperature



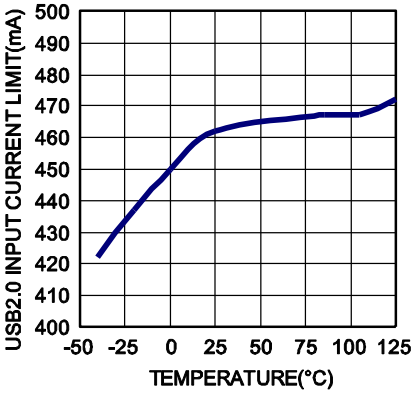
System Voltage Regulation vs. Temperature



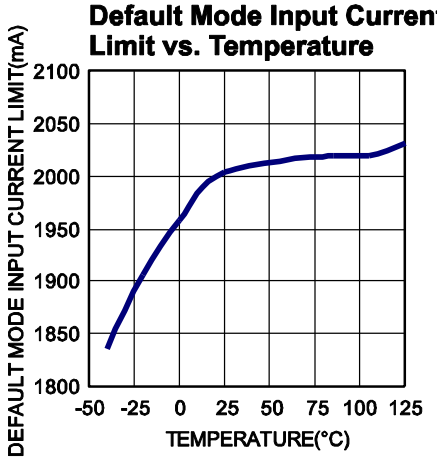
USB3.0 Input Current Limit vs. Temperature



USB2.0 Input Current Limit vs. Temperature

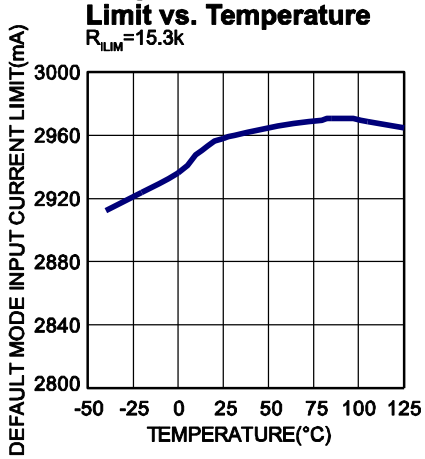


Default Mode Input Current Limit vs. Temperature

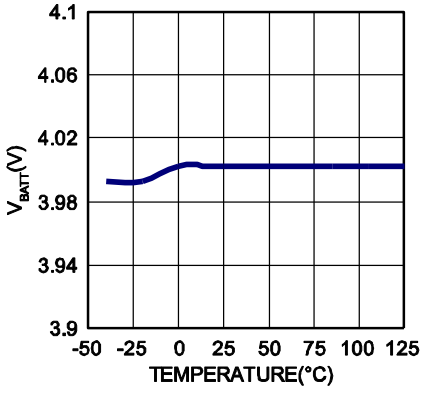


Program Mode Input Current Limit vs. Temperature

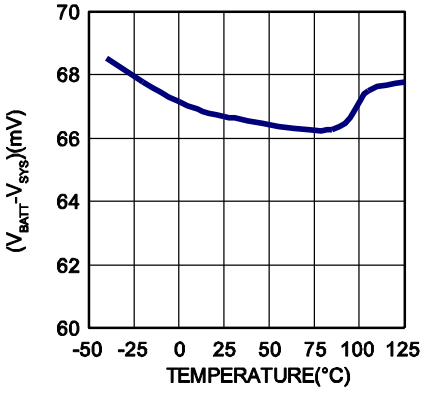
R_{ILIM}=15.3k



Battery Auto-recharge Threshold vs. Temperature



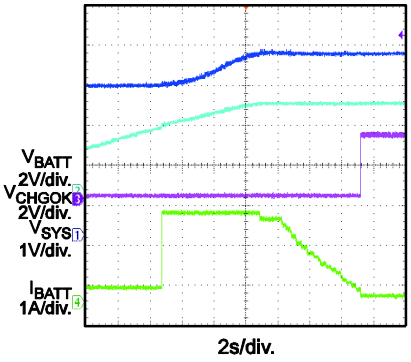
Ideal Diode Regulation vs. Temperature



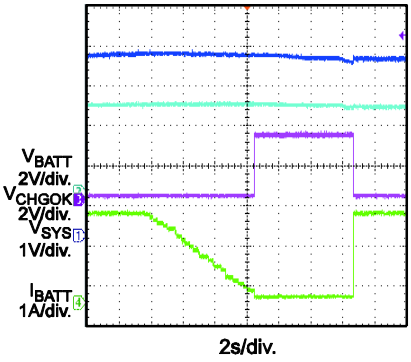
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BATT} = full range, default mode, I_{IN} limit = 2A, V_{SYS} = 4.4V, R6 and R7 are floating, I_{CHG} = 2A, V_{IN} clamp = 4.71V, L = 2.2µH, T_A = +25°C, unless otherwise noted.

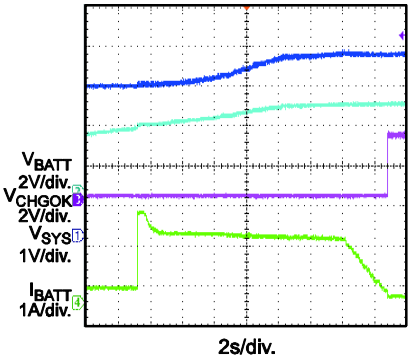
Battery Charge Curve
I_{SYS} = 0A



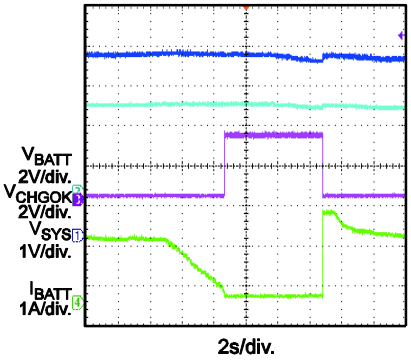
Auto-Recharge
I_{SYS} = 0A



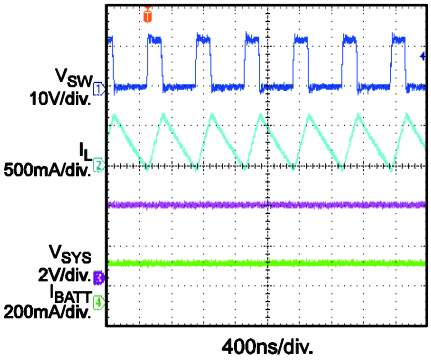
Battery Charge Curve
I_{SYS} = 1.5A



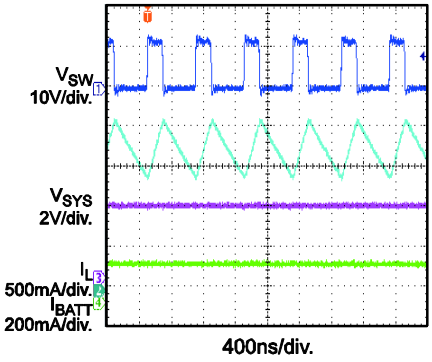
Auto-Recharge
I_{SYS} = 1.5A



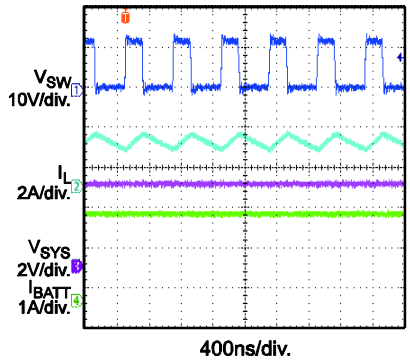
TC Steady State
V_{BATT} = 2.6V, I_{SYS} = 0A



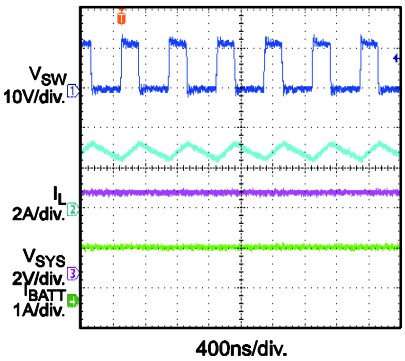
TC Steady State
V_{BATT} = 2.6V, I_{SYS} = 1.5A



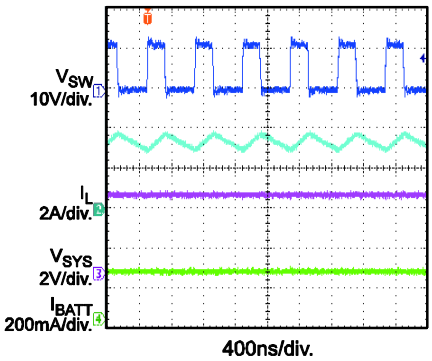
CC Steady State
V_{BATT} = 3.6V, I_{SYS} = 0A



CC Steady State
V_{BATT} = 3.6V, I_{SYS} = 1.5A



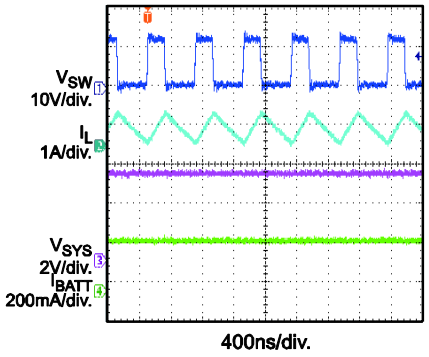
CC Steady State
V_{BATT} = 3.6V, I_{SYS} = 3A



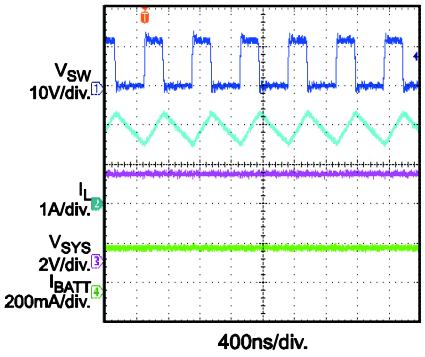
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BATT} = full range, default mode, I_{IN} limit = 2A, V_{SYS} = 4.4V, R6 and R7 are floating, I_{CHG} = 2A, V_{IN} clamp = 4.71V, L = 2.2µH, T_A = +25°C, unless otherwise noted.

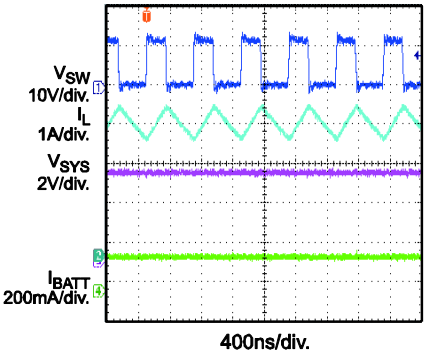
CV Steady State
V_{BATT} = 4.2V, I_{SYS} = 0A



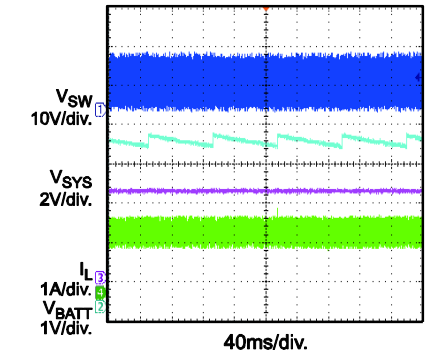
CV Steady State
V_{BATT} = 4.2V, I_{SYS} = 1.5A



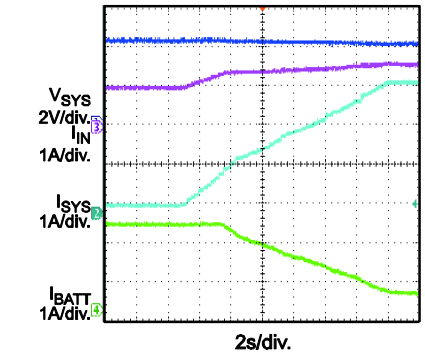
CV Steady State
V_{BATT} = 4.2V, I_{SYS} = 3A



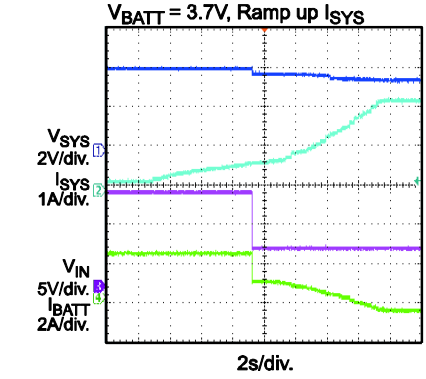
Battery Float Steady State
No Battery, I_{SYS} = 1.5A



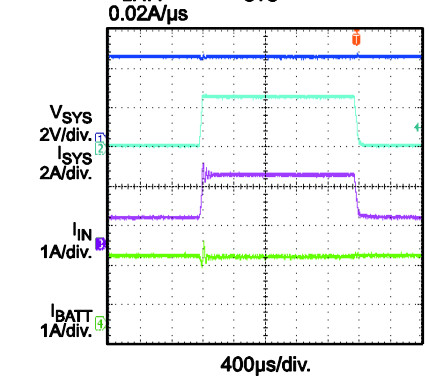
Input Current Limit
V_{BATT} = 3.7V, Ramp up I_{SYS}



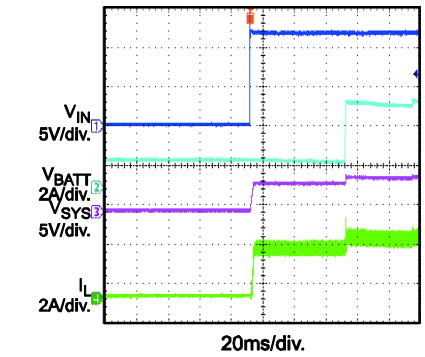
Input Voltage Limit
12V/1A Adapter IN,
V_{BATT} = 3.7V, Ramp up I_{SYS}



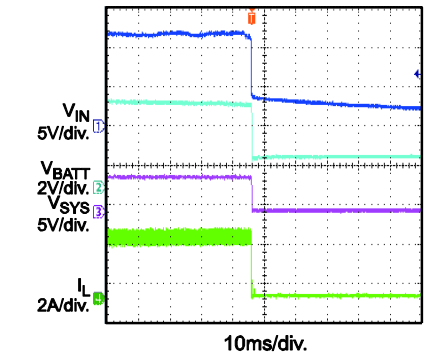
System Current Transient
V_{BATT} = 3.7V, I_{SYS} = 0-2.5A transient, 0.02A/µs



Plug in Adapter
No Battery, V_{SYS} = 4.4V, I_{SYS} = 3A



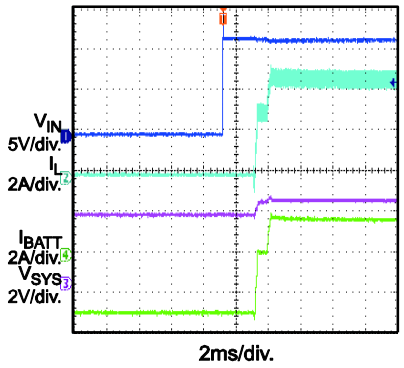
Remove Adapter
No Battery, V_{SYS} = 4.4V, I_{SYS} = 3A



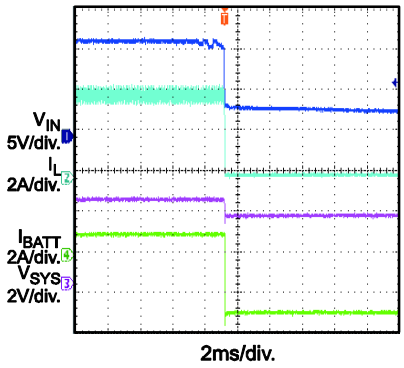
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BATT} = full range, default mode, I_{IN} limit = 2A, V_{SYS} =4.4V, R6 and R7 are floating, I_{CHG} = 2A, V_{IN} Clamp = 4.71V, L = 2.2µH, T_A = +25°C, unless otherwise noted.

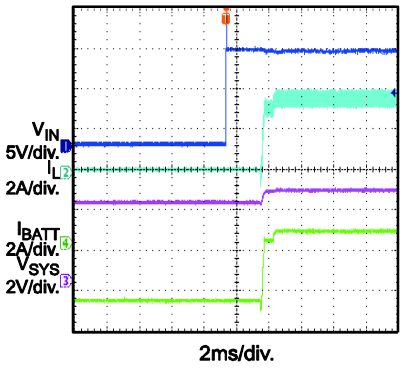
Plug in Adapter
V_{BATT} = 3.7V, I_{SYS} = 3A



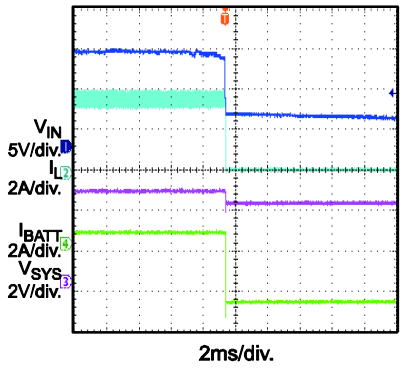
Remove Adapter
V_{BATT} = 3.7V, I_{SYS} = 3A



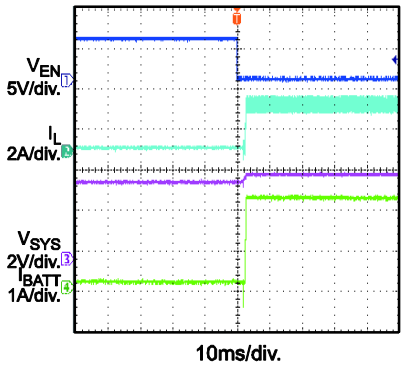
Plug in Adapter
V_{BATT} = 4.2V, I_{SYS} = 3A



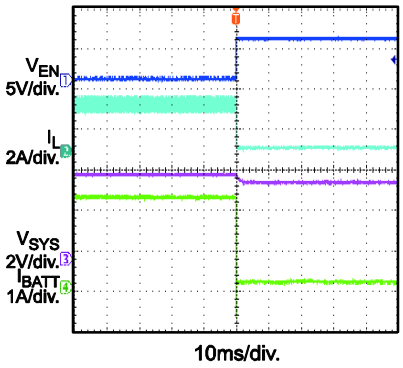
Remove Adapter
V_{BATT} = 4.2V, I_{SYS} = 3A



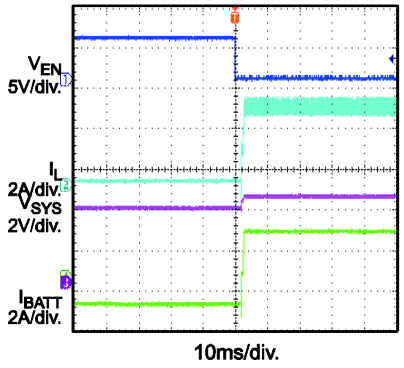
En On
V_{BATT} = 3.7V, I_{SYS} = 0A



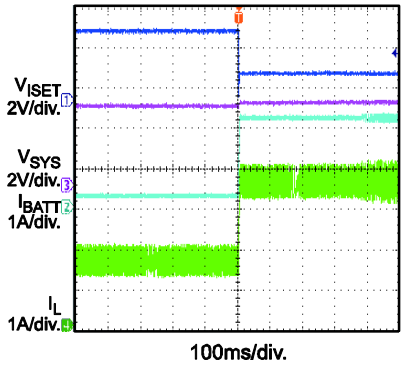
En Off
V_{BATT} = 3.7V, I_{SYS} = 0A



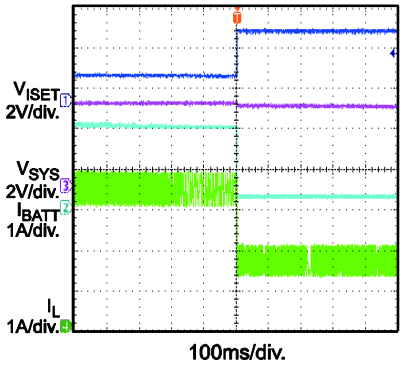
En On
V_{BATT} = 3.7V, I_{SYS} = 1.5A



Charge On
V_{BATT} = 3.7V, I_{SYS} = 1.5A



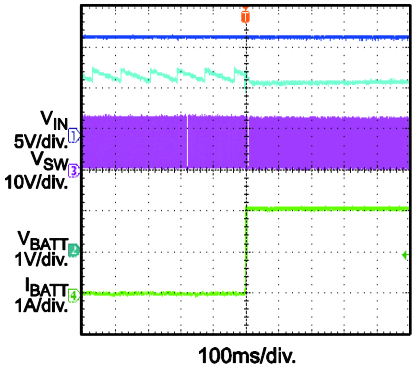
Charge Off
V_{BATT} = 3.7V, I_{SYS} = 1.5A



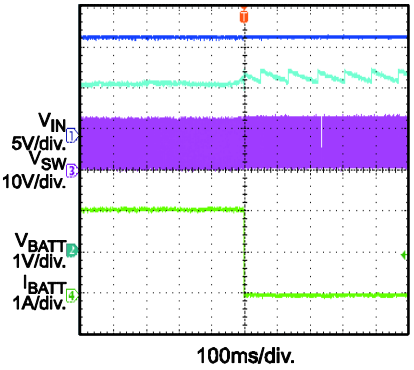
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BATT} = full range, default mode, I_{IN} limit = 2A, V_{SYS} = 4.4V, R6 and R7 are floating, I_{CHG} = 2A, V_{IN} clamp = 4.71V, L = 2.2µH, T_A = +25°C, unless otherwise noted.

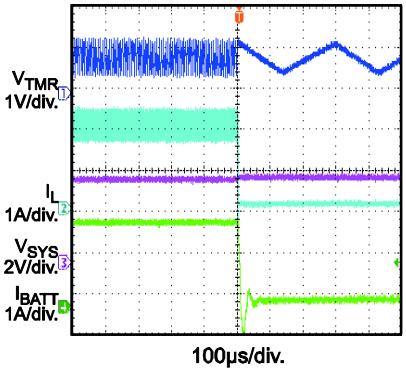
Battery Insertion
V_{BATT}= 3.7V, I_{SYS} = 0A



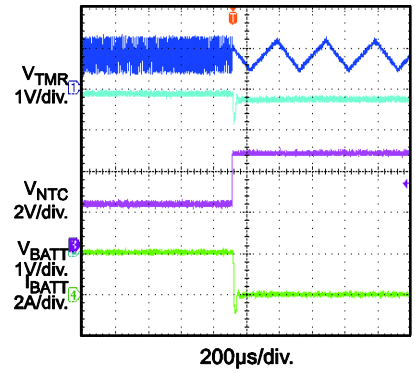
Battery Removal
V_{BATT} = 3.7V, I_{SYS} = 0A



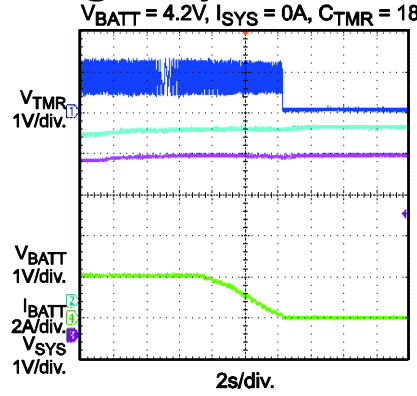
Time Out
V_{BATT} = 3.7V, I_{SYS} = 0A, C_{TMR}=180pF



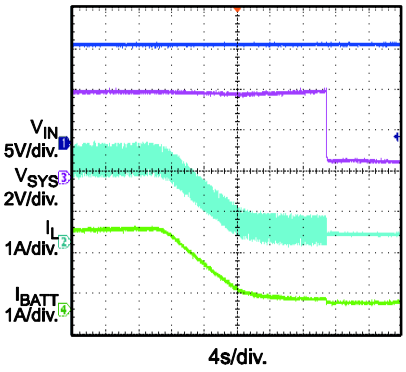
Time Suspend @ NTC Fault
V_{BATT} = 3.7V, I_{SYS} = 0A, C_{TMR} = 180pF



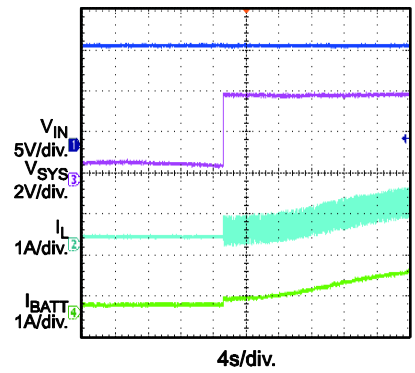
Time Refreshed @ Battery Full
V_{BATT} = 4.2V, I_{SYS} = 0A, C_{TMR} = 180pF



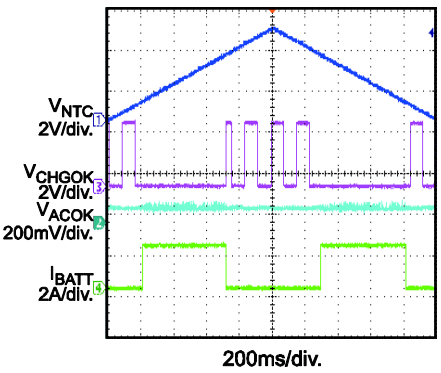
Thermal Shutdown
V_{BATT} = 3.7V, I_{SYS} = 0A
Increase the Ambier temperature slowly



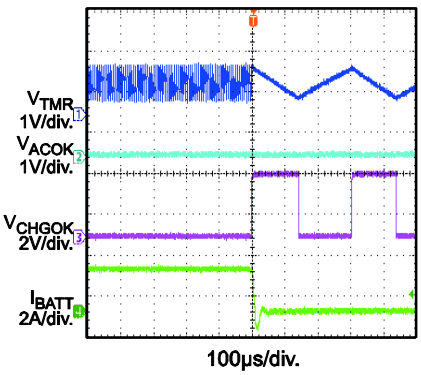
Thermal Recovery
V_{BATT} = 3.7V, I_{SYS} = 0A



Indication @ NTC Fault
V_{BATT} = 3.7V, I_{SYS} = 0A



Indication @ Timer Out
V_{BATT} = 3.7V, I_{SYS} = 0A



BLOCK DIAGRAM

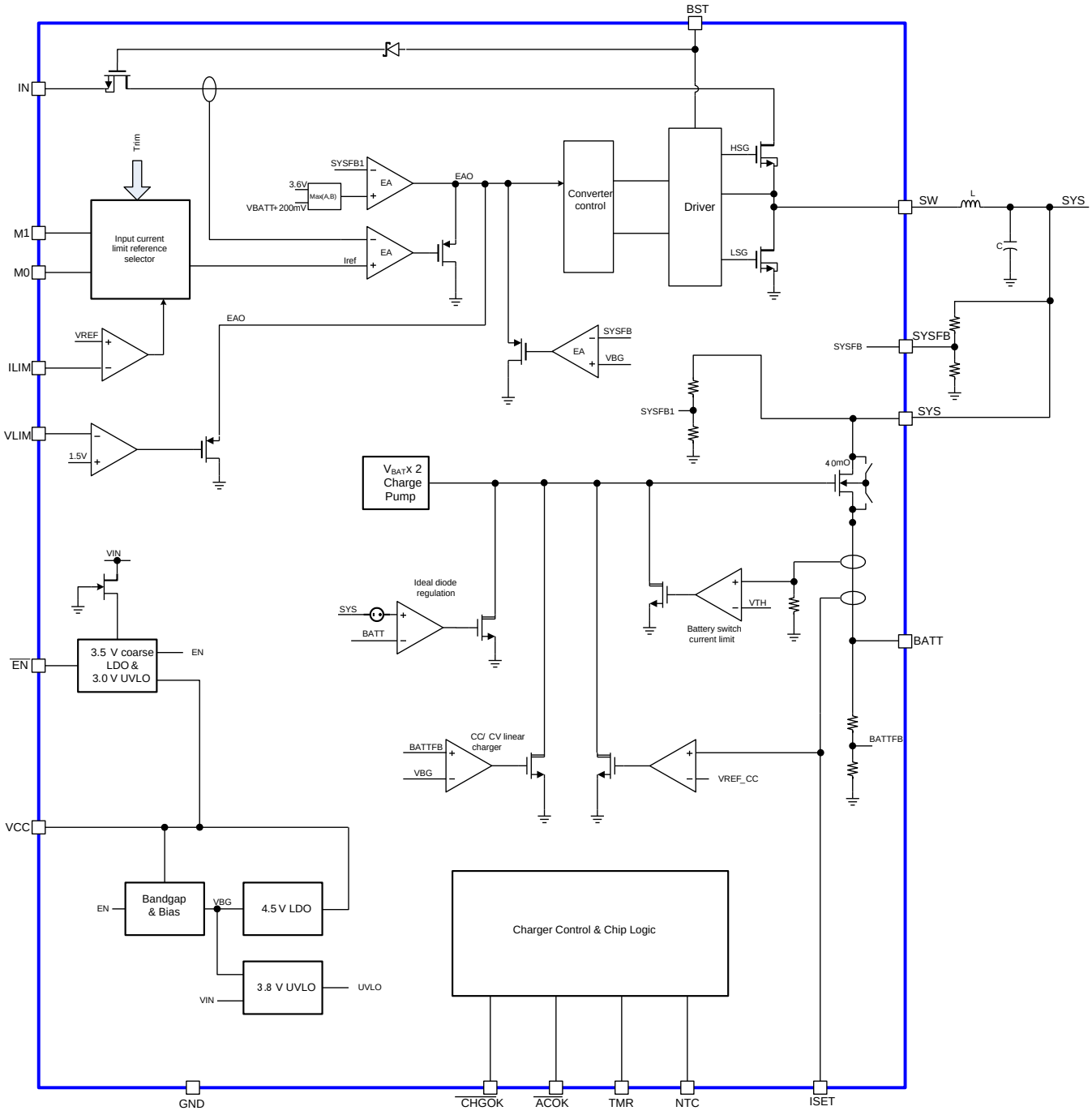


Figure 1: Functional Block Diagram

Figure 2: Functional Block Diagram

OPERATION

The MP2617H is a switching charger IC with integrated, smart, power path management for powering the system and charging a single-cell battery independently and simultaneously.

The MP2617H includes an input DC/DC step-down converter for a wide range of DC sources and USB inputs. The MP26127H has a precision average input current limit to make maximum use of the allowable input power. This feature allows for fast charging when the charger is powered from a USB port and ensures that the input current never exceeds the input power specification. Additionally, the input current limit threshold can be programmed by the logic inputs or a resistor from ILIM to ground.

The MP2617H implements an on-chip 40mΩ MOSFET, which works as a full-featured linear charger with trickle charge, high-accuracy, constant-current (CC) charge and constant-voltage (CV) charge, charge termination, auto-recharge, NTC monitor, built-in timer control, charge status indication, and thermal protection. The charge current can be programmed by an external resistor connected from ISET to AGND. The IC limits the charge current when the die temperature exceeds thermal regulation threshold.

The 40mΩ MOSFET works as an ideal diode to connect the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 40mΩ MOSFET is turned on, allowing the battery to power up the system.

With smart power path management, the system load is satisfied first, and the remaining current is used to charge the battery. The MP2617H reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

DC/DC Step-Down Converter

The DC/DC converter is a 1.6MHz, step-down, switching regulator to provide input power to SYS, which drives the combination of the system load and battery charger. The regulator contains an input current measurement and control scheme to ensure that the average input current remains below the level programmed via ILIM or the logic inputs (M0 and M1). This ensures compliance with the USB specifications and prevents overloading the wall adapter.

When the input voltage is higher than the under-voltage lockout (UVLO) threshold and 280mV higher than the battery voltage, the input voltage OK signal is active ($\overline{ACOK}$ becomes low), and the DC/DC converter soft starts. The input power is sufficient for supplying the combination of the system load and battery charger, and the input current limit loop is not triggered. The converter output voltage (V_{SYS}) is regulated.

If BATT is greater than 3.4V, V_{SYS} is approximately 0.2V above the battery voltage to minimize the power loss of the battery charger during fast charging. If BATT is less than 3.4V, V_{SYS} is fixed at 3.6V to power the system immediately, even when a drained battery is inserted to be charged (see Figure 2).

The system voltage can also be regulated to any value between 4.08V to 4.4V in the MP2617H by using a resistor divider on SYSFB (see R6 and R7 in Figure 10). If SYSFB is left floating, the system program is invalid, and V_{SYS} is regulated according to BATT voltage (see Figure 2).

The converter adopts a fixed off-time control to extend the duty cycle (close to 100%) when the input of the converter is close to V_{SYS}.

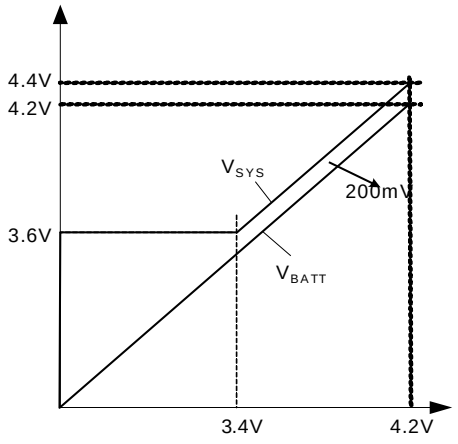


Figure 3: SYS Regulation Output

At near-100% duty operation, the BST refresh operation ensures that the driver voltage of the high-side MOSFET (HS-FET) is charged by turning on the low-side MOSFET (LS-FET) until the negative inductor current (I_L) reaches a threshold.

If the input power is insufficient for supplying the combination of the system load and battery charger, the DC/DC converter limits the total power requirement by restricting the input voltage, input current, and peak current through the MOSFET. The power path management reduces the charge current to satisfy the external system load first. According to this feature, the USB specification is always satisfied first, even if the charge current is set higher than the USB input current limit, and the real charge current is reduced as needed.

Input Limit State

If the input power is insufficient for supplying the combination of the system load and battery charger, the MP2617H implements three input limit control loops to reduce the charge current and satisfy the external system load first. The input in this case might be limited with either input current limit, input voltage limit, or DC/DC peak current limit.

1. Input-Current Limit: When the input current is higher than the programmed input current limit, the input current limit loop takes the control of the converter and regulates the input current at a constant value. If the battery voltage is over 3.4V, the output voltage (V_{SYS}) drops down according to the increase of the system current, and the charge current drops down after the BATT-to-SYS switch (40mΩ MOSFET) is fully on according to V_{SYS} dropping down. During this process, the system voltage is slightly higher than V_{BATT}. If the battery voltage is lower than 3.4V, to maintain the minimum system voltage and ensure system operation, the input current limit control pulls down the charge current directly o reduce the load of the converter so the system current is satisfied first.
2. Input-Voltage Limit: A resistor divider from IN to VLIM to AGND is used for input voltage limit control. When the voltage on VLIM reaches the 1.52V reference voltage, the output of the input voltage limit error amplifier drops to control the operation duty. In this mode, the input voltage is clamped according to the value set by the resistor divider. The control to the system voltage and charge current is the same as the input current limit control. The charge current drops down to satisfy the system current request first. This feature provides a second protection to the input power and ensures safe operation of the input adapter. Even if the wrong adapter is inserted, the MP2617H can continue operating, providing the maximum power to its load. The input voltage limit value can be programmed through the resistor divider from IN to VLIM to AGND.
3. Peak-Current Limit: The peak current of the high-side switch of the DC/DC converter is sensed during every cycle and is compared to the 4.8A reference. If the peak current reaches the threshold, peak-current limit mode is triggered. The control of the charge current is the same as the input current limit and input voltage limit.

Input Current Limit Setting

The ILIM current is a precise fraction of the adapter input current. When a programming resistor is connected from ILIM to AGND, the voltage on ILIM represents the average input current of the pulse-width modulation (PWM) converter. The input current approaches the programmed limit, and the ILIM voltage reaches 1.14V.

The average input current limit can be set through the resistor connected from ILIM to AGND according to Equation (1):

$$I_{IN\_LIM}=1.14\times\frac{40000}{R_{ILIM}(k\Omega)}(mA) \quad (1)$$

When connected to a USB power source, the input current limit is set internally, and the programmed value is invalid. The MP2617H provides a typical 450mA input current limit for USB2.0 specification, and a typical 825mA current limit for USB3.0 specification.

The input current limit can be set through the two logic pins (M0 and M1) according to its input specification (see Table 1). Both M0 and M1 are pulled to logic high when floating. Under this condition, the input current is limited to a default value of 2A.

Table 1: Input Current Limit Setting by M0 and M1

M0	M1	Mode
Low	Low	USB2.0 mode
Low	High	USB3.0 mode
High	Low	Programmable mode
High/float	High/float	Default mode

Input Voltage Limit Setting

The input voltage can be limited at a value set by a resistor divider from IN to VLIM to AGND according to the Equation (2):

$$V_{IN\_LIM}=1.52\times\frac{R1+R2}{R2}(V) \quad (2)$$

When the voltage on VLIM drops and reaches the 1.52V reference voltage, the input voltage is clamped to the setting value.

Battery Charger

The MP2617H's complete charge operation consists of trickle charge, automatic charge termination, charge status indication, timer control, NTC indication, automatic recharge, and thermal limiting.

When the PWM converter exits soft start, the battery charge cycle begins. The MP2617H first determines if the battery is deeply discharged. If the battery voltage is lower than the trickle charge threshold (typically 3.0V), the battery charger starts in trickle charge mode. The trickle charge current is limited to 10% of the programmed charge current until the battery voltage reaches 3.0V. If the charge remains in trickle charge mode for longer than "trickle charge timer period", the timer out condition is triggered, the charge is terminated, and $\overline{\text{CHGOK}}$ starts blinking to indicate that the battery is unresponsive. When the battery voltage is above 3.0V, the charger operates in constant-current mode. The current delivered to the battery attempts to reach the value programmed by ISET. Depending on the available input power and system load conditions, the battery charger may or may not be able to charge at the fully programmed rate. The system load is always satisfied first over the battery charge current. If the system load requirement is low, the battery can be charged at a fully constant current.

When the battery voltage reaches the battery full threshold, the charger enters constant-voltage mode operation.

End of Charge (EOC) and Indication

In constant-voltage charge mode, the battery voltage is regulated at 4.2V when SYSFB is floating or SYS is programmed higher than the battery-full threshold, and the charge current decreases naturally. Once the charge current reaches the battery full threshold (I_{BF}, 1/10 the programmed charge current), the battery is fully charged, and charge cycle is terminated.

If the charge current drops below I_{BF} because of any limit condition, the MP2617H exits CV mode, and the charge-full detection is invalid.

A safe timer starts at the beginning of each new charge cycle and monitors whether the entire charge period is within the programmed time limit. After each charge cycle, when the battery is indicated as full, the timer counter resets. If the time expires while the charging is still ongoing, the timer forces the MP2617H to terminate charging. $\overline{\text{CHGOK}}$ blinks to indicate the fault condition.

If system voltage is programmed below 4.2V by the resistor divider at SYSFB, the battery is charged close to V_{SYS} until the charge current reaches the I_{BF} threshold.

Automatic Recharge

Once the battery charge cycle is completed, the MP2617H turns off, indicating the battery-full status. During this process, the battery power may be consumed by the system load or self-discharge. If the input power is always on, to ensure that the battery is not exhausted, the new charge cycle begins automatically when

the battery voltage falls below the auto-recharge threshold (V_{RCHG}) when SYSFB is floating, or V_{RCHG} minus 50mV if SYSFB is not floating and connected to a resistor divider. The timer restarts when the auto-recharge cycle begins.

During the charge-off state when the battery is fully charged, if the input power is recycled, or the EN signal is refreshed, the charge cycle restarts, and the timer refreshes, even if the battery voltage is above the auto-recharge threshold.

Charge Current Setting

The charge current of the MP2617H is programmed using a single resistor from ISET to ground. The program resistor and charge current can be calculated with Equation (3):

$$I_{CHG} = 1.15 \times \frac{1800}{R_{SET}(k\Omega)} (mA) \quad (3)$$

In either constant-current mode or constant-voltage mode, the ISET voltage is proportional to the actual charge current delivered to the battery (I_{BATT}). The charge current can be calculated by monitoring the ISET voltage with Equation (4):

$$I_{BATT} = \frac{V_{ISET}}{1.15} \times I_{CHG} \quad (4)$$

Additionally, the actual battery charge current may be lower than the programmed current due to the limited input power available and prioritization of the system load.

The battery charge full-current threshold (I_{BF}) is set internally at 10% of the programmed charge current. However, I_{BF} has a 150mA maximum limit which cannot be exceeded.

Logic Control

The MP2617H has two separate enable control pins. $\overline{EN}$ is a logic control pin that controls the operation of the entire IC. When $\overline{EN}$ is low, the IC is enabled, and the PWM converter output powers the system and the charger. When $\overline{EN}$ is high, both the PWM converter and the charger are disabled. The BATT-to-SYS switch fully turns on to connect the battery to power the system.

ISET can be also used to control the operation of the charger. Floating ISET disables the charger function, while the output of the PWM converter continues to supply power to the system. Conversely, a resistor from ISET to AGND enables charging at the programmed charge current.

The logic control of the ISET pin of the MP2617H can be set as shown in Figure 3. In this way, logic low can be set as the off signal, and logic high can be set as the on signal with an N-channel MOSFET.

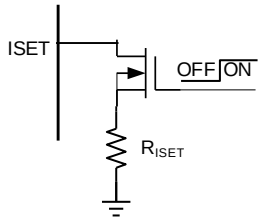


Figure 3: ISET Logic Control

Input Power Status Indication ($\overline{ACOK}$)

An internal UVLO circuit monitors the input voltage and keeps the IC in its off state until the input rises over the rising threshold (3.8V). When the input voltage decreases below the lower threshold (3.5V), the IC turns off, and the system load is powered by the battery automatically. $\overline{ACOK}$ is an open-drain, active-low output that indicates the status of the input power. The input is considered valid when the input voltage is over the UVLO rising threshold and 280mV higher than the battery voltage to ensure that both the converter and the charger can operate normally. If the input voltage from an adapter or a USB port is indicated as OK, $\overline{ACOK}$ turns low.

During $\overline{EN}$ off or thermal shutdown conditions, $\overline{ACOK}$ turns high to indicate that no power is provided by the input to the system. The $\overline{ACOK}$ signal indicates whether the input is supplying power to the system load or not. Any other condition cannot affect the $\overline{ACOK}$ indication as long as the input power is present.

Charge Status Indication ($\overline{CHGOK}$)

$\overline{CHGOK}$ is an open-drain, active-low output that indicates the status of the charge. $\overline{CHGOK}$ is low during normal charging operation and turns high after the charge is full. $\overline{CHGOK}$ blinks if a fault condition occurs, including an NTC fault (battery temperature is invalid) and timer out (bad battery).

In the event of a fault condition, $\overline{CHGOK}$ switches at 6Hz with a 50% duty cycle and enters blinking mode. Check the application circuit to find the root cause of the fault condition if the blinking signal is asserted.

For no-battery conditions, $\overline{CHGOK}$ blinks according to the transition between charging and charge full. The blinking frequency is determined by the charge and discharge cycle of the output capacitor.

If the charge current to the battery is low or if the battery is in supplement mode caused by insufficient input power, $\overline{CHGOK}$ remains low to avoid providing a false charge-full indication.

Table 2 shows the $\overline{ACOK}$ and $\overline{CHGOK}$ status under different charge conditions.

Table 2: Charger Status Indication

$\overline{ACOK}$	$\overline{CHGOK}$	Charger Status
Low	Low	In charging, supplement mode
Low	High	End of charge, ISET disable charger only
Low	Blinking at 6Hz	NTC fault, timer out
High	High	V_{IN} absent, $\overline{EN}$ disable, thermal shutdown

Timer Setting

The MP2617H uses an internal timer to terminate the charge if the timer times out. The timer duration is programmed by an external capacitor at TMR and related to the real charge current.

The trickle-mode charge time can be calculated with Equation (5):

$$t_{Trickle\_TMR} = 45 \times \frac{C_{TMR}}{0.1\mu F}(min)\ (I_{CHG} = 1A) \quad (5)$$

The total charge time can be calculated with Equation (6):

$$t_{Total\_TMR} = 6.5 \times \frac{C_{TMR}}{0.1\mu F}(hr)\ (I_{CHG} = 1A) \quad (6)$$

Equation (5) and Equation (6) are based on a 1A charge current. As a result of the power path management control, the charge current might vary during normal operation. Under this condition, the MP2617H takes this variation into account automatically and adjusts the timer period accordingly.

When the charge current is higher than 1A, the safe timer period is reduced accordingly with the same TMR capacitor. If the charge current is reduced because of insufficient input power, the timer period is increased proportionally with the same rate at which the charge current is reduced.

If the charge current reduces to 0 due to a high system load, the timer is suspended temporarily. This feature prevents falsely tripping the timer and indicating a bad battery when there is little charge current delivered to the battery as a result of insufficient input power. When a timer-out condition occurs, the MP2617H terminates the charge immediately, and $\overline{CHGOK}$ blinks to indicate the fault status. The timer is refreshed and the MP2617H restarts the charge cycle if the input starts up again, the $\overline{EN}$ or ISET signal is refreshed, or auto-recharge occurs.

NTC Thermistor

NTC allows the MP2617H to sense the battery temperature using a negative thermal coefficient (NTC) thermistor, usually available in the battery pack to ensure a safe operating environment for the battery. Connect a resistor with an appropriate value from VCC to NTC and the NTC resistor from NTC to AGND. The voltage on NTC is determined by the resistor divider whose divide ratio as the different resistance of the NTC thermistor depends on the ambient temperature of the battery.

The MP2617H has an internal NTC voltage comparator to set the upper and lower limit of the divide ratio. If the NTC voltage falls out of this range, then the temperature is outside of the safe operating range. As a result, the

MP2617H stops charging and reports this on the indication pins. Charging resumes automatically after the temperature falls back into the safe range.

Thermal Protection

The MP2617H implements thermal protection to prevent thermal damage to the IC or surrounding components. An internal thermal sense and feedback loop decrease the charge current automatically when the die temperature rises to about 120°C. This function is referred to as the charge current thermal fold-back. This feature protects the MP2617H from excessive temperature due to high-power operation or high ambient thermal conditions. Another benefit of this feature is that the charge current can be set according to the requirement rather than the worst-case condition for a given application with the assurance of safe operation. The MP2617H stops charging if the junction temperature rises above 150°C as the IC enters thermal shutdown protection.

Ideal Diode Mode

If the system current requirement increases such that the pre-set input current limit of the PWM converter is reached and the charge current has reduced to zero, the additional current will be drawn from the battery via the BATT-to-SYS switch. To avoid very large currents from being drawn from the battery which might affect the reliability of the device, the MP2617H controls the battery MOSFET to work in the ideal diode mode. When V_{SYS} drops to 40mV lower than V_{BATT}, then the MP2617H will enter ideal diode mode and regulate V_{SYS} to V_{BATT} - 65mV. After the system load decreases and V_{SYS} is 40mV higher than V_{BATT}, the battery MOSFET exits ideal diode mode, and the charge cycle restarts softly.

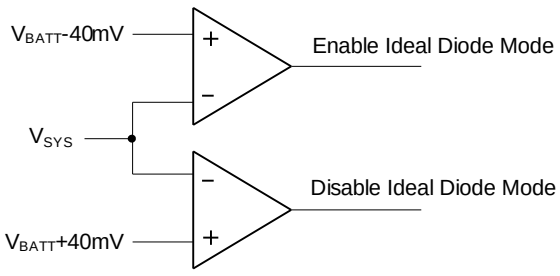


Figure 4: Ideal Diode Mode Enable/Disable

Battery Discharge Protection

When the input power is removed or invalid, the system load draws power from the battery via the battery switch. Under this condition, the battery switch is fully on to minimize power loss. The MP2617H integrates battery discharge protection. If the battery discharge current is larger than the discharge current limit threshold (I_{DIS}, 6.2A), the current is regulated at the pre-set limited value. If the current increases further, the SYS voltage starts to decrease. When V_{SYS} drops to about 800mV below V_{BATT}, a SYS short condition is detected. Under this condition, the discharge current is limited at 230mA. In the event of a short from the system to GND, the discharge current from the battery to the system is also limited to 230mA.

The battery voltage UVLO is always monitored. If the battery voltage is lower than the battery UVLO threshold, the battery switch is turned off immediately. This feature prevents the battery from being over-discharged.

Dynamic Power Path Management (DPPM)

In the presence of a valid input source, the PWM converter supplies current to both the system and the battery charger.

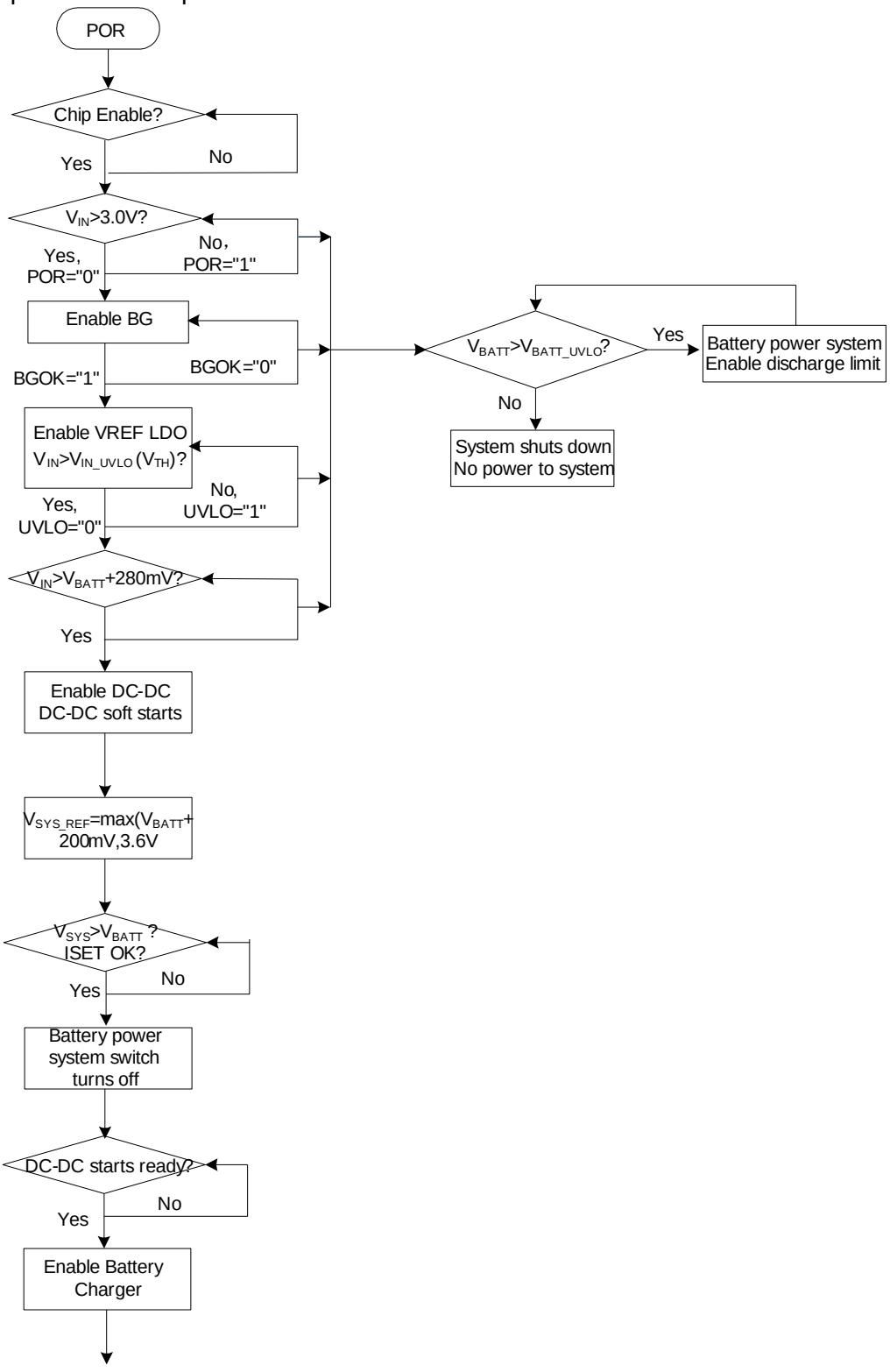
The voltage (V_{SYS}) is regulated based on the value of the battery voltage. When V_{BATT} is higher than 3.4V, V_{SYS} is regulated 200mV above V_{BATT} to charge the battery. When V_{BATT} is lower than 3.4V, V_{SYS} is regulated at a constant 3.6V to ensure that the system can still be powered up, even with a drained battery connected.

When the input source is overloaded, either the current exceeds the input current limit or the voltage falls below the input voltage limit. The MP2617H then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit. If the system current increases beyond the power allowed by the input source, additional power is drawn from the battery via an on-chip 40mΩ MOSFET working as an ideal diode. If the system current increased further, when the discharge current times the Ron is over 65mV, the V_{SYS} can not be regulated, the BATT to SYS MOSFET just turned fully on, the battery powers the system together with the converter from VIN as the supplement mode.

Additionally, if the input source is removed, the MP2617H turns on the 40mΩ MOSFET, allowing the battery to power the system load to maintain the operation of the portable device.

Operation Flow Chart

Figure 5 shows the operation flow chart of the MP2617H. Figure 6 shows the operation process.



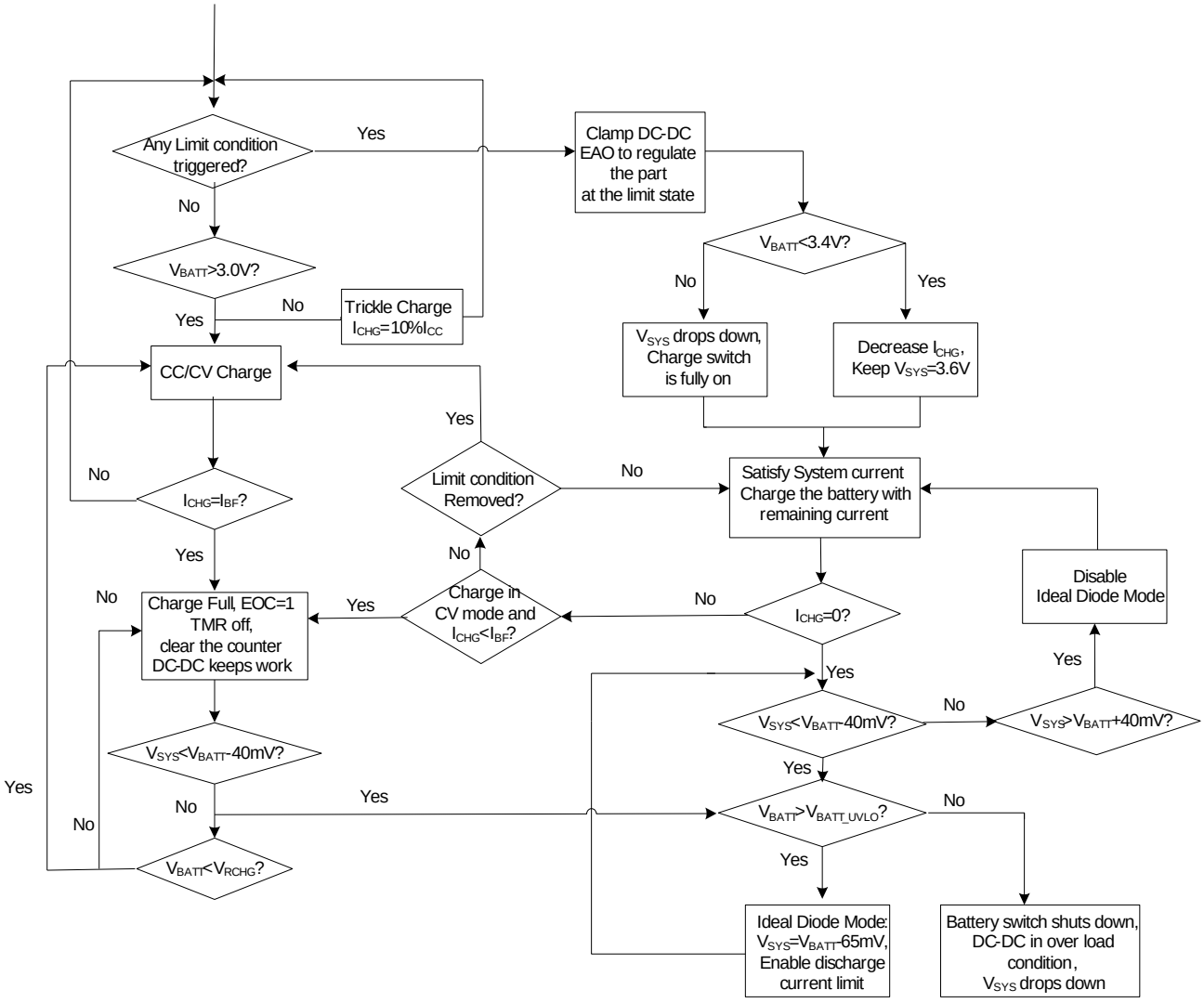


Figure 5: MP2617H Operation Flow Chart under No Fault Condition

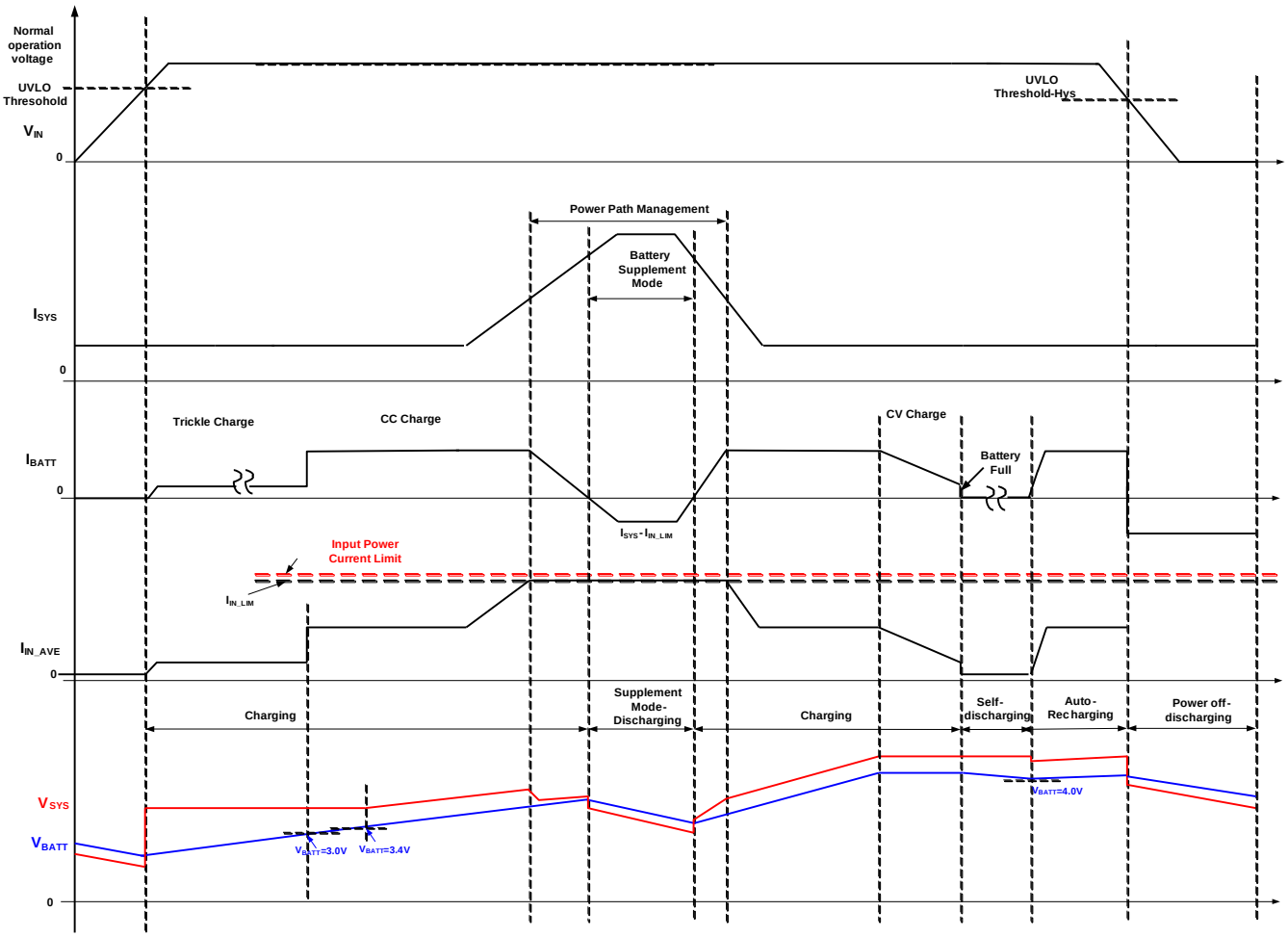


Figure 6: MP2617H Operation Process under No Fault Condition

APPLICATION INFORMATION

Setting the Input Current Limit

First the input current limit can be set by the M0 and M1 pins refer to the Table 1, the exact current value in minimum, typical and maximum is listed in the EC table.

Under program mode, connect a resistor (R_{ILIM}) from ILIM to AGND to program the input current limit for different input ports. The relationship between the input current limit and resistor value is as the following formula from Equation (1):

$$I_{IN\_LIM}=1.14\times\frac{40000}{R_{ILIM}(k\Omega)}(mA) \quad (1)$$

The tolerance is ±8% of the input current limit setting.

So for a required minimum input current limit value, just calculate its typical value first, then calculate the setting resistor based on Equation (1). Also the maximum value can be calculated according to the tolerance. 1% accuracy resistor is used for this setting.

Also, for a given resistor of R_{ILIM}, the input current limit can be calculated. Following table is an example:

Table 3: Example of R_{ILIM} setting

Resistor	R_{ILIM} (kΩ)	I_{IN_LIM} (mA)	8%	-8%
Typ.	54.9	830.601	897.049	764.153
Min.	54.351	838.991	906.11	771.872
Max.	55.449	822.377	888.168	756.587

Therefore, if customer selected a 54.9k in 1% accuracy resistor for the input current limit setting, then the typical input current limit value is 830.6mA, the minimum is 756.6mA and the maximum is 906mA.

Setting the Charge Current

A resistor (R_{ISET}) connected from ISET to AGND sets the charge current (I_{CHG}). The relationship between the charge current and setting resistor is shown in Equation (3):

$$I_{CHG}=1.15\times\frac{1800}{R_{SET}(k\Omega)}(mA) \quad (3)$$

For example, if the typical I_{CHG} is designed as 2A, then the R_{SET} is calculated at 1.05kΩ. For example, if the typical I_{CHG} is designed as 2A, then the R_{SET} is calculated at 1.05kΩ. The tolerance of the I_{CHG} setting is ±10%. If the minimum or maximum charge current is required, first the typical value should be calculated according to the tolerance. After that, calculate the resistor according to formula (3). 1% accuracy resistor is used for this setting.

For a given setting resistor, the charge current can be calculated by the same way did in the input current limit setting. Usually in USB mode, the charge current is always set over the USB input limit specification. Then the MP2617H regulates the input current constant at the limitation value. Therefore, the real CC charge current is not the setting value and varies with different input and battery voltages.

The maximum CC charge value can be calculated with Equation (7):

$$I_{CC\_MAX}=\frac{V_{IN}\times I_{ILIM}\times\eta}{V_{TC}}(A) \quad (7)$$

Where V_{TC} is the trickle charge threshold (3V), and η is the current charge efficiency. If V_{IN} is 5.5V, I_{ILIM} is 1.5A, η is 83%, then I_{CC_MAX} is 2.28A.

Figure 7 shows a calculating charge current curve by limiting the input current limit based on the MP2617H.

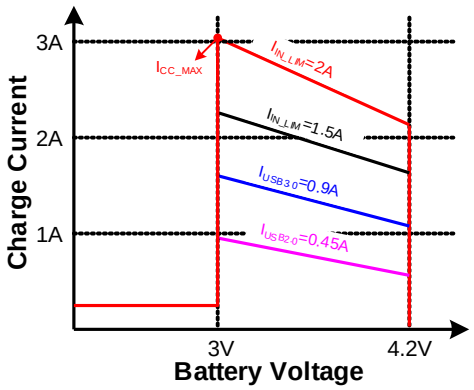


Figure 7: I_{CHG} Variation with Different Input Current Limit

Setting the Input Voltage Limit

The input clamp voltage is set using a resistive voltage divider from the input voltage to VLIM pin. The voltage divider divides the input voltage down to the limit voltage with the ratio in Equation (8):

$$V_{VLIM} = V_{IN\_LIM} \times \frac{R2}{R1+R2} (V) \quad (8)$$

The input voltage can be calculated with Equation (10):

$$V_{IN\_LIM} = V_{VLIM} \times \frac{R1+R2}{R2} (V) \quad (9)$$

The voltage clamp reference voltage (V_{VLIM}) is 1.52V, and R2 is typically 10kΩ. With this value, calculate R1 with Equation (11):

$$R1 = R2 \times \frac{V_{IN\_LIM} - V_{VLIM}}{V_{VLIM}} (V) \quad (10)$$

For example, for a 4.65V input limit voltage, R2 is 10kΩ, and R1 is 20.6kΩ.

The minimum value and the maximum value of the input voltage limit can be calculated according to the accuracy of the resistor and the tolerance of V_{VLIM}. 1% accuracy resistors are used for R1 and R2.

Setting the System Voltage

The system voltage can be regulated to any value between 4.08V to 4.4V by the resistor divider on SYSFB, shown as R6 and R7 in Figure 10. Calculate V_{SYS} with Equation (11):

$$V_{SYS} = V_{SYS\_REF} \times \frac{R6+R7}{R7} \quad (11)$$

Where V_{SYS_REF} is the reference voltage of SYS (1.152V). With a typical value for R7 (10kΩ), R6 can be determined with Equation (12):

$$R6 = R7 \times \frac{V_{SYS} - V_{SYS\_REF}}{V_{SYS\_REF}} (V) \quad (12)$$

For example, for a 4.2V system voltage, R7 is 10kΩ, and R6 is 26.5kΩ. 1% resistors are selected for the R5 and R6.

Be noted that, the minimum V_{SYS} is limited to be higher than the maximum value of the auto-recharge threshold, which is 4.05V.

Selecting the Inductor

Inductor selection trades off among cost, size, and efficiency. A lower inductance value corresponds to a smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. From a practical standpoint, the inductor ripple current does not exceed 30% of the maximum load current under worst cases conditions. For example, if the I_{CHG} is setting to 3A in MP2617H, then, ΔI_L is general set at 0.9A.

However, for the light load condition, the inductor ripple current will be very small which may cause unstable operation due to the peak current mode control of the IC. For stable operation, the experienced minimum limit value for inductor current ripple is 0.5A. Therefore, the inductor current ripple is the maximum one of 30% times I_{CHG} and 0.5A.

And the inductance can be calculated according to Equation (13):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L\_MAX}} \frac{V_{BATT}}{V_{IN} \times f_S (MHz)} (\mu H) \quad (13)$$

The peak current of the inductor is calculated as Equation (14):

$$I_{PEAK} = I_{LOAD(MAX)} \times (1 + \frac{\%ripple}{2}) (mA) \quad (14)$$

Where V_{IN}, V_{SYS}, and f_S are the input voltage, the SYS output voltage, and the switching frequency, respectively.

Following Table 4 provides the selection guide of the inductance based on different input voltage.

Table 4: Inductance Selection Guide under different Input Voltage

SPEC	Inductance Selection						
V_{IN}	$L=\frac{V_{IN}-V_{SYS}}{\Delta I_L}\frac{V_{SYS}}{V_{IN}\times f_S(MHz)}$ ΔI_L=max (0.3*I_{CHG},0.5A) ΔI_{LMIN}=0.5A ΔI_{LMAX}=0.9A	L_{MIN} (uH)	L_{MAX} (uH)	L (uH)	Saturation Current (A)(6)	DCR (mΩ)	Package
5V		0.367	1.25	1.0	>3.95	<50	Application Required
9V		1.5	2.8	2.2	>3.95	<50	Application Required
12V		1.75	3.5	2.2	>6(7)	<50	Application Required

For the condition that VIN is higher or equal to 12V, and the total output power including system load and battery charging is over 10W, an 1A schottky diode from SW to GND is required. The voltage rating of the schottky diode is usually selected at 30V.

Selecting the Input Capacitor

The input capacitor (C_{IN}) from the typical application circuit absorbs the maximum ripple current from the PWM converter, which is given by Equation (15):

$$I_{RMS\_MAX}=I_{CC\_MAX}\times\frac{\sqrt{V_{SYS\_MIN}\times(V_{IN\_MAX}-V_{SYS\_MIN})}}{V_{IN\_MAX}} \quad (15)$$

For I_{CC_MAX} = 3A, V_{SYS_MIN} = 3.6V, V_{IN_MAX} = 14V, the maximum ripple current is 1.3A. Select the input capacitors so that the temperature rise caused by the ripple current does not exceed 10°C. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use a 10μF capacitor. When input voltage is over 10V, 22uF capacitor is used for C_{IN}.

Besides, usually a small cap with at least 1uF (C1) from IN to GND is required to be put as much close as possible to the IC.

For the input voltage is high to 14V, consider the spike when input insert, select the input capacitors (both the 22uF and 1uF) in 25V rating.

Selecting the Output Capacitor

The output capacitor (C_{SYS}) from the typical application circuit is parallel with the SYS load. C_{SYS} absorbs the high-frequency switching ripple current and smoothes the output voltage. Its impedance must be much less than that of the system load to ensure that it absorbs the ripple current properly.

Ceramic capacitors are recommended for their lower ESR and smaller size, which allows the ESR of the output capacitor to be ignored. The output voltage ripple can be calculated with Equation (16):

$$\Delta r=\frac{\Delta V_{SYS}}{V_{SYS}}=\frac{1-\frac{V_{SYS}}{V_{IN}}}{8\times C2\times f_S^{\,2}\times L}\% \quad (16)$$

To guarantee ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g.: 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

The output capacitor can be calculated with Equation (17):

$$C_{SYS}=\frac{1-\frac{V_{SYS\_MIN}}{V_{IN}}}{8\times f_S^{\,2}\times L\times\Delta r} \quad (17)$$

When SYSFB pin is floating, output voltage ripple is the main concern to select the output capacitor (C_{SYS}), refer to Table 5 for detail selection guide about the SYS capacitance selection under typical inputs.

NOTE:

6) Saturation Current of the inductor should be higher than the IPEAK, add 0.5A margin here.
7) This requirement is for SYS short protection consideration. It could be >3.95A as usual if this feature is not included in the application.

Table 5: SYS Capacitance Selection Guide

SPEC	SYS Capacitance (C_{SYS}) Selection				
V_{IN}	$C_{SYS} = \frac{1-\frac{V_{SYS}}{V_{IN}}}{8 \times f_S^2 \times L \times \Delta r}$	C_{SYS_MIN} (uF) [8] When SYSFB is Floating	C_{SYS_MIN} (uF) [8] When SYSFB is Programmed	Temperature Characteristic	Package
5V	Δr=0.1% L=1uH @V_{IN}=5V L=2.2uH @V_{IN}=9V L=2.2uH @V_{IN}=12V	13.6	20	X5R;X7R	Application Required
9V		13.3	20	X5R;X7R	Application Required
12V		15.5	20	X5R;X7R	Application Required

When SYSFB is programmed using external resistors, the control loop function is changed. A zero point is added around the cross over frequency of the DC gain, and this may result in the phase margin varied a lot, which may cause the unstable operation. To avoid this condition, a minimum capacitance requirement should be satisfied to make the pole point to compensate the zero point. This minimum capacitance is 20uF for a general application.

So, for the SYSFB programmed condition, the C_{SYS} should be selected as max (C_{SYS_MIN}, 20uF), C_{SYS_MIN} is calculated from the formula of equation (17), as shown in Table 5. For better stability margin, select a 47uF ceramic capacitor with 6.3V and above voltage rating as the output capacitor in this case.

Selecting a Resistor for the NTC Sensor

Figure 8 shows an internal resistor divider reference circuit to limit the low temperature threshold and high temperature threshold at V_{THH} and V_{THL}, respectively.

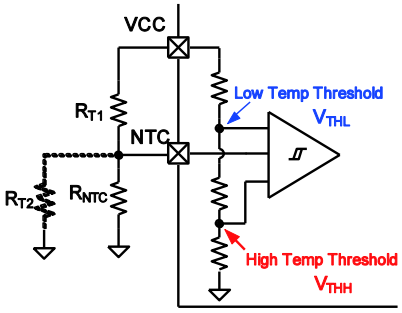


Figure 8: NTC Function Block

For a given NTC thermistor, set the NTC window by selecting appropriate R_{T1} and R_{T2} values with Equation (18) and Equation (19):

$$\frac{R_{T2}//R_{NTC\_Cold}}{R_{T1}+R_{T2}//R_{NTC\_Cold}} = \frac{V_{THL}}{VCC} \quad (18)$$

$$\frac{R_{T2}//R_{NTC\_Hot}}{R_{T1}+R_{T2}//R_{NTC\_Hot}} = \frac{V_{THH}}{VCC} \quad (19)$$

Where R_{NTC_Hot} is the value of the NTC resistor at the high end of the required temperature operation range, and R_{NTC_Cold} is NTC resistor value at a low temperature. The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be programmed independently. With this feature, the MP2617H can fit most NTC resistor types and different temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of NTC resistor used. For example, for the thermistor NCP18XH103, R_{NTC_Cold} is 27.445kΩ at 0°C, and R_{NTC_Hot} is 4.1601kΩ at 50°C.

Equation (18) and Equation (19) can be used to calculate R_{T1} = 7.15kΩ and R_{T2} = 25.5kΩ, assuming that the NTC window is between 0°C and 50°C and using the $\frac{V_{THL}}{VCC}$ and $\frac{V_{THH}}{VCC}$ values from the EC table.

NOTE:

8) For different voltage rating, capacitance will have different DC bias characteristic. Suppose a general condition, capacitance drops 40% under VSYS=4.4V under 10V rating, and 50% at 6.3V rating.

PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. For best performance, follow the guidelines below.

1) Route the power stage adjacent to its ground.
2) Minimize the high-side switching node (SW, inductor) trace lengths in the high-current paths and the current sense resistor trace.
3) Keep the switching node short and away from all small control signals, especially the feedback network.
4) Place the input capacitor as close to IN and PGND as possible.
5) Place the output inductor close to the IC.
6) Connect the output capacitor between the inductor and PGND of the IC.
7) Connect the balls for the power pads (IN, SW, SYS, BATT, and PGND) to as much copper on the board as possible for high-current applications.
   This improves thermal performance because the board conducts heat away from the IC.
8) Connect the PCB ground planes directly to the return of all components through vias.
9) Place vias inside the PGND pads for the IC if possible.

A star ground design approach is used to keep circuit block currents isolated (high-power/low-power small signal), which reduces noise-coupling and ground-bounce issues. A single ground plane with a small layout produces no ground bounce issues, and segregating the components minimizes coupling between signals.

TYPICAL APPLICATION CIRCUITS

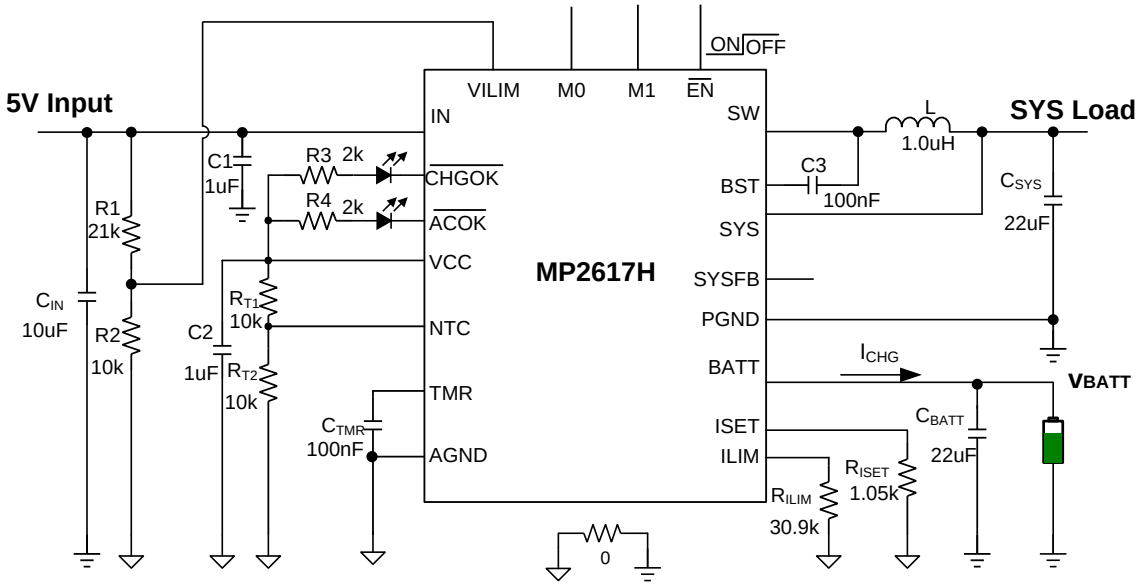


Figure 9: Typical Charge Application Circuit for 5V input

Table 6: The Key BOM of Figure 9.

Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	10μF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	C1	1μF	Ceramic Capacitor;10V; X5R or X7R	0603	Any
1	C2	1uF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
1	C3	100nF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C_{TMR}	100nF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
2	C_{SYS},C_{BATT}	22uF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
2	R_{T1},R_{T2}	10k	Film Resistor;1%	0603	Any
1	L1	1.0μH	Inductor;1.0uH;Low DCR;I_{SAT}>3.95A	SMD	Any

TYPICAL APPLICATION CIRCUITS

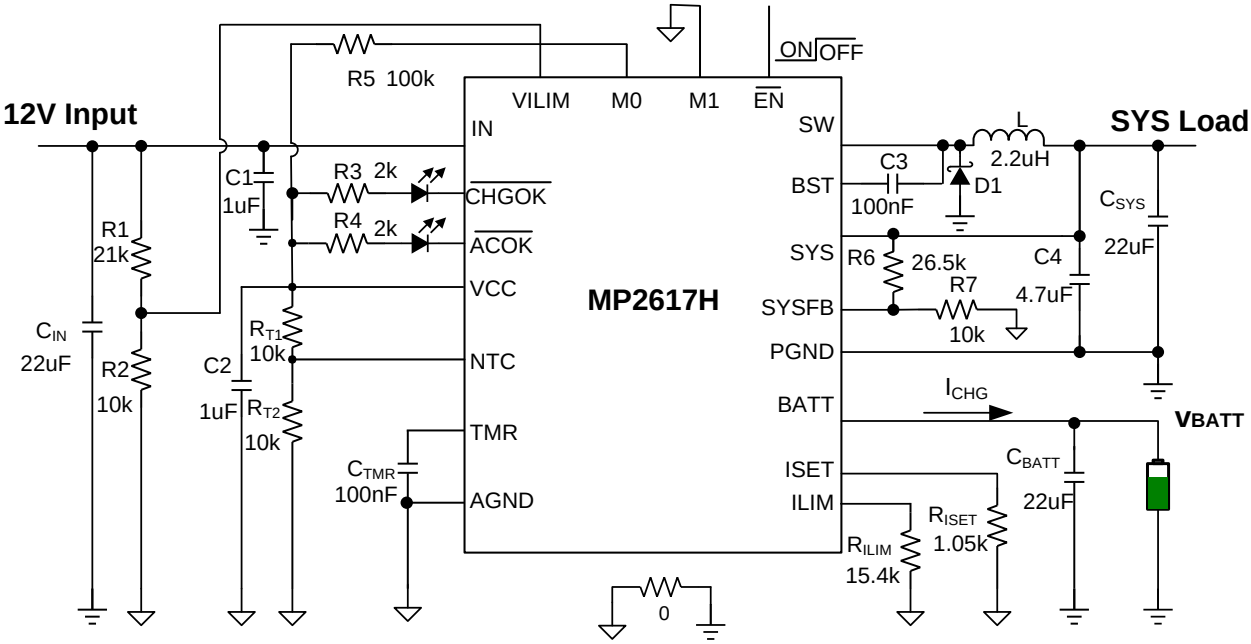


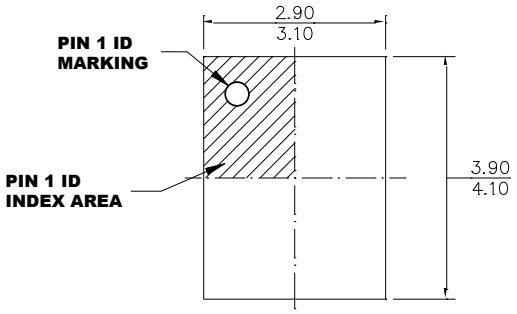
Figure 10: Typical Charge Application Circuit for 12V Input and 3A Total System Load

Table 7: The Key BOM of Figure 10.

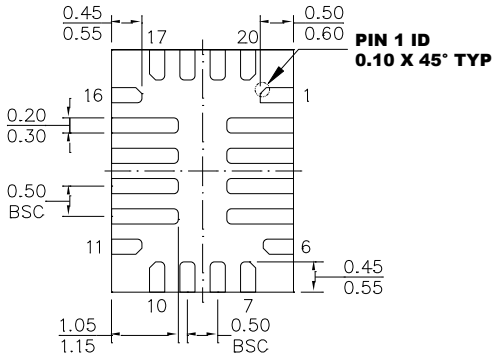
Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	22μF	Ceramic Capacitor;25V; X5R or X7R	1206	Any
1	C1	1μF	Ceramic Capacitor;25V; X5R or X7R	0603	Any
1	C2	1uF	Ceramic Capacitor; 6.3V; X5R or X7R	0603	Any
1	C3	100nF	Ceramic Capacitor;25V; X5R or X7R	0603	Any
1	C4	4.7uF	Ceramic Capacitor;10V; X5R or X7R	0603	Any
1	C_{TMR}	100nF	Ceramic Capacitor; 6.3V;X5R or X7R	0603	Any
2	C_{SYS},C_{BATT}	22uF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	R6	26.5k	Film Resistor;1%	0603	Any
3	R_{T1},R_{T2},R7	10k	Film Resistor;1%	0603	Any
1	L1	2.2μH	Inductor;2.2uH;Low DCR;I_{SAT}>6A	SMD	Any
1	D1	30V,1A	30V,1A,schottky diode	SMD	Any

PACKAGE INFORMATION

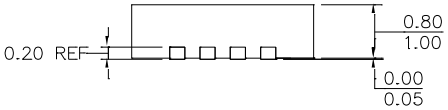
QFN-20 (3mmx4mm)



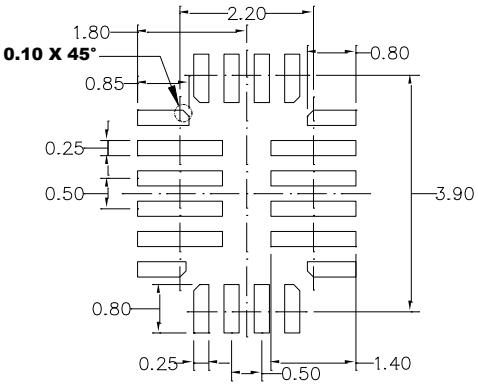
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.