NCP6361

Buck Converter with Bypass Mode for RF Power Amplifiers

The NCP6361, a PWM synchronous step−down DC−to−DC converter, is optimized for supplying RF Power Amplifiers (PAs) used in 3G/4G wireless systems (Mobile / Smart Phones, Tablets,…) powered by single−cell Lithium−Ion batteries. The device is able to deliver up to 2 A current in bypass mode and 800 mA in buck mode. The output voltage is monitorable from 0.4 V to 3.5 V by an analog control pin VCON. The analog control allows dynamically optimizing the RF Power Amplifier's efficiency through the monitoring of the PA output power. With an improved overall system efficiency the communication time and phone autonomy can be consequently increased. At light load for optimizing the DC−to−DC converter efficiency, the NCP6361 enters automatically in PFM mode and operates in a slower switching frequency. The NCP6361 enters in bypass mode when the desired output voltage becomes close to the input voltage (e.g.: low battery conditions). The device operates at 3.429 MHz or 6 MHz switching frequency. This way the system tuning can focus respectively either on a better efficiency (3.249 MHz) or on employing smaller value inductor and capacitors (6 MHz). Synchronous rectification and automatic PFM / PWM / By−Pass operating mode transitions improve overall solution efficiency. The NCP6361 has two versions: NCP6361A and NCP6361B. Version B has a spread spectrum function for low EMI operation. The NCP6361 is available in a space saving, low profile 1.36 x 1.22 mm CSP−9 package.

ON Semiconductor®

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WLCSP9
CASE 567GM

MARKING DIAGRAM

6361x = Specific Device Code
x = A or B
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 19 of this data sheet.

Features

- Input Voltage from 2.5 V to 5.5 V for Battery Powered Applications
- Adjustable Output Voltage (0.4 V to 3.50 V)
- 3.429 / 6 MHz Selectable Switching Frequency
- Uses 470 nH Inductor and 4.7 μF Capacitor for Optimized Footprint and Solution Thickness
- PFM /PWM/Bypass Automatic Mode Change for High Efficiency
- Low 45 μA Quiescent Current
- Thermal Protections to Avoid Damage of the IC
- Small 1.36 x 1.22 mm / 0.4 mm Pitch CSP Package
- This is a Pb−Free Device

Typical Applications

- 3G / 4G Wireless Systems, Smart−Phones and Webtablets

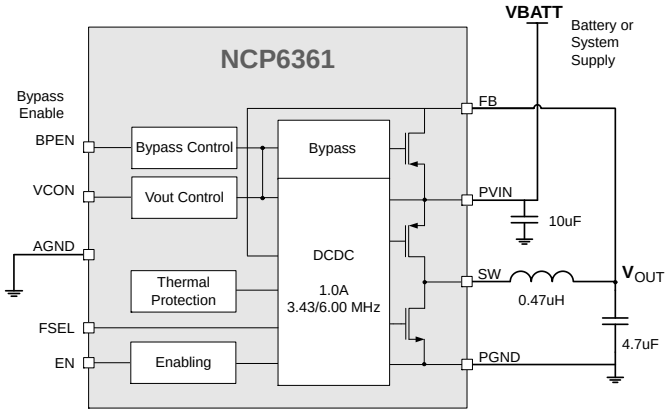


Figure 1. NCP6361 Block Diagram

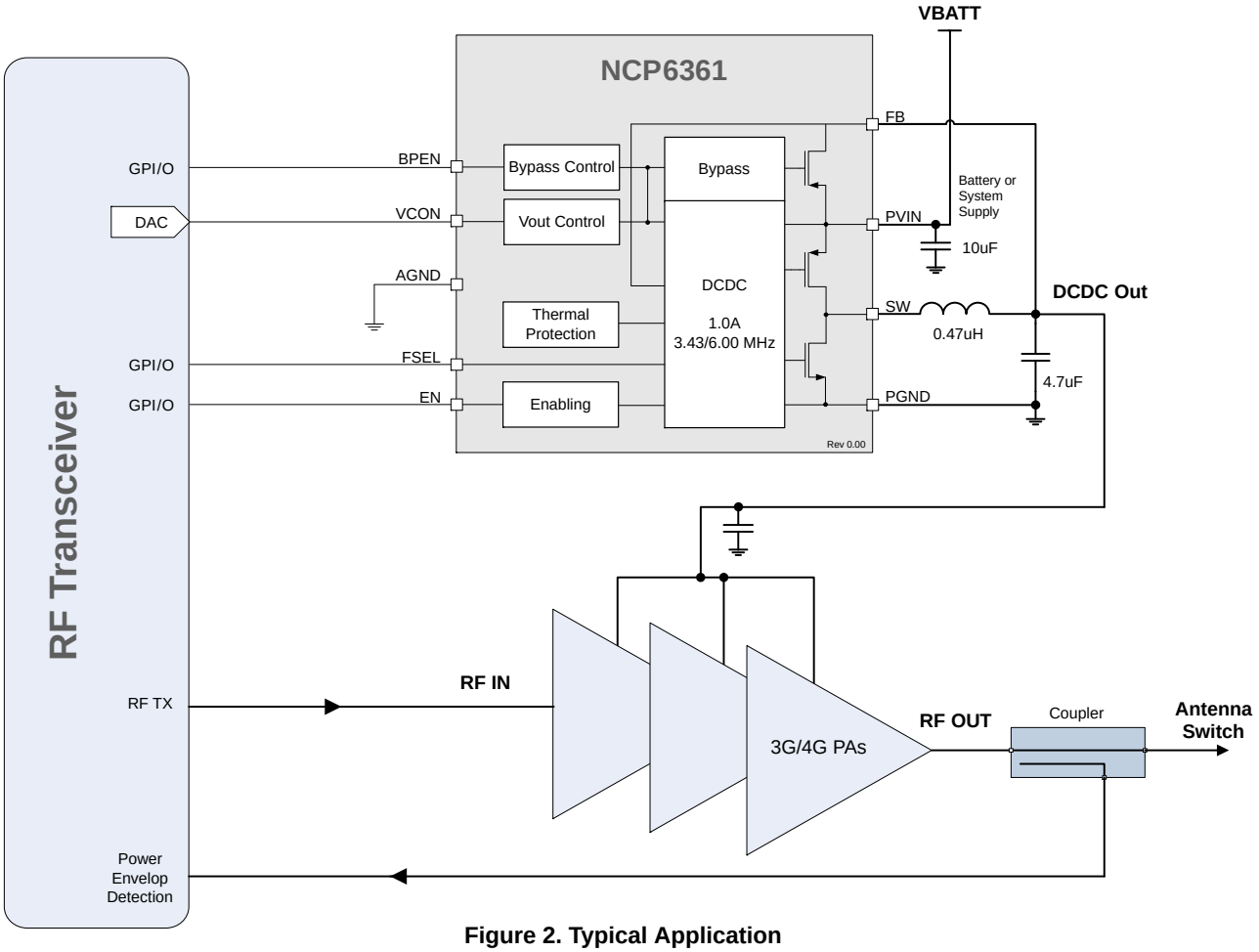


Figure 2. Typical Application

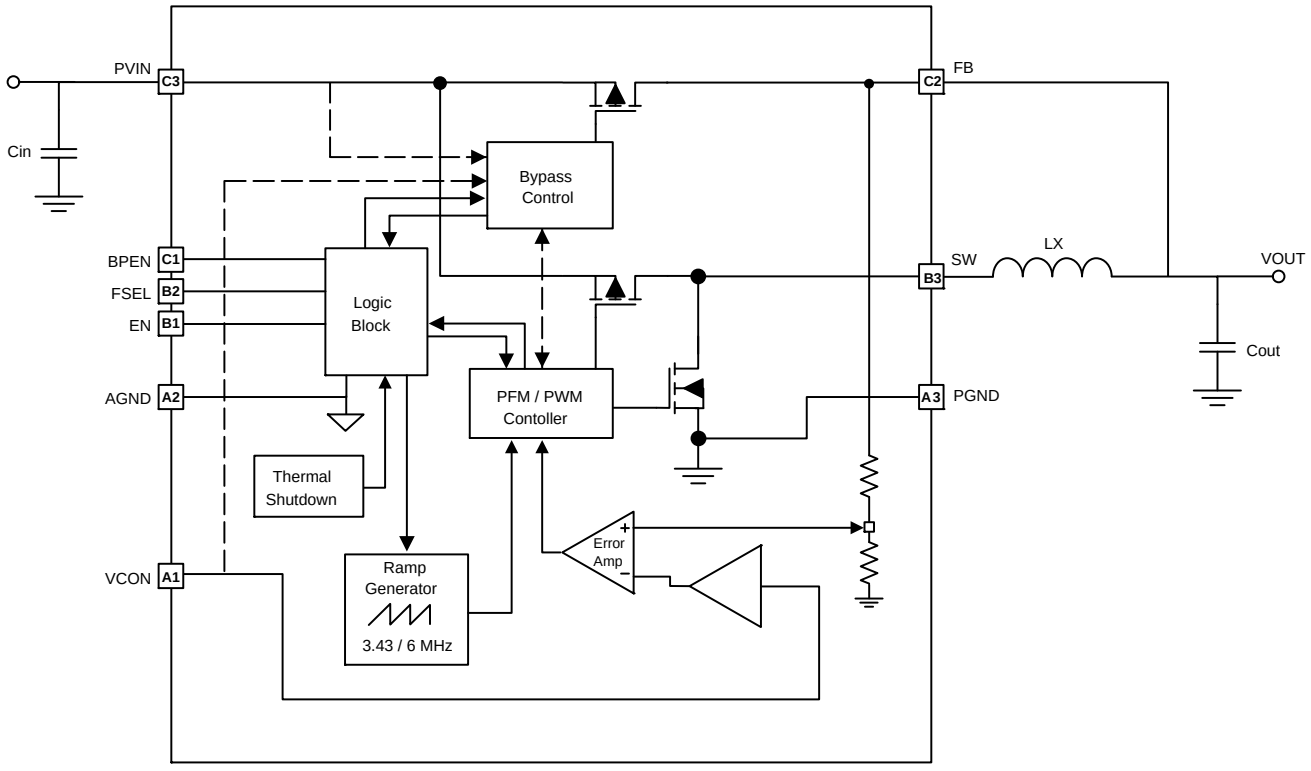


Figure 3. NCP6361 Internal Block Diagram

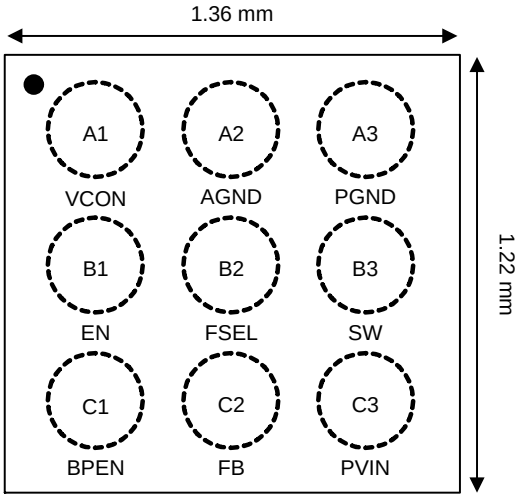


Figure 4. Pin Out (Top View)

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
A1	VCON	Input	Voltage Control Analog Input. This pin controls the output voltage. It must be shielded to protect against noise. V_{OUT} = 2.5 x VCON
A2	AGND	Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
A3	PGND	Ground	DC−DC Power Ground. This pin is the power ground and carries high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local large ground plane is recommended.
B1	EN	Input	Enable Control. Active high will enable the part. There is an internal pull down resistor on this pin.
B2	FSEL	Input	Frequency selection pin. Active low will select 6 MHz switching frequency. Active high will select 3.429 MHz switching frequency. Internal pull−down resistor connected to this pin.
B3	SW	Power Output	DC−DC Switch Power. This pin connects the power transistors to one end of the inductor. Typical application (6 MHz) uses 0.470 μH inductor; refer to application section for more information.
C1	BPEN	Input	Bypass Enable Pin. Set a high level to force bypass mode. Set a low level for auto−bypass mode. Internal pull−down resistor connected to this pin.
C2	FB	Power Input	DCDC Feedback Voltage. Must be connected to the output capacitor positive terminal. This is the input to the error amplifier.
C3	PV_{IN}	Power Input	DCDC Power Supply. This pin must be decoupled to ground by a 10 μF and 1 μF ceramic capacitor. These capacitors should be placed as close as possible to this pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog and power pins: PV_{IN}, SW, FB	V_A	−0.3 to + 7.0	V
VCON pin	V_{VCON}	−0.3 to + 2.5	V
Digital pins: EN, BPEN & FSEL: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A +0.3 ≤ 7.0 10	 V mA
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range (Note 1)	T_J	−40 to +125	°C
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Thermal Resistance Junction−to−Ambient (Note 2)	$R_{\theta JA}$	85	°C/W
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal shutdown set to 165°C (typical) avoids potential irreversible damage on the device due to power dissipation.
2. The Junction−to−Ambient thermal resistance is a function of Printed Circuit Board (PCB) layout and application. This data is measured using 4−layer PCBs (2s2p). For a given ambient temperature T_A it has to be pay attention to not exceed the max junction temperature T_{JMAX}.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PV_{IN}	Power Supply (Note 4)		2.5		5.5	V
L	Inductor for DCDC converter (Note 5)	F = 6 MHz		0.47		μH
Co	Output Capacitor for DCDC Converter (Note 5)	F = 6 MHz, L = 0.47 μH	4.7	−	33	μF
Co	Output Capacitor for DCDC Converter (Note 5)	F = 6 MHz, L = 0.33 μH	33	−	220	μF
L	Inductor for DCDC converter (Note 5)	F = 3.429 MHz		1		μH
Co	Output Capacitor for DCDC Converter (Note 5)	F = 3.429 MHz, L = 1 μH	4.7	−	33	μF
Co	Output Capacitor for DCDC Converter (Note 5)	F = 3.429 MHz, L = 0.47 μH	33	−	220	μF
Cin	Input Capacitor for DCDC Converter (Note 5)		4.7	10		μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Operation above 5.5 V input voltage for extended period may affect device reliability.
5. Including de−ratings (refer to application information section of this document for further details)

ELECTRICAL CHARACTERISTICS

Min and Max Limits apply for T_A up to +85°C unless otherwise specified. PV_{IN} = 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and default configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PIN PV_{IN}						
I_Q	Operating quiescent current	DCDC on – no load – no switching, EN = High T_A = up to +85°C	−	45	60	μA
I_{SLEEP}	Product sleep mode current	PV_{IN} = 2.5 V to 5.5 V V_{CON} < 0.1 V, EN = High T_A = up to +85°C	−	55	70	μA
I_{OFF}	Product off current	EN = Low PV_{IN} = 2.3 V to 5.5 V T_A = up to +85°C	−	0.9	3	μA
DCDC CONVERTER						
PV_{IN}	Input Voltage Range		2.5	−	5.5	V
V_{OUT_MIN}	Minimum Output Voltage	V_{CON} = 0.16 V (Note 8)	0.35	0.40	0.45	V
V_{OUT_MAX}	Maximum Output Voltage	V_{CON} = 1.40 V (Note 8)	3.45	3.50	3.55	V
Gain	V_{CON} to V_{OUT} Gain			2.5		V/V
V_{OUT_ACC}	V_{OUT} Accuracy	Ideal = 2.5 x V_{CON}	−50 −3		+50 +3	mV %
F_{SW1}	Switching Frequency	FSEL = 0	5.4	6	6.6	MHz
F_{SW2}	Switching Frequency	FSEL = 1	3.085	3.429	3.772	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PV_{IN} to SW T_J up to +85°C, PV_{IN} = 3.6 V	−	177	−	mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW1 to PGND T_J up to 85°C, PV_{IN} = 3.6 V	−	100	−	mΩ
R_{ONBP}	BP MOSFET On Resistance	From PV_{IN} to FB T_J up to 85°C, PV_{IN} = 3.6 V	−	217	−	mΩ
I_{PKHS}	Peak Inductor Current PMOS		−	1.4	−	A
I_{PKLS}	Peak Inductor Current NMOS		−	1.0	−	A
DC_{MAX}	Maximum Duty Cycle		−	100	−	%
η	Efficiency	PV_{IN} = 3.6 V, V_{OUT} = 0.8 V I_{OUT} = 10 mA, PFM mode PV_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{OUT} = 200 mA, PWM mode PV_{IN} = 3.9 V, V_{OUT} = 3.3 V I_{OUT} = 500 mA, PWM mode		75 90 95		% % %
$LINE_{TR}$	Line Transient Response	PV_{IN} = 3.6 V to 4.2 V I_{OUT} = 100 mA, V_{OUT} = 0.8 V T_R = T_F = 10 μs		50		mV_{pk}
$LOAD_{TR}$	Load Transient Response	PV_{IN} = 3.1 V / 3.6 V / 4.5 V I_{OUT} = 50 to 150 mA T_R = T_F = 0.1 μs		50		mV_{pk}
$V_{CON\_BP\_EN}$	Vcon Forced Bypass Mode Enter		1.6			V
$V_{CON\_BP\_EX}$	Vcon Forced Bypass Mode Exit				1.4	V

6. Guaranteed by design and characterized.
7. Operation above 5.5 V input voltage for extended periods may affect device reliability.
8. Tested and guaranteed by correlation.

ELECTRICAL CHARACTERISTICS

Min and Max Limits apply for T_A up to +85°C unless otherwise specified. PV_{IN} = 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and default configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EN, BPEN						
V_{IH}	Positive Going Input High Voltage Threshold		1.1	−	−	V
V_{IL}	Negative Going Input Low Voltage Threshold		−	−	0.4	V
TOTAL DEVICE						
I_{OUTMAX}	PWM mode (Note 6)		800			mA
	BP mode (Note 6)		2000			mA
T_{VCON}	V_{OUT} step rise time	PV_{IN} = 3.6 V, V_{OUT} = 1.4 V to 3.4 V, C_{OUT} = 4.7 μF, R_L = 12 Ω, T_{R_VCON} < 1 μs		8		μs
	V_{OUT} step fall time	PV_{IN} = 3.6 V, V_{OUT} = 3.4 V to 1.4 V, C_{OUT} = 4.7 μF, R_L = 12 Ω, T_{F_VCON} < 1 μs		6		μs
T_{START}	Soft−Start Time (Time from EN transitions from Low to High to 90% of Output Voltage)	PV_{IN} = 4.2 V, C_{OUT} = 4.7 μF, V_{OUT} = 3.4 V, no load (Note 8)	−	50	90	μs
T_{SP_en}	Sleep mode Enter Time	VCON < 75 mV	−	4	−	μs
T_{SP_ex}	Sleep mode Exit Time	VCON > 75 mV	−	5	−	μs
V_{BPNEG}	Auto Bypass Detection Negative threshold	$PV_{IN} – V_{OUT}$		200		mV
V_{BPPOS}	Auto Bypass Detection Positive threshold	$PV_{IN} – V_{OUT}$		320		mV
V_{UVLO}	Under Voltage Lockout	PV_{IN} falling	−	−	2.4	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	PV_{IN} rising − PV_{IN} falling	60	−	200	mV
T_{SD}	Thermal Shut Down Protection		−	155	−	°C
T_{SDH}	Thermal Shut Down Hysteresis		−	30	−	°C

6. Guaranteed by design and characterized.
7. Operation above 5.5 V input voltage for extended periods may affect device reliability.
8. Tested and guaranteed by correlation.

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

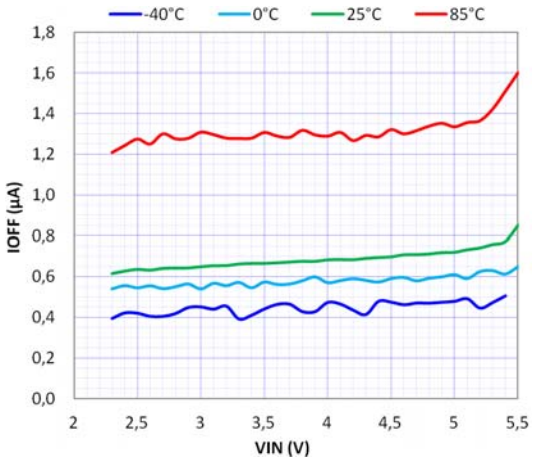


Figure 5. Shutdown Current vs Input Voltage (EN = Low, VCON = 0 V)

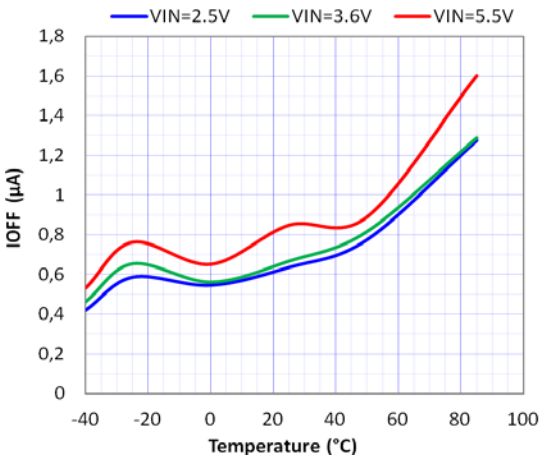


Figure 6. Shutdown Current vs Temperature (T_A) (EN = Low, VCON = 0 V)

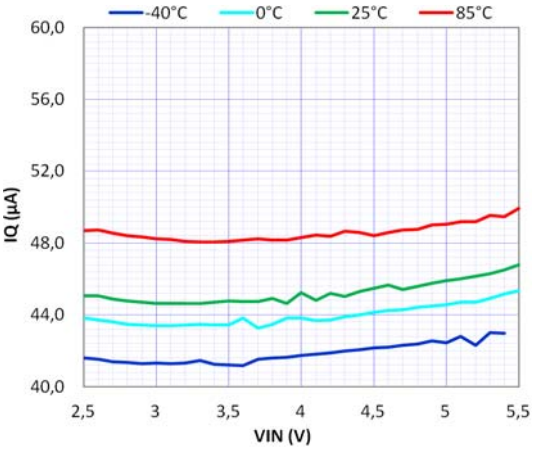


Figure 7. Quiescent Current vs. Input Voltage (EN = High, VCON = 0.8 V, V_{OUT} = 2 V)

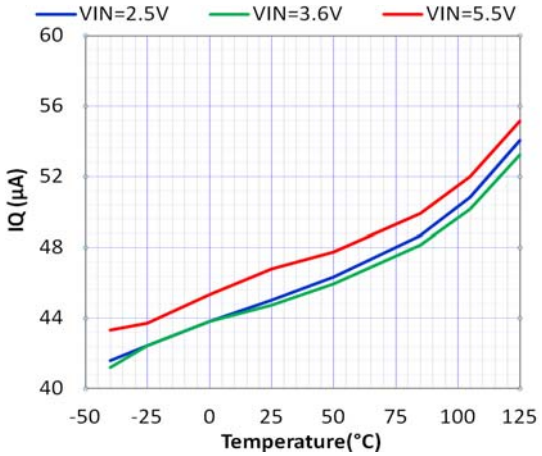


Figure 8. Quiescent Current vs Temperature (T_A) (EN = High, VCON = 0.8 V, V_{OUT} = 2 V)

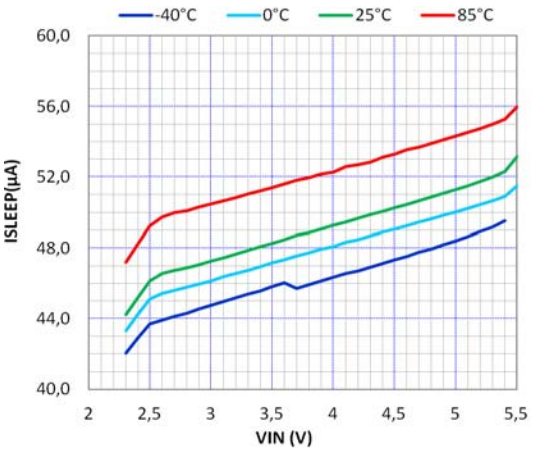


Figure 9. Sleep Mode Current vs. Input Voltage (EN = High, VCON = 0 V, V_{OUT} = 0 V)

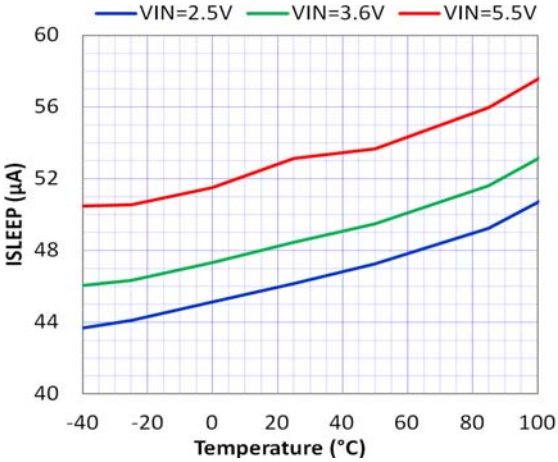


Figure 10. Sleep Mode Current vs. Temperature (T_A) (EN = High, VCON = 0 V, V_{OUT} = 0 V)

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

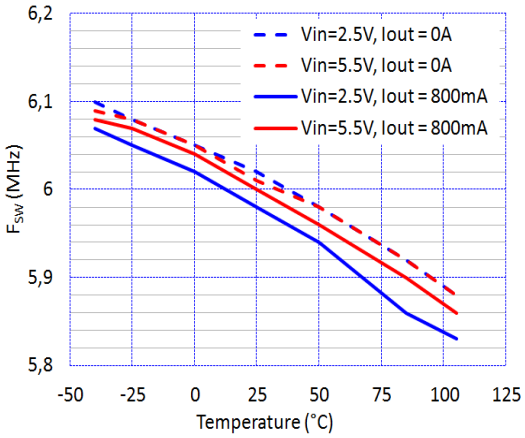


Figure 11. 6 MHz Switching Frequency Variation (Fsw) vs. Temperature

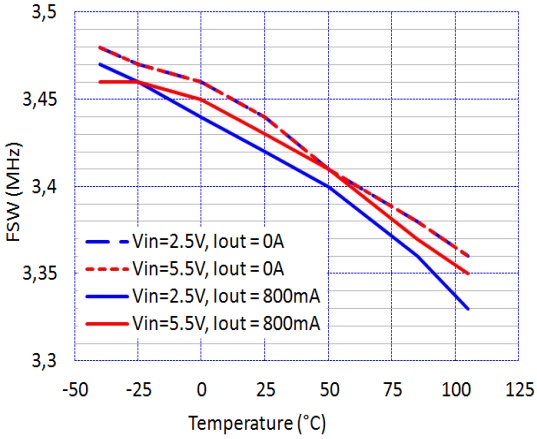


Figure 12. 3.429 MHz Switching Frequency Variation (Fsw) vs. Temperature (L = 1 μH)

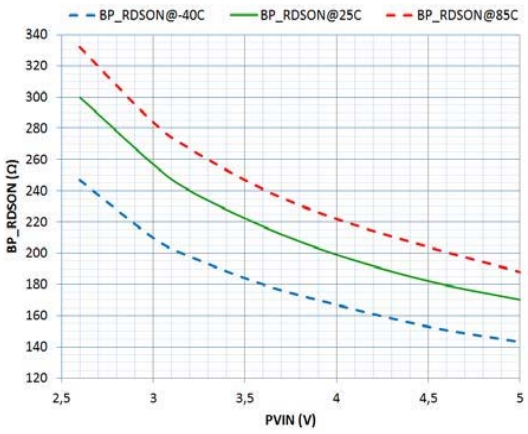


Figure 13. By−Pass PMOS $R_{DS(on)}$ vs. PV_{IN} and Temperature

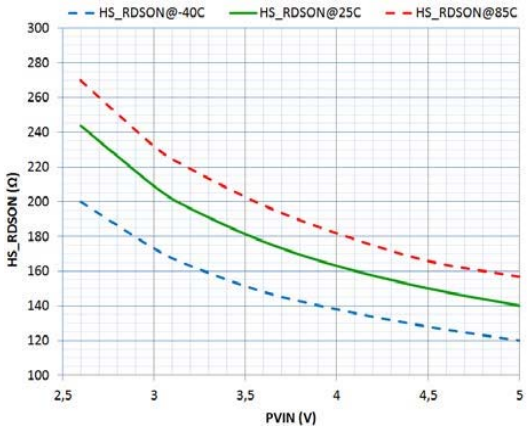


Figure 14. High−Side PMOS $R_{DS(on)}$ vs. PV_{IN} and Temperature

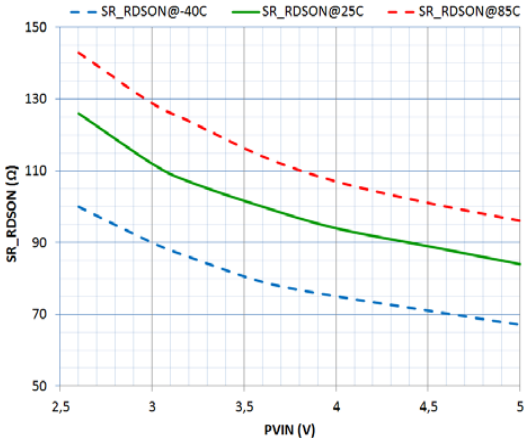


Figure 15. Low−Side NMOS $R_{DS(on)}$ vs. PV_{IN} and Temperature

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

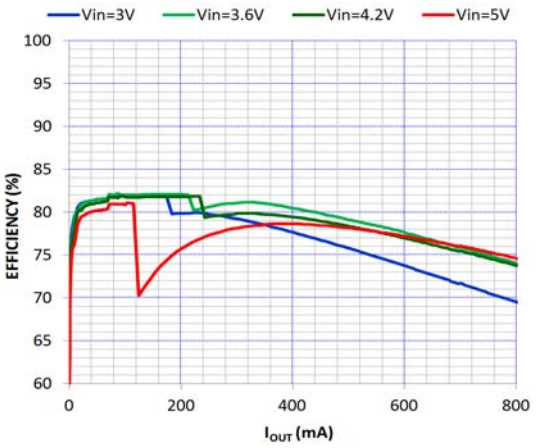


Figure 16. Efficiency vs Output Current vs PV_{IN} @25°C, Fsw = 6 MHz, V_{OUT} = 0.8 V

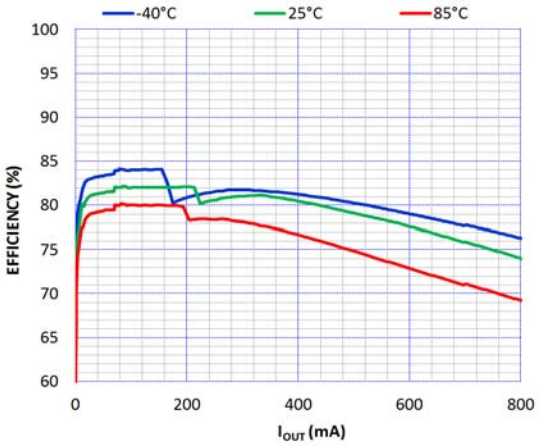


Figure 17. Efficiency vs Output Current vs Temperature PV_{IN} = 3.6 V, Fsw = 6 MHz, V_{OUT} = 0.8 V

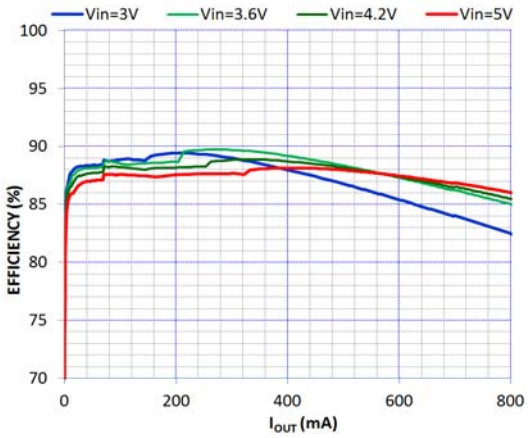


Figure 18. Efficiency vs Output Current vs PV_{IN} @25°C, Fsw = 6 MHz, V_{OUT} = 1.8 V

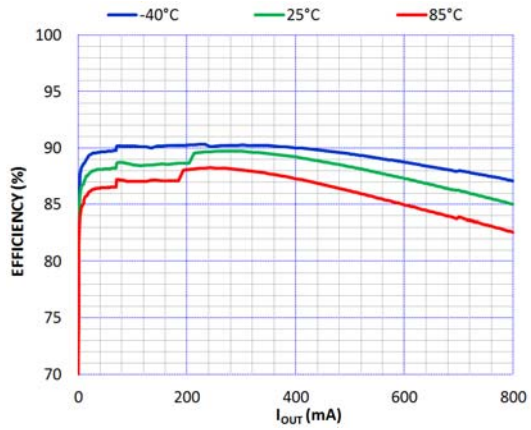


Figure 19. Efficiency vs Output Current vs Temperature PV_{IN} = 3.6 V, Fsw = 6 MHz, V_{OUT} = 1.8 V

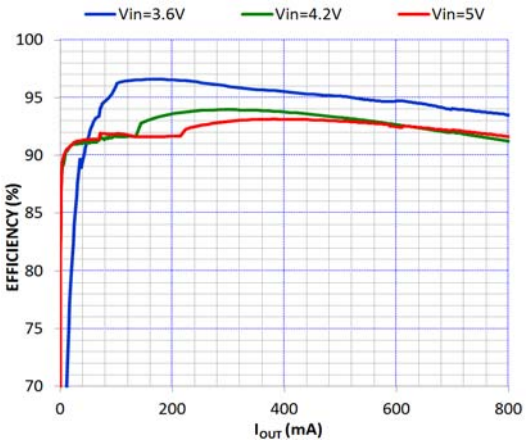


Figure 20. Efficiency vs Output Current vs PV_{IN} @25°C, Fsw = 6 MHz, V_{OUT} = 3.3 V

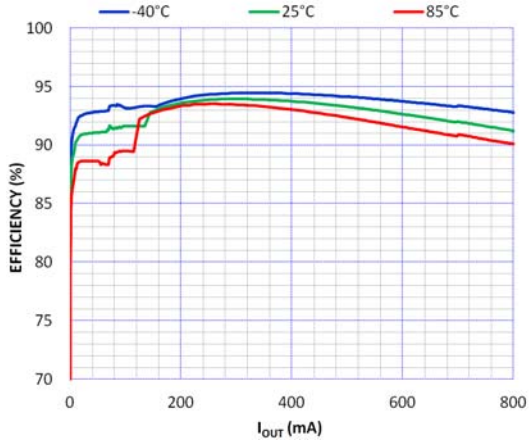


Figure 21. Efficiency vs Output Current vs Temperature PV_{IN} = 3.6 V, Fsw = 6 MHz, V_{OUT} = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 1 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 3.429 MHz, T_A = 25°C (unless otherwise noted)

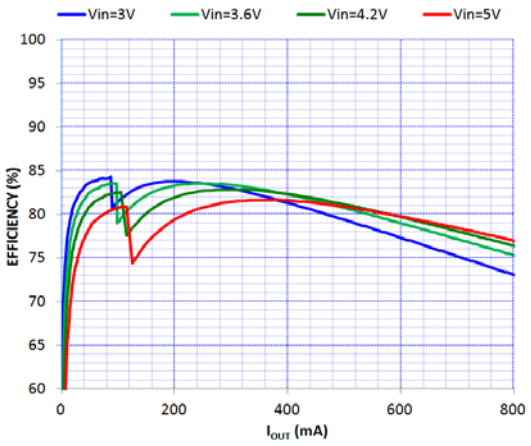


Figure 22. Efficiency vs Output Current vs PV_{IN} @25°C, Fsw = 3.429 MHz, V_{OUT} = 0.8 V

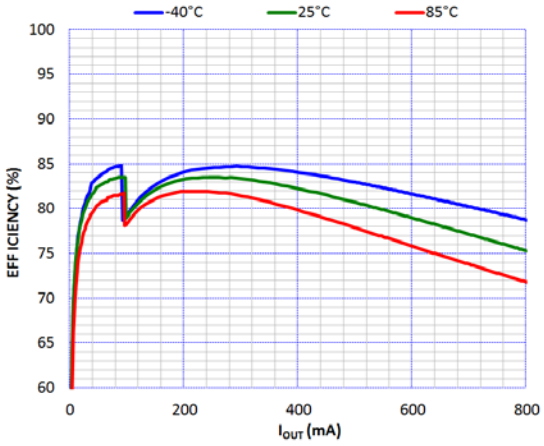


Figure 23. Efficiency vs Output Current vs Temperature PV_{IN} = 4.2 V, Fsw = 3.429 MHz, V_{OUT} = 0.8 V

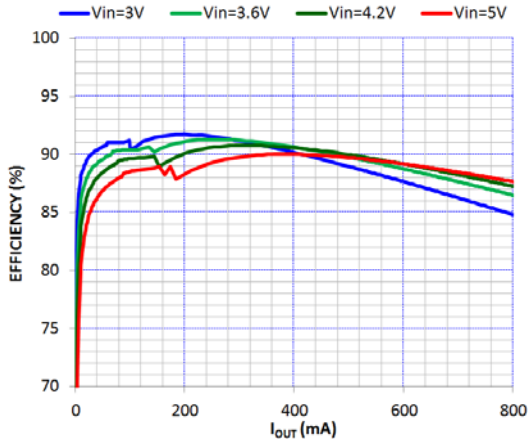


Figure 24. Efficiency vs Output Current vs PV_{IN} @25°C, Fsw = 3.429 MHz, V_{OUT} = 1.8 V

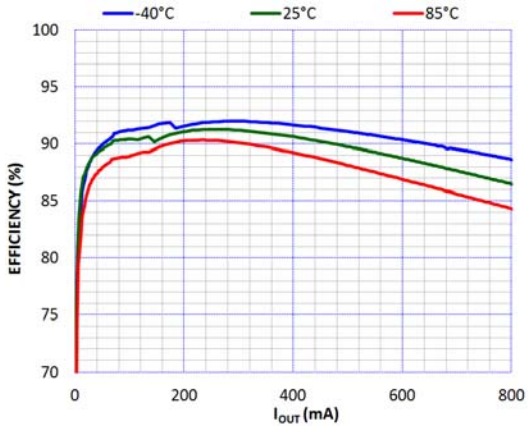


Figure 25. Efficiency vs Output Current vs Temperature PV_{IN} = 4.2 V, Fsw = 3.429 MHz, V_{OUT} = 1.8 V

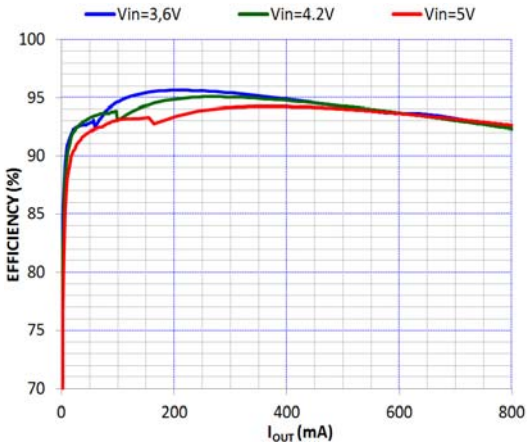


Figure 26. Efficiency vs Output Current vs PV_{IN} @25°C, Fsw = 3.429 MHz, V_{OUT} = 3.3 V

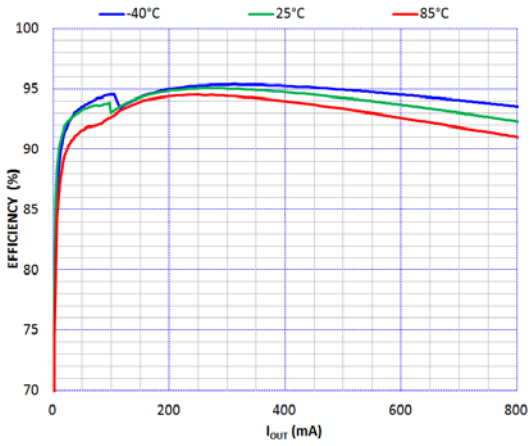


Figure 27. Efficiency vs Output Current vs Temperature PV_{IN} = 4.2 V, Fsw = 3.429 MHz, V_{OUT} = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

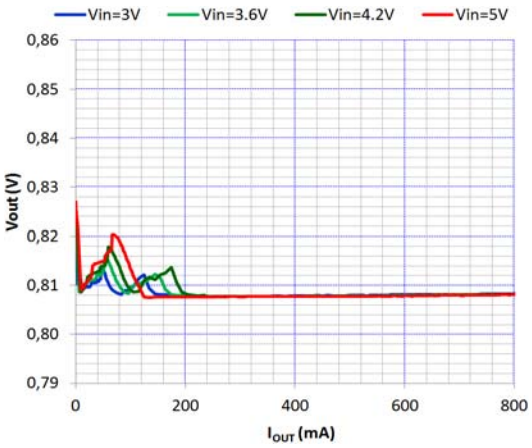


Figure 28. V_{OUT} Accuracy vs Output Current vs PV_{IN} @ 25°C, FSW = 6 MHz, V_{OUT} = 0.8 V

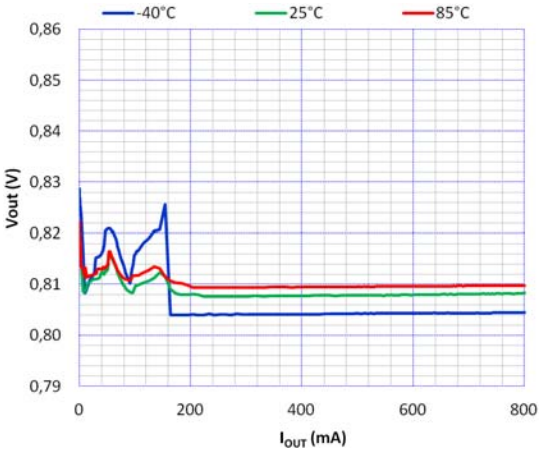


Figure 29. V_{OUT} Accuracy vs Output Current vs Temperature PV_{IN} = 3.6 V, FSW = 6 MHz, V_{OUT} = 0.8 V

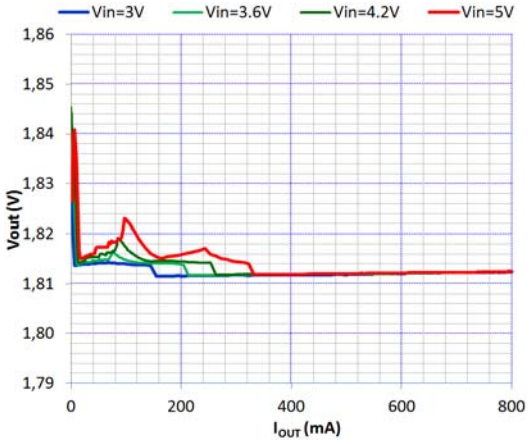


Figure 30. V_{OUT} Accuracy vs Output Current vs PV_{IN} @ 25°C, FSW = 6 MHz, V_{OUT} = 1.8 V

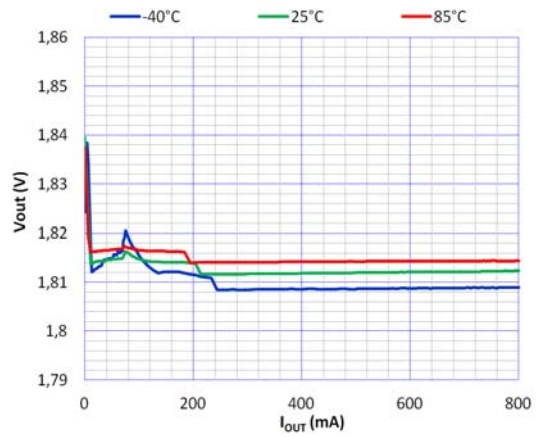


Figure 31. V_{OUT} Accuracy vs Output Current vs Temperature PV_{IN} = 3.6 V, FSW = 6 MHz, V_{OUT} = 1.8 V

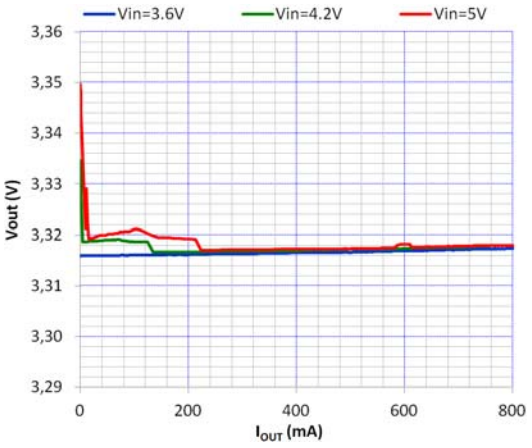


Figure 32. V_{OUT} Accuracy vs Output Current vs PV_{IN} @ 25°C, FSW = 6 MHz, V_{OUT} = 3.3 V

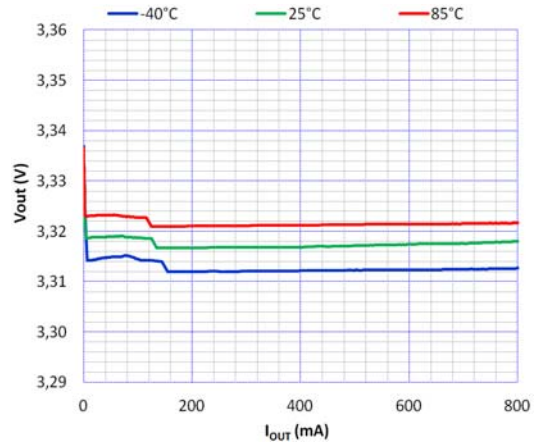


Figure 33. V_{OUT} Accuracy vs Output Current vs Temperature PV_{IN} = 3.6 V, FSW = 6 MHz, V_{OUT} = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 1 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{SW} = 3.429 MHz, T_A = 25°C (unless otherwise noted)

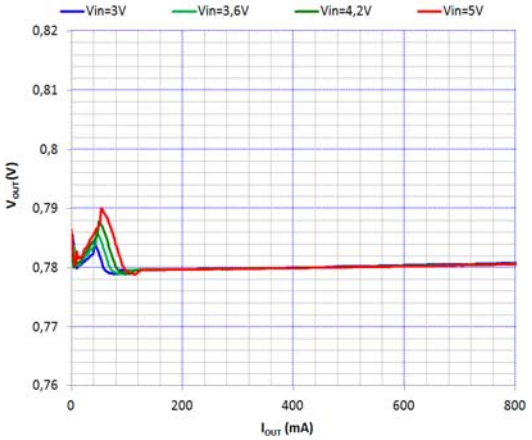


Figure 34. V_{OUT} Accuracy vs Output Current vs PV_{IN} @ 25°C, FSW = 3.429 MHz, V_{OUT} = 0.8 V

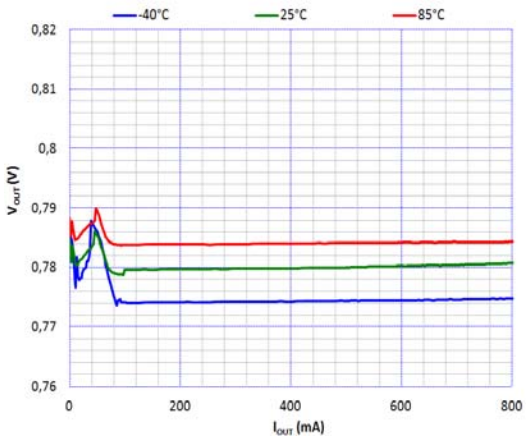


Figure 35. V_{OUT} Accuracy vs Output Current vs Temperature PV_{IN} = 4.2 V, FSW = 3.429 MHz, V_{OUT} = 0.8 V

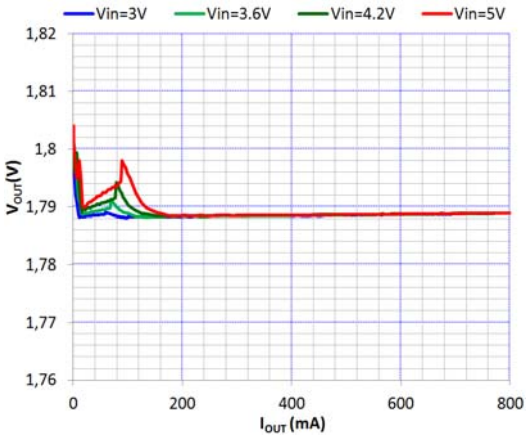


Figure 36. V_{OUT} Accuracy vs Output Current vs PV_{IN} @ 25°C, FSW = 3.429 MHz, V_{OUT} = 1.8 V

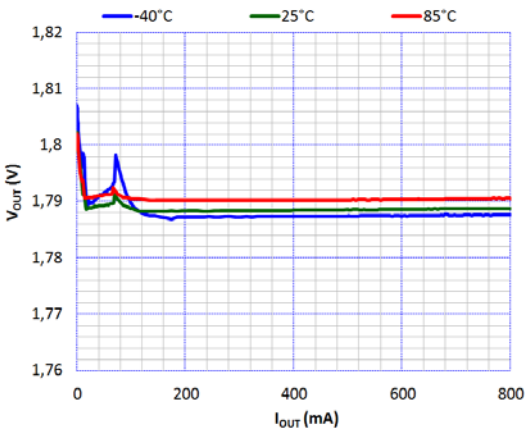


Figure 37. V_{OUT} Accuracy vs Output Current vs Temperature PV_{IN} = 4.2 V, FSW = 3.429 MHz, V_{OUT} = 1.8 V

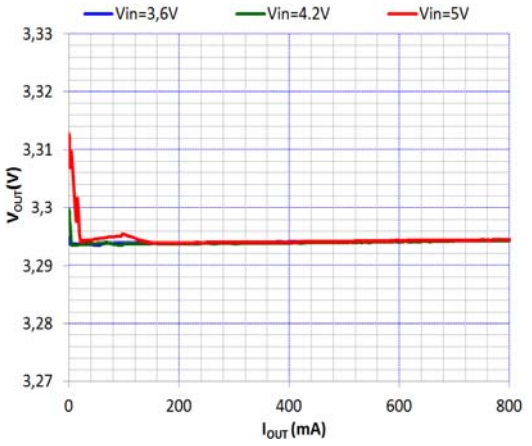


Figure 38. V_{OUT} Accuracy vs Output Current vs PV_{IN} @ 25°C, FSW = 3.429 MHz, V_{OUT} = 3.3 V

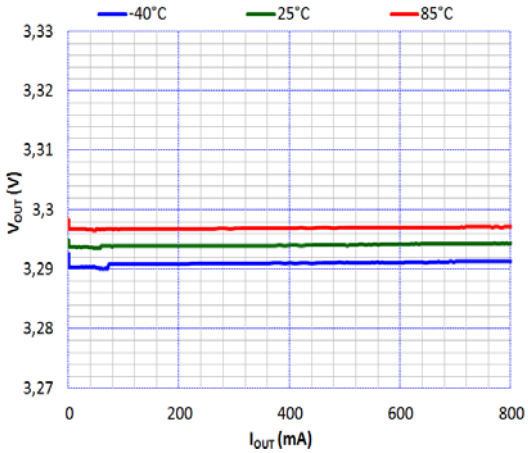


Figure 39. V_{OUT} Accuracy vs Output Current vs Temperature PV_{IN} = 3.6 V, FSW = 3.429 MHz, V_{OUT} = 3.3 V

TYPICAL OPERATING CHARACTERISTIC

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

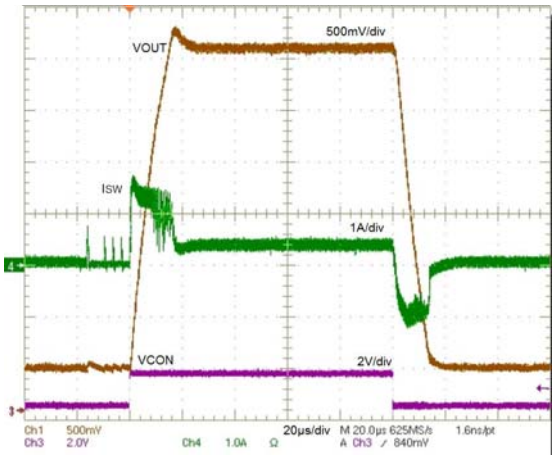


Figure 40. Transient Response V_{OUT} vs VCON
R_L = 10 Ω, V_{OUT} = 0.4 V to 3.5 V, PV_{IN} = 3.9 V

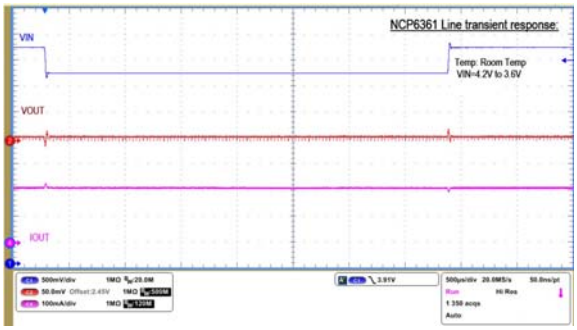


Figure 41. Line Transient Response
PV_{IN} = 3.6 V to 4.2 V, R_L = 10 Ω, V_{OUT} = 2.5 V

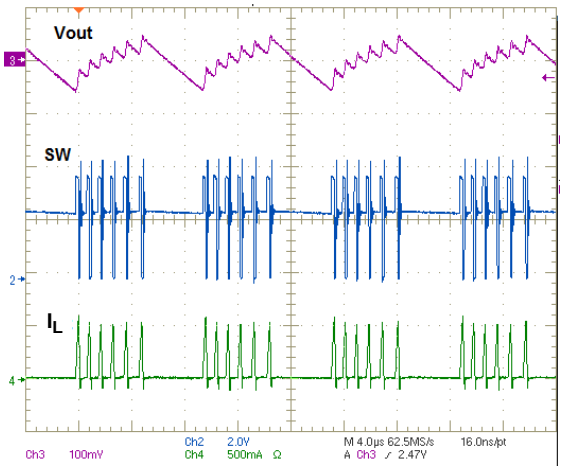


Figure 42. Output Voltage Waveforms in PFM Mode
I_{OUT} = 50 mA, V_{OUT} = 2.5 V

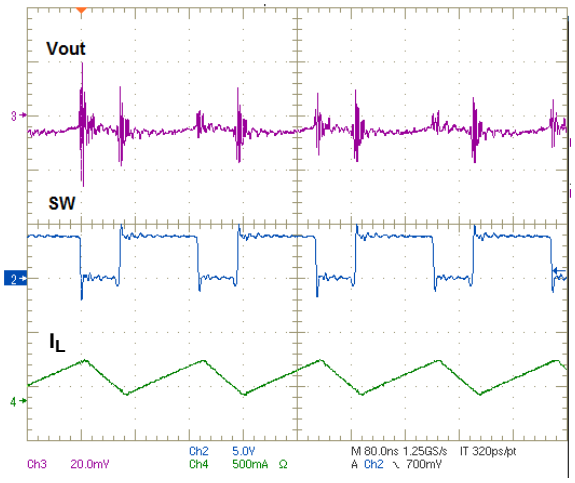


Figure 43. Output Voltage Waveforms in PWM Mode
I_{OUT} = 250 mA, V_{OUT} = 2.5 V

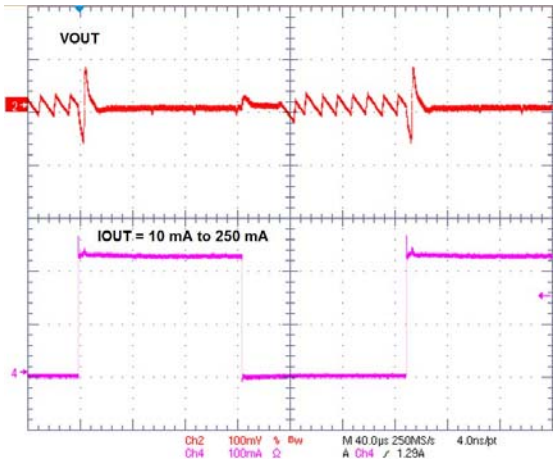


Figure 44. Load Transient Response
I_{OUT} = 10 to 250 mA, V_{OUT} = 2.5 V

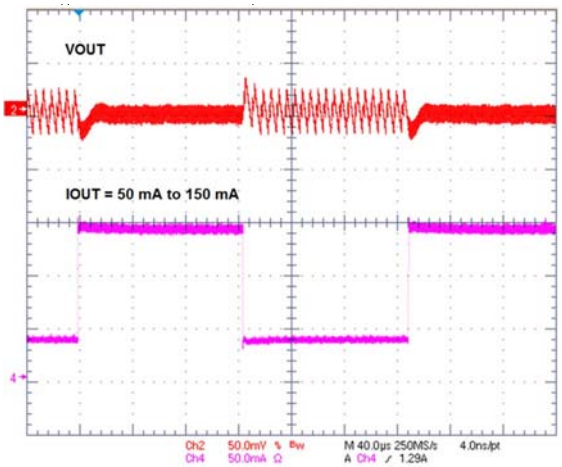


Figure 45. Load Transient Response
I_{OUT} = 50 mA to 150 mA, V_{OUT} = 0.8 V

TYPICAL OPERATING CHARACTERISTICS

(Results based on silicon Rev1.0 – Rev 1.1 to come)

PV_{IN} = EN = 3.7 V, L = 0.47 μH, Cout = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

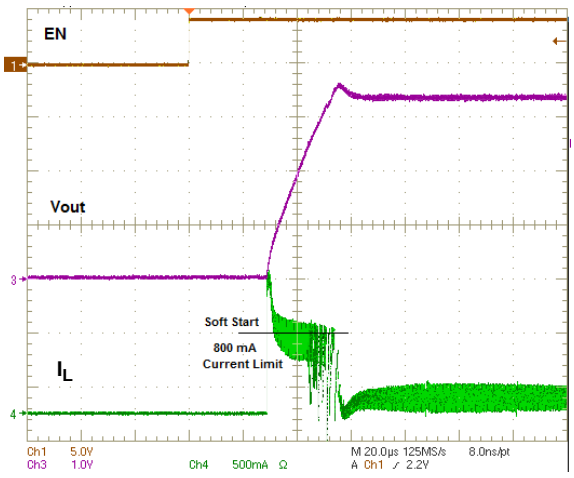


Figure 46. Power−up Transient Response
PV_{IN} = 3.9 V, Vout = 3.4 V, Iout = 150 mA

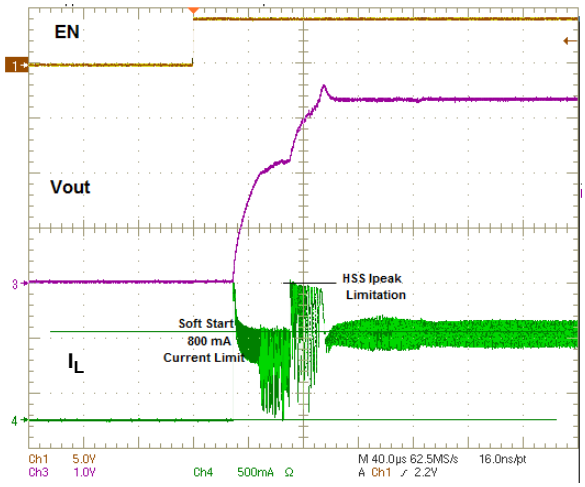


Figure 47. Power−up Transient Response
PV_{IN} = 3.9 V, Vout = 3.4 V, Iout = 800 mA

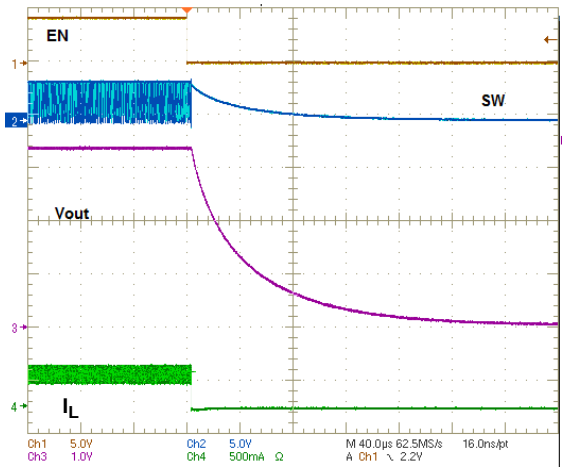


Figure 48. Power−down Transient Response
PV_{IN} = 3.7 V, Vout = 3.4 V, RL = 10 Ω

OPERATING DESCRIPTION

General Description

The NCP6361 is a voltage−mode standalone synchronous step−down DC−to−DC converter designed to supply RF Power Amplifiers (PAs) used in 3G/4G wireless systems (Mobile / Smart Phones, Tablets, …) powered by single−cell Lithium−Ion batteries. The IC can deliver up to 800 mA when operating in PWM mode and up to 2 A when in by−pass operating mode.

The buck converter output voltage ranging from 0.4 V to 3.5 V can be monitored by the system's PA output RF power through the control pin VCON. The control voltage range is from 0.16 V to 1.4 V and Vout is equal to 2.5 times this control voltage. VCON allows the PA to have its efficiency dynamically optimized during communication calls in the case for example of roaming situation or data transmission involving a constant adjustment of the PA output power. The value−added benefit is an increase of the absolute talk time.

Synchronous rectification and automatic PFM / PWM / By−Pass operating mode transitions improve overall solution efficiency. The device operates at 3.429 MHz or 6 MHz switching frequency. This way tuning the DC−to−DC converter can focus respectively either on a better efficiency (3.429 MHz) or on employing smaller value inductor and capacitors (6 MHz). These two switching frequencies are selectable using a dedicated pin FSEL.

A By−pass mode is also supported and is enable automatically or can be forced through the BPEN pin. The output voltage is the copy of the battery input voltage minus a drop−out voltage resulting from the By−Pass MOSFET transistor's low on−state resistance in parallel with the High−Side FET RDSON resistance added to the inductor series resistance.

Protections are also implemented for preventing the device against over−current or short−circuit event or over junction temperature situation.

Buck DC−to−DC Converter Operating

The converter is a synchronous rectifier type with both high side and low side integrated switches. In addition it includes a by−pass MOSFET transistor. Neither external transistor nor diodes are required for NCP6361 operation. Feedback and compensation network are also fully integrated. The device can operate in five different modes: shutdown mode (EN = Low, device off), Sleep Mode when VCON below about 0.1 V, PFM mode for efficiency optimization purpose when operating at light load, PWM mode when operating in medium and high loads and Bypass mode when PV_{IN} (Vbatt) is close to Vout (low battery situation). The transitions between PWM, PFM and By−pass modes occur automatically.

Shutdown Mode

The NCP6361 enters shutdown mode when setting the EN pin Low (below 0.4 V) or when PV_{IN} drops below its UVLO threshold value. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. The typical current consumption is 0.9 μA. Applying a voltage above 1.1 V to EN pin will enable the device for normal operation. A soft−start sequence is run when activating EN high. EN pin should be activated after the input voltage is applied.

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, the NCP6361 operates in PWM mode from a fixed clock (3.43 MHz or 6 MHz) and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM. The internal N−MOSFET switch operates as synchronous rectifier and is driven complementary to the P−MOSFET switch. In CCM, the lower switch (N−MOSFET) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the NCP6361 operates in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N−MOSFET operates as synchronous rectifier after each P−MOSFET on−pulse. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM mode.

By−Pass Operating Mode

The NCP6361 has been designed to manage low battery conditions when PV_{IN} or VBAT becomes close to the required Vout output voltage. In that case the NCP6361 enters By−pass Operating mode (or wire mode). To this end a specific low resistance on−state By−Pass MOSFET is included and activated while the buck converter low side N−MOSFET is set off. The PA is then directly powered by the battery. The output voltage is the copy of the input voltage minus a drop−out voltage resulting from the resistance of the BP MOSFET in parallel with the High−Side P−MOSFET plus the inductor: the consequence is a resulting resistance smaller than the available one − P−MOSFET + inductor − when in PWM mode and 100% duty cycle. In that specific case the By−pass mode offers a better efficiency.

The By−pass mode is triggered automatically when PV_{IN} = V_{OUT} + 200 mV typically. The NCP6361 exit automatically the By−pass mode when PV_{IN} = V_{OUT} + 320 mV typically. Nevertheless it is possible to force the By−pass mode by setting the pin BPEN High. In By−Pass mode the NCP6361 is capable to source a current of up to 2 A.

Sleep Mode

The NCP6361 device enters the sleep mode in about 4μs when the control voltage VCON goes below typically 70 mV. Vout is extremely low, close to 0 V and in a state out of regulation. In this Vout condition the Sleep mode enables a low current state (55 μA typical range). The buck converter exits the sleep mode and returns in a regulation state when VCON goes above 110 mV after typically 5 μs.

Inductor Peak Current limitations

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrain inductor power. The High Side Switch (HSS) peak current limitation is typically 1.4 A, while the Low Side Switch (LSS) has a peak current up to 1.0 A. The HSS peak current contributes to limit the current during soft start sequence in high load conditions (see Figure 46).

Under−voltage Lockout (UVLO)

NCP6361 core does not operate for voltages below the Under Voltage lock Out (UVLO) level. Below UVLO threshold, all internal circuitry (both analog and digital) is held in reset. NCP6361 operation is not guaranteed down to VUVLO when battery voltage is dropping off. To avoid erratic on / off behavior, a maximum 100 mV hysteresis is implemented. Restart is guaranteed at 2.6 V when VBAT voltage is recovering or rising.

Power−Up / Power−Down Sequencing

The EN pin controls NCP6361 start up. EN pin Low to High transition starts the power up sequencer which is combined with a soft start consisting to limit the inrush current at 800 mA while the output voltage is establishing. If EN is made low, the DC to DC converter is turned off and device enters shutdown mode.

A built−in pull−down resistor disables the device when this pin is left unconnected or not driven.

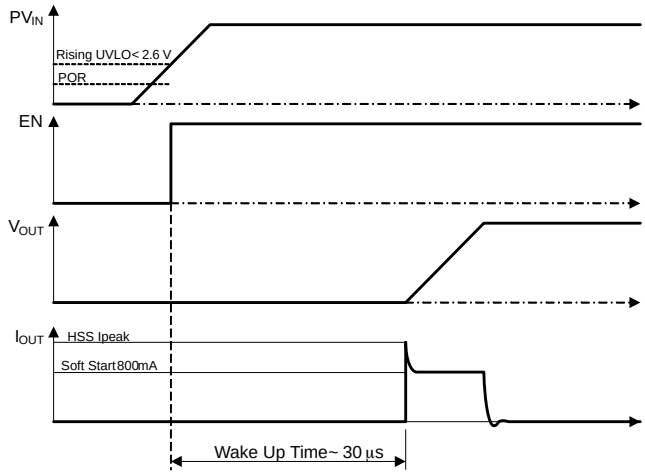


Figure 49. Power−Up Sequence

In order to power up the circuit, the input voltage PVIN has to rise above the UVLO threshold (Rising UVLO). This triggers the internal core circuitry power up which is the “Wake Up Time” (including “Bias Time”).

This delay is internal and cannot be bypassed.

The power down sequence is triggered by setting Low the EN pin. The output voltage goes down to 0 V.

Thermal Shutdown Feature (TSD)

The thermal capability of IC can be exceeded due to step down converter output stage power level. A thermal protection circuitry is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shut down, output voltage is turned off and the device enters sleep mode.

Thermal shut down threshold is set at 155°C (typical) when the die temperature increases and, in order to avoid erratic on / off behavior, a 30°C hysteresis is implemented. So, after a typical 155°C thermal shut down, the NCP6361 will return to normal operation when the die temperature cools to 120°C. This normal operation depends on the input conditions and configuration at the time the device recovers.

Spread Spectrum

The NCP6361A version operates at a constant frequency while the NCP6361B has a spread spectrum mode activated. The switching frequency is dithered around a center frequency of 3.429 MHz (FSEL = High) or of 6 MHz (FSEL = Low) depending on the FSEL position selected. Spread spectrum lowers noise at the regulated output and at the input.

The spread−spectrum modulation technique spreads the energy of switching frequency and harmonics over a wider band while reducing their peaks. This option can help to meet stringent EMI goals. The spread−spectrum feature implemented consists in adding spurs generated from a 24 MHz on−chip oscillator with the result of spreading the buck’s switching frequency. This option allows reducing the peak power at the switching frequency by about 10 dB and by the way reduces the noise level compared to a standard mode of operation.

The NCP6361B can definitely be used for EMI−sensitive applications.

APPLICATION INFORMATION

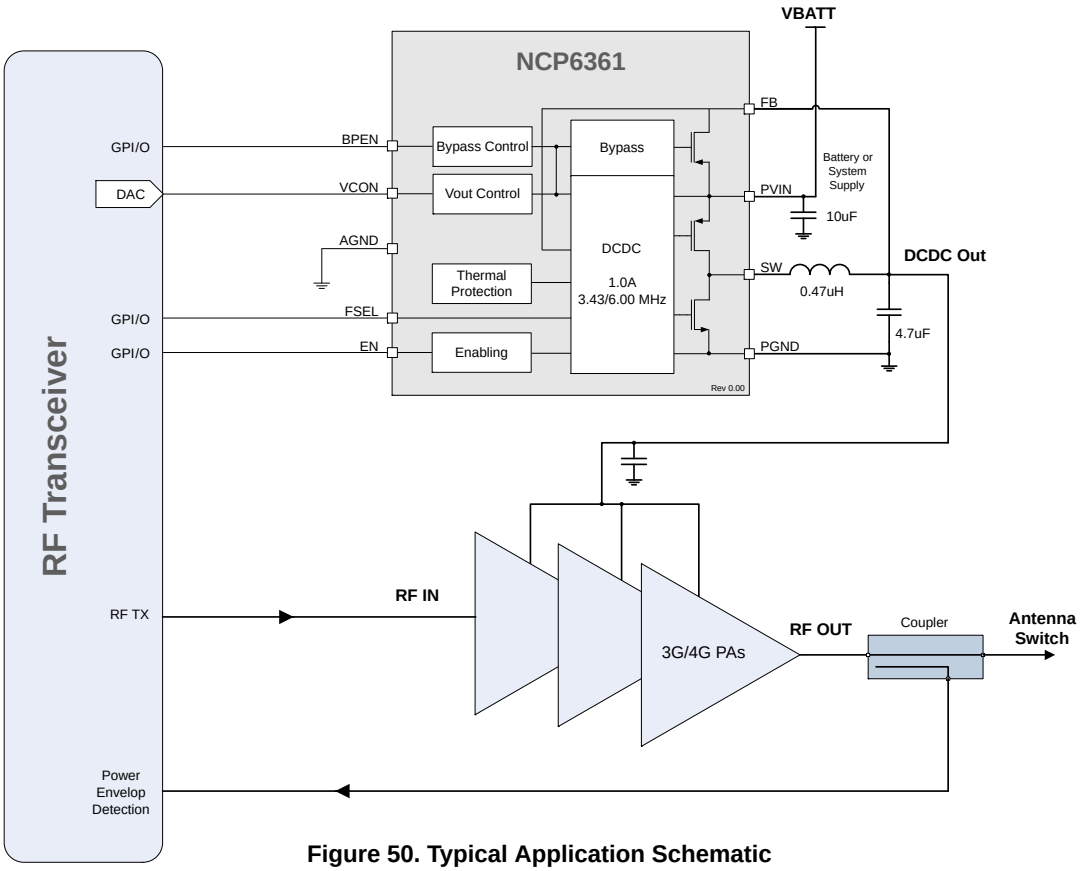


Figure 50. Typical Application Schematic

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of:

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \qquad \text{(eq. 1)}$$

The NCP6361 internal compensation network is optimized for a typical output filter comprising a 470 nH inductor and one 4.7 μF capacitor as described in the basic application schematic Figure 50.

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current I_{LPP} of approximately 20% to 50% of the maximum output current I_{OUTMAX} for a trade−off between transient response and output ripple. The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is:

$$I_{LMAX} = I_{OUTMAX} + \frac{I_{LPP}}{2} \qquad \text{(eq. 2)}$$

The inductor also needs to have high enough current rating in regards to temperature rise. Low DCR is good for efficiency improvement and temperature rise reduction. Tables 1 and 2 show recommended inductor references.

Table 1. RECOMMENDED INDUCTORS WHEN OPERATING AT 6 MHz

Supplier	Part#	Value (μH)	Size (L x l x T) (mm)	DC Rated Current (A)	DCR Max @ 25°C (mΩ)
TDK	TFM201610A−R47M−T00	0.47	20x16x1	3.5	46
TDK	TFM201210A−R47M−T00	0.47	20x12x1	2.5	65
Toko	DFE201610R−R47M−T00	0.47	20x16x1	3.8	48
Toko	DFE201610A−R47M−T00	0.47	20x16x1	3.7	58

Table 2. RECOMMENDED INDUCTORS WHEN OPERATING AT 3.43 MHz

Supplier	Part #	Value (μH)	Size (L x l x T) (mm)	DC Rated Current (A)	DCR Max @ 25°C (mΩ)
TDK	TFM201610A−1R0M−T00	1	20x16x1	2.9	75
Toko	DFE201610R−1R0M−T00	1	20x16x1	2.7	79

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be used. For a given peak−to−peak ripple current I_{LPP} in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as below.

$$V_{OUTPP} = V_{OUTPP(C)} + V_{OUTPP(ESR)} + V_{OUTPP(ESL)} \quad \text{(eq. 3)}$$

Where $V_{OUTPP(C)}$ is the ripple component coming from an equivalent total capacitance of the output capacitors, $V_{OUTPP(ESR)}$ is a ripple component from an equivalent ESR of the output capacitors, and $V_{OUTPP(ESL)}$ is a ripple component from an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUTPP(C)} = \frac{I_{L\_PP}}{8 \cdot C \cdot f_{SW}} \quad \text{(eq. 4)}$$

$$V_{OUTPP(ESR)} = I_{LPP} \cdot ESR \quad \text{(eq. 5)}$$

$$V_{OUT\_PP(ESL)} = \frac{ESL}{ESL + L} \cdot V_{IN} \quad \text{(eq. 6)}$$

And the peak−to−peak ripple current is:

$$I_{LPP} = \frac{\left(PV_{IN} - V_{OUT}\right) \cdot V_{OUT}}{PV_{IN} \cdot F_{SW} \cdot L} \quad \text{(eq. 7)}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUTPP}(C)$. So that the minimum output capacitance can be calculated regarding to a given output ripple requirement V_{OUTPP} in PWM operation mode.

$$C_{MIN} = \frac{I_{LPP}}{8 \cdot V_{OUTPP} \cdot f_{SW}} \quad \text{(eq. 8)}$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding the input ripple voltage V_{INPP} is

$$C_{INMIN} = \frac{I_{OUTMAX} \cdot \left(D - D^2\right)}{V_{INPP} \cdot f_{SW}} \quad \text{(eq. 9)}$$

Where

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 10)}$$

In addition the input capacitor needs to be able to absorb the input current, which has a RMS value of:

$$I_{INRMS} = I_{OUTMAX} \cdot \sqrt{D - D^2} \quad \text{(eq. 11)}$$

The input capacitor needs also to be sufficient to protect the device from over voltage spike and a minimum of 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC. PGND is connected to the ground terminal of the input cap which then connects to the ground plane. The PV_{IN} is connected to the V_{BAT} terminal of the input capacitor which then connects to the V_{BAT} plane.

Layout and PCB Design Recommendations

Good PCB layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Use two layers for the high current paths (PVIN, PGND, SW) in order to split current in two different paths and limit PCB copper self heating.

(See demo board example Figure 52)

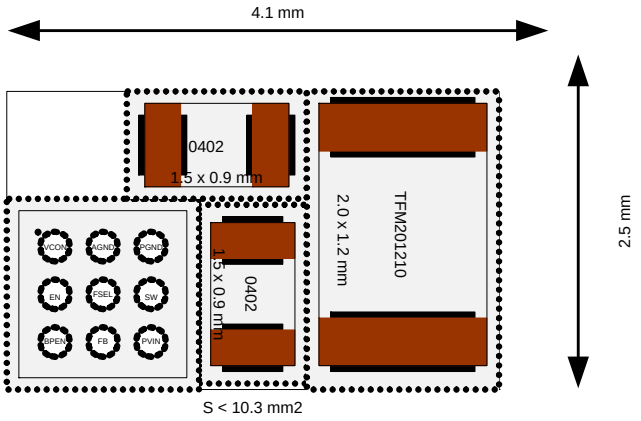


Figure 51. Layout Minimum Recommended Occupied Space Using 0402 Capacitors and 0805 (2.0 x1.2 x1 mm) Inductor

Input capacitor placed as close as possible to the IC.

- PV_{IN} directly connected to Cin input capacitor, and then connected to the Vin plane. Local mini planes used on the top layer (green) and layer just below top layer with laser vias.
- AGND directly connected to the GND plane.
- PGND directly connected to Cin input capacitor, and then connected to the GND plane: Local mini planes used on the top layer (green) and layer just below top layer with laser vias.
- SW connected to the Lout inductor with local mini planes used on the top layer (green) and layer just below top layer with laser vias.

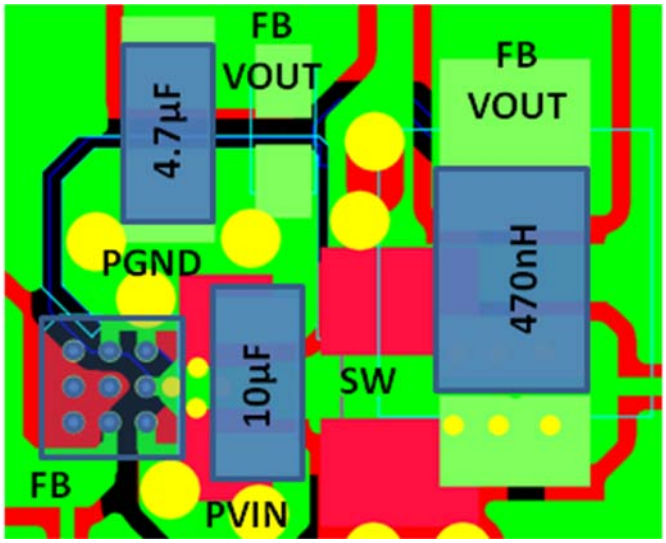


Figure 52. Example of PCB Implementation (PCB case with 0805 (2.0x1.2 mm) Capacitors and 2016 (2.0 x 1.6 x 1 mm) Inductors

ORDERING INFORMATION

Device	Spread−Sprectrum Option (F_{SW})	Package	Shipping†
NCP6361AFCCT1G	No	WLCSP9 (Pb−Free)	3000 / Tape & Reel
NCP6361BFCCT1G	Yes		

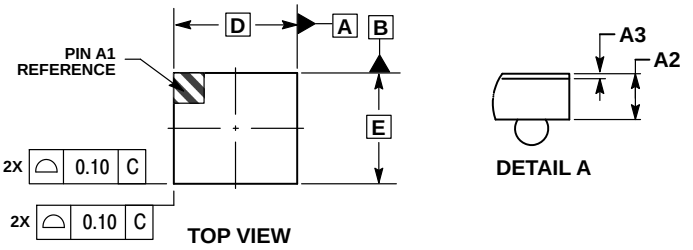
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Evaluation Boards:

NCP6361AGEVB and NCP6361BEVB evaluation boards are available under request. Contact Local Sales Representative or Sales Office.

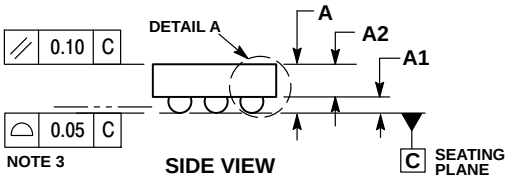
PACKAGE DIMENSIONS

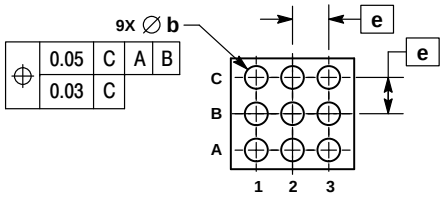
WLCSP9, 1.36x1.22
CASE 567GM
ISSUE A



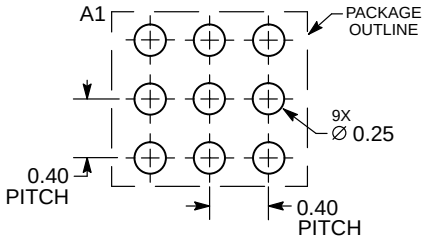
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.02	0.04
b	0.24	0.29
D	1.36 BSC	
E	1.22 BSC	
e	0.40 BSC	





RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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For additional information, please contact your local Sales Representative