PI6C4921506

High Performance LVDS Fanout Buffer

Features

- 6 LVDS outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Single differential input
- Low delay from input to output (Tpd typ. < 1.5ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-24 package

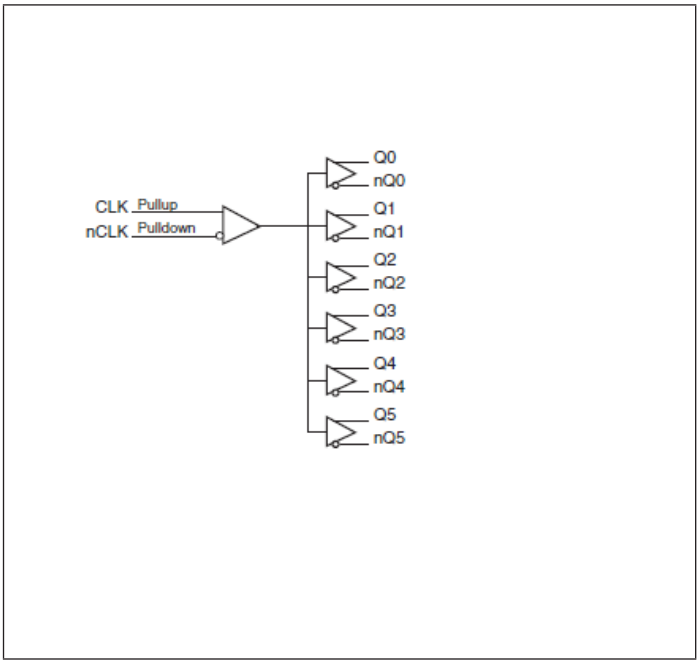
Description

The PI6C4921506 is a high performance fanout buffer device-which supports up to 1.5GHz frequency. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

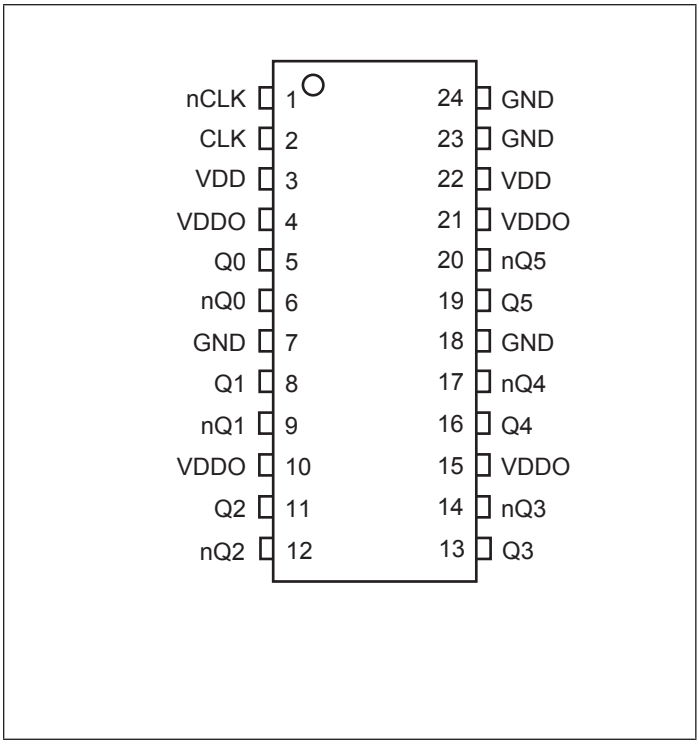
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (24-Pin TSSOP)



Pinout Table

Pin #	Pin Name	Type	Description
1, 2	nCLK CLK	Input	Differential clock input
3, 22	V_{DD}	Power	Power supply
4, 10, 15, 21	V_{DDO}	Power	IO power supply
5, 6	Q0 nQ0	Output	LVDS output clock
7, 18, 23, 24	GND	Power	Ground
8, 9	Q1 nQ1	Output	LVDS output clock
11, 12	Q2 nQ2	Output	LVDS output clock
13, 14	Q3 nQ3	Output	LVDS output clock
16, 17	Q4 nQ4	Output	LVDS output clock
19, 20	Q5 nQ5	Output	LVDS output clock

Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q5	nQ0:nQ5		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased	HIGH	LOW	Single Endded to Differential	Non Inverting
Biased	0	HIGH	LOW	Single Endded to Differential	Inverting
Biased	1	LOW	HIGH	Single Endded to Differential	Inverting

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Supply Voltage, V_{DD} 4.65V
Inputs, V_I ..... 0.5V to V_{DD} +0.5V
Outputs, I_O (LVDS)
Continuous Current 10mA
Surge Current 15mA
Package Thermal Impedence, Θ_{JA} ..... 70°C/W (0 mps)
Storage temperature, T_{STG} (Junction-to-Ambient)
..... -65 to +150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply DC Characteristics ($V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				70	mA
I_{DDO}	Output Supply Current				100	mA

Power Supply DC Characteristics ($V_{DD} = V_{DDO}$ = 2.5V±5%, T_A = -40°C TO 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				65	mA
I_{DDO}	Output Supply Current				102	mA

Differential DC Characteristics ($V_{DD} = V_{DDO}$ = 3.3V±5% or 2.5V±5%, T_A = -40°C TO 85°C)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	CLK	$V_{IN} = V_{DD}$			10	µA
		nCLK	$V_{IN} = V_{DD}$			150	µA
I_{IL}	Input Low Current	CLK	V_{IN} = 0V	-150			µA
		nCLK	V_{IN} = 0V	-10			µA
V_{PP}	Peak-to-Peak Input Voltage(1)			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage(1, 2)			GND+0.5		V_{DD}-0.85	V

Note:

1. VIL should not be less than -0.3V
2. Common mode voltage is defined as VH

LVDS DC Characteristics (V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage		326		526	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2		1.3	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Note:
Please refer to Parameter Measurement Information for output information.

LVDS DC Characteristics (V_{DD} = V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage		305		505	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15		1.3	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Note:
Please refer to Parameter Measurement Information for output information.

AC Characteristics (V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency				1.5	GHz
t_{PD}	Propagation Delay(1)		800		1100	ps
$t_{sk(o)}$	Output Skew(2, 3)				55	ps
t_{jit}	Buffer Additive Phase Jitter, RMS	622.08MHz, Integration Range: 12kHz – 20MHz		0.067		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤ 622MHz	47		53	%

Note:

Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

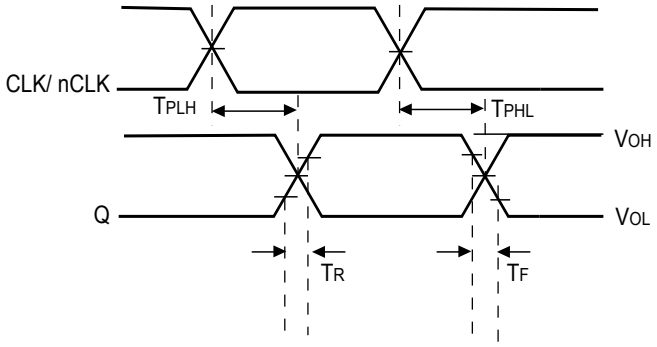
1. Measured from the differential input crossing point to the differential output crossing point.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from at the output differential cross points.
3. This parameter is defined in accordance with JEDEC Standard 65.

AC Characteristics ($V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency				1.5	GHz
t_{PD}	Propagation Delay(1)		800		1200	ps
$t_{sk(o)}$	Output Skew(2, 3)				55	ps
t_{jit}	Buffer Additive Phase Jitter, RMS	622.08MHz, Integration Range: 12kHz – 20MHz		0.067		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤ 622MHz	47		53	%

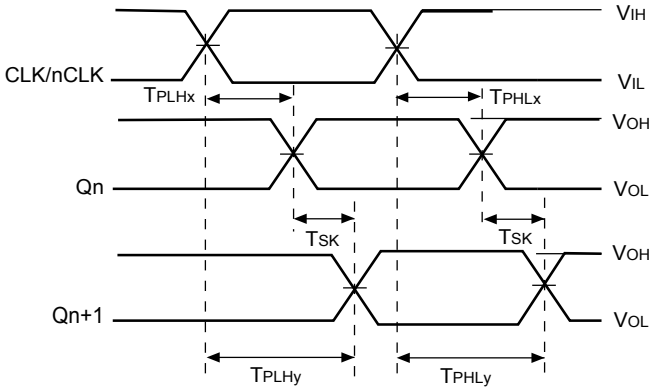
Propagation Delay

Propagation Delay T_{PD}



Output Skew

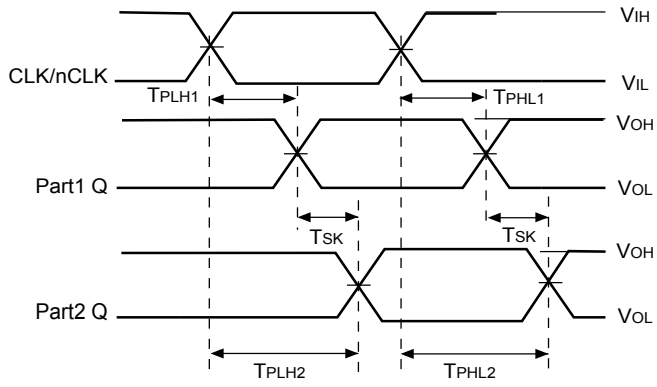
Output Skew T_{SK}



$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

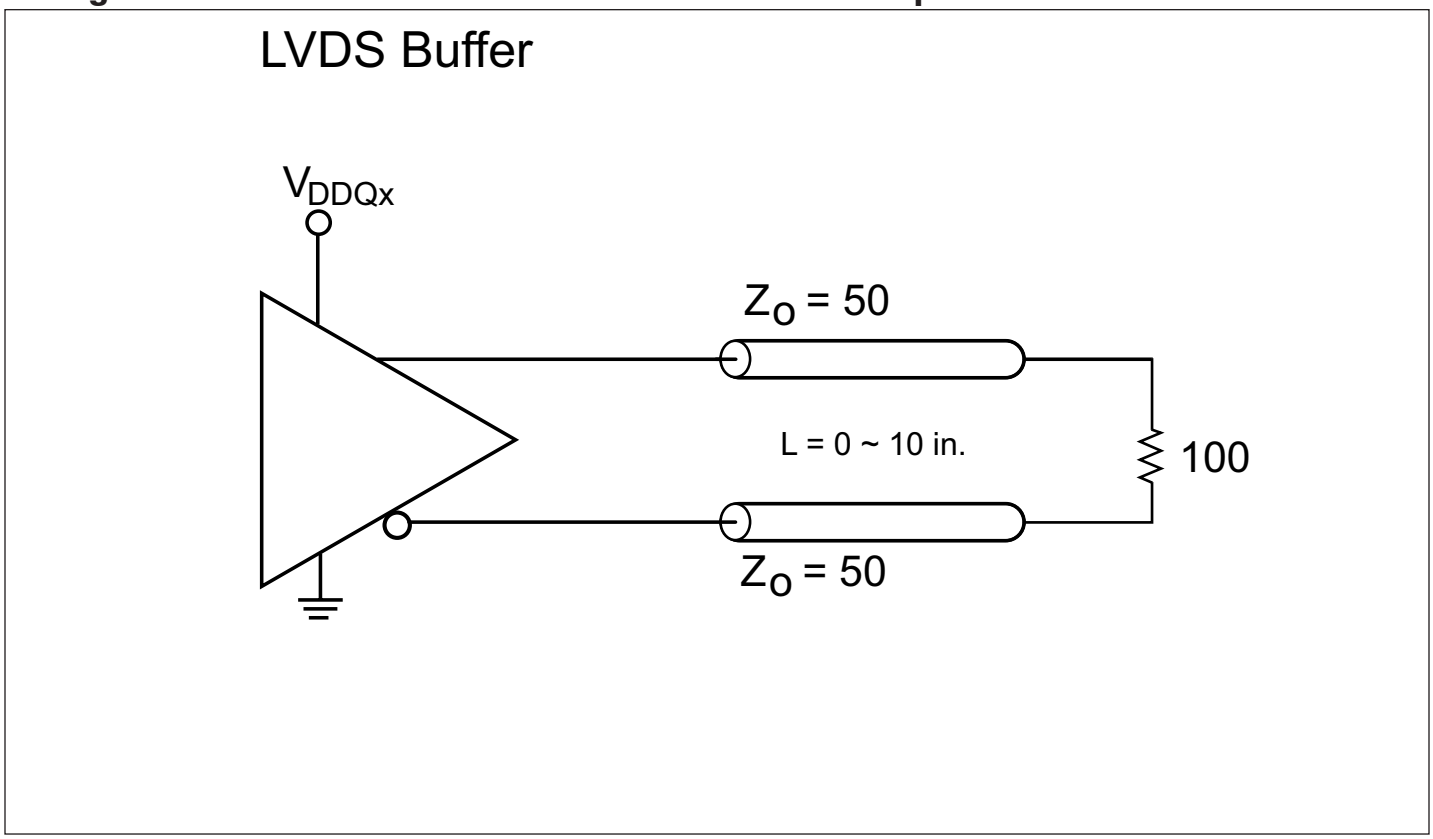
Part to Part Skew

Part-to-Part Skew

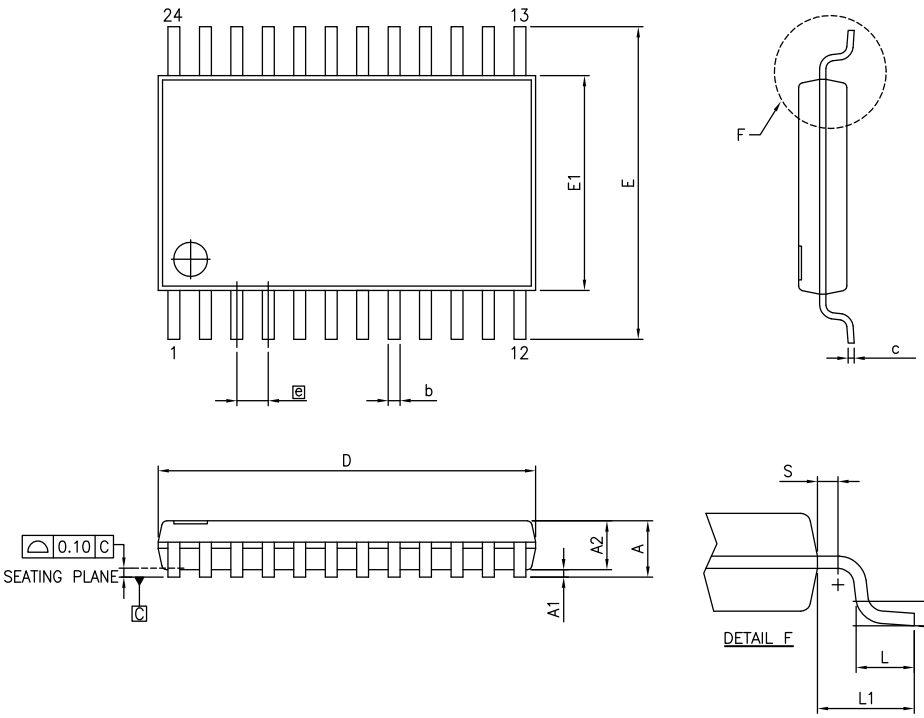


$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

Configuration Test Load Board Termination for LVDS outputs



Packaging Mechanical: 24-Contact TSSOP (L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC: MO-153F/AD
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 24-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1312 **REVISION: F**

12-0374 **Please check for the latest package information on the Pericom web site at www.pericom.com/packaging/**

Ordering Information

Ordering Number	Package Code	Package Description
PI6C4921506LIE	L	Pb-free & Green 24-Contact TSSOP
PI6C4921506LIEX	L	Pb-free & Green 24-Contact TSSOP, Tape & Reel

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**