

DATA SHEET

PTN3310/PTN3311

High-speed serial logic translators

Product data
Supersedes data of 2002 Oct 24

2004 Feb 24

High-speed serial logic translators

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FEATURES

- Meets LVDS EIA-644 and PECL standards
- 2 pin-for-pin replacement input/output choices:
 - LVDS in, PECL out (PTN3310)
 - PECL in, LVDS out (PTN3311)
- Single +3.3 V supply voltage operation
- Available in 8-pin SO or TSSOP package
- Maximum throughput data rate of 800 Mbps typical

APPLICATIONS

- High-speed networking and telecom applications
 - ATM
 - SONET/SDH
 - Switches
 - Routers
 - Add-drop multiplexers

GENERAL DESCRIPTION

The High-Speed Serial Logic Translator provides a point solution that addresses the various interface logic requirements of Optical Transceiver Modules. The product offers a compact translation between LVDS and PECL high speed serial data lines. This provides the end users a simple way to mix or match Optical Transceiver ICs from various vendors to maximize desired performance and reduces the need to redesign interfaces to accommodate new Optical Transceiver ICs.

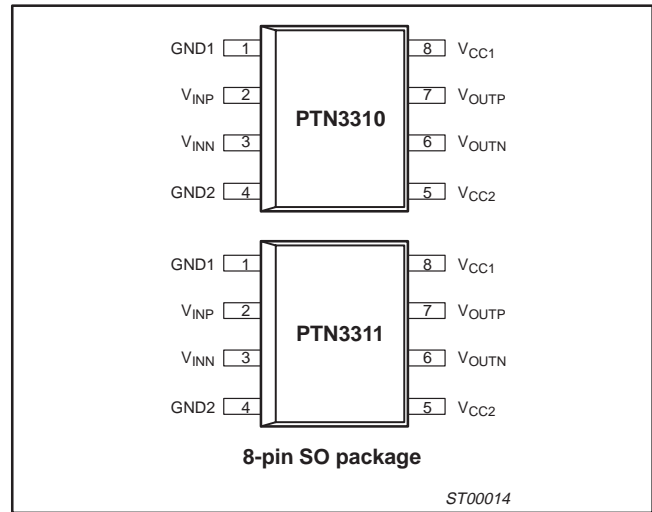
The High-Speed Serial Logic Translator comes in two translation choices to allow mixing LVDS and PECL input/outputs. The product is offered in a small, convenient, 8-pin package.

Figure 1 shows the High-Speed Serial Logic Translator Device in a typical high speed optical module application. Figure 2 shows the circuit block diagrams.

ORDERING INFORMATION

| Type number | Package | | |
|-------------|---------|---|----------|
| | Name | Description | Version |
| PTN3310D | SO8 | Plastic small-outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| PTN3311D | SO8 | Plastic small-outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| PTN3310DP | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |
| PTN3311DP | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |

PIN CONFIGURATIONS



PIN DESCRIPTIONS

8-pin SO and TSSOP package

| Pin # | Symbol | Name and function |
|-------|---------------------------------------|----------------------|
| 1, 4 | GND1, GND2 | Ground |
| 2, 3 | V _{INP} , V _{INN} | Differential inputs |
| 5, 8 | V _{CC1} , V _{CC2} | Supply voltage |
| 6, 7 | V _{OUTN} , V _{OUTP} | Differential outputs |

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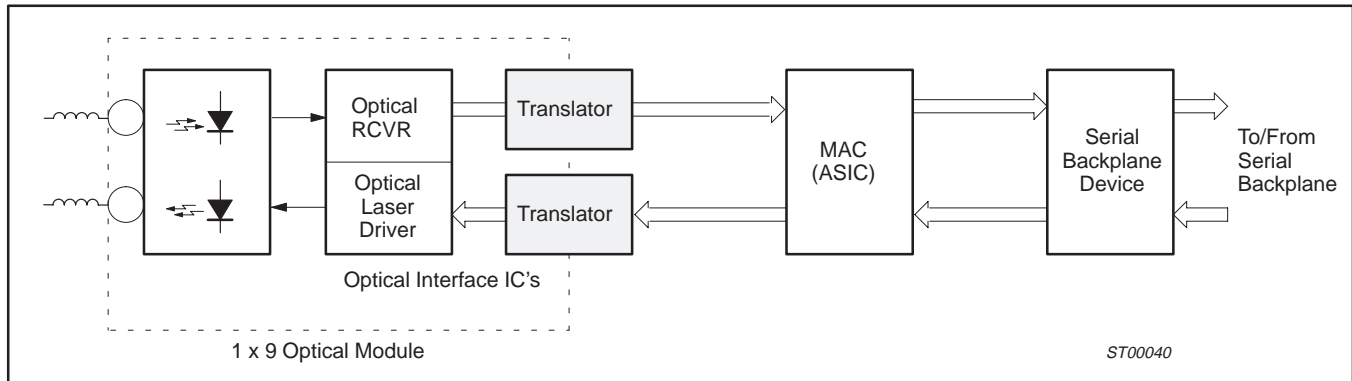


Figure 1. High-Speed Serial Logic Translators in Optical Module Application

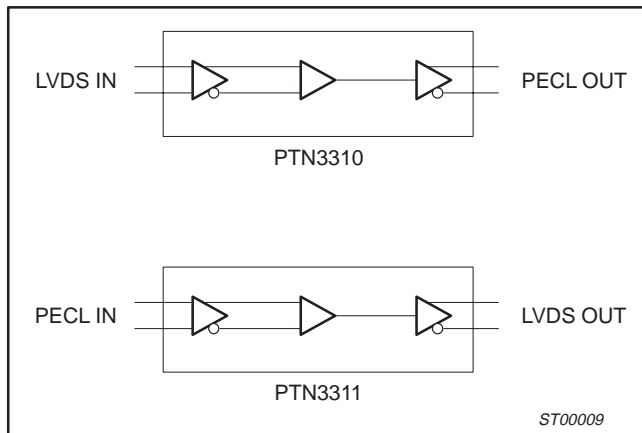


Figure 2. High-Speed Serial Logic Translator Block Diagrams

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Limits | Unit |
|--------------------|--|--------------|------|
| V _{CC} | Supply voltage | -0.3 to +4.0 | V |
| V _I | LVDS receiver input voltage | -0.3 to +5.5 | V |
| V _O | LVDS driver output voltage | -0.3 to +5.5 | V |
| t _{SC} | LVDS output short circuit duration | continuous | |
| T _j | Maximum junction temperature | +150 | °C |
| T _{stg} | Storage temperature range | -65 to +150 | °C |
| ESD _{HBM} | Electrostatic discharge (Human Body Model, 1.5 kΩ, 100 pF) | >2 | kV |
| ESD _{MM} | Electrostatic discharge (Machine Model, 0 kΩ, 200 pF) | >200 | V |

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------|---|-----|-----|------------------|
| V _{CC} | Supply voltage | 3.0 | 3.6 | V |
| T _{amb} | Operating ambient temperature range in free air | -40 | +85 | °C |
| V _{CCN} | Power supply noise voltage | - | 100 | mV _{PP} |

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|--------------------------|-------|-------|-------|------|
| General | | | | | | |
| V_{CC} | Supply voltage | | 3.0 | 3.3 | 3.6 | V |
| I_{CC} | Power supply current | PTN3311 | – | 12 | 20 | mA |
| I_{EE} | Power supply current | PTN3310 | – | 13 | 20 | mA |
| PECL inputs (PTN3311) | | | | | | |
| V_{IH} | Input HIGH voltage ¹ | | 2.135 | – | 2.420 | V |
| V_{IL} | Input LOW voltage ¹ | | 1.490 | – | 1.825 | V |
| I_I | Input current | $V_{IN} = V_{CC}$ or GND | – | – | ±10 | μA |
| LVDS inputs (PTN3310) | | | | | | |
| V_{ID} | Minimum differential input signal amplitude | | 100 | – | – | mV |
| I_{IN} | Input current ² | $V_{IN} = 0$ V | – | – | 20 | μA |
| | | $V_{IN} = V_{CC}$ | – | – | 20 | μA |
| PECL outputs (PTN3310) | | | | | | |
| V_{OH} | Output HIGH voltage ¹ | | 2.275 | 2.345 | 2.420 | V |
| V_{OL} | Output LOW voltage ¹ | | 1.490 | 1.595 | 1.680 | V |
| C_L | Output load capacitance | | – | 5 | – | pF |
| LVDS outputs (PTN3311); $R_L = 100 \Omega$ | | | | | | |
| V_{OD} | Output differential voltage | | 250 | 350 | 450 | mV |
| ΔV_{OD} | Steady-state difference in output differential voltage between complementary output states | | – | – | 50 | mV |
| V_{OS} | Offset voltage | | 1.125 | 1.250 | 1.375 | V |
| ΔV_{OS} | Steady-state difference in offset voltage between complementary output states | | – | – | 50 | mV |
| I_{OS} | Output short-circuit current | outputs mutually shorted | – | – | 12 | mA |
| | | output shorted to GND | – | – | 24 | mA |
| C_L | Output load capacitance | | – | 5 | – | pF |

NOTES:

1. These values are for $V_{CC} = 3.3$ V; PECL level specifications are referenced to V_{CC} and will track 1:1 with variation of V_{CC} .
2. Power supply either on or off.

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AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|-----|-----|-----|------|
| General | | | | | | |
| f _{MAX} | Maximum throughput data rate | | 655 | 800 | – | Mbps |
| t _{SKEW} | Clock output skew, part-to-part | | – | 100 | – | ps |
| | Clock output pulse skew | | – | 50 | – | ps |
| t _{PLH} /t _{PHL} | Propagation delay input (differential) to output | | – | 1 | 3 | ns |
| | Propagation delay input (single-ended) to output | | – | 1 | 3 | ns |
| PECL outputs (PTN3310) | | | | | | |
| t _r /t _f | Output rise and fall times at 20% and 80% intersects | | – | 200 | 300 | ps |
| LVDS outputs (PTN3311); R_L = 100 Ω; C_L = 5 pF | | | | | | |
| t _{TLH} | Transition time LOW to HIGH | R _L = 100 Ω; C _L = 5 pF | – | 500 | 650 | ps |
| t _{THL} | Transition time HIGH to LOW | R _L = 100 Ω; C _L = 5 pF | – | 500 | 650 | ps |
| V _{OSS} | Peak-to-peak switching offset voltage | Measured between two matched 49.9 Ω load resistors; 5 pF load capacitance | – | – | 150 | mV |

LVDS REFERENCE MEASUREMENT CONFIGURATION

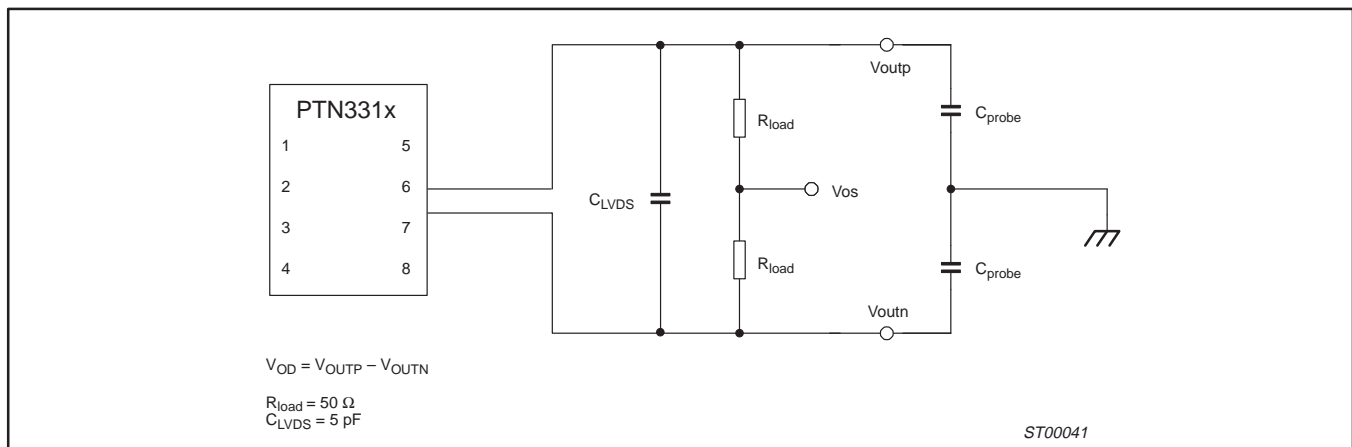


Figure 3.

The above diagram shows the test set-up used when evaluating LVDS outputs. According to the TIA-EIA-644 Standard, the maximum lumped capacitance test load should be 5 pF. However, by using probes or cables to observe the signal, additional capacitance is added, which has an effect on the rise and fall times. C_{probe} represents any capacitance caused by the use of probes or cables. Assuming balanced loading and balanced output drivers, the total effective capacitance seen by the part is:

$$C_{\text{Eff}} = C_{\text{LVDS}} + \frac{1}{2} C_{\text{probe}}$$

To correctly account for the effects of C_{probe}, the following formula should be used:

$$\Delta t = \frac{5 \text{ pF}}{C_{\text{Eff}}} \Delta t_{\text{measured}}$$

Where Δt is the 20%–80% rise/fall time.

To avoid the use of additional calculation of the measured results, a different approach could be taken; however, the value of C_{probe} has to be known in advance. In that case, the value of C_{LVDS} can be chosen such that the sum of the capacitances equals 5 pF, i.e.:

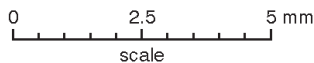
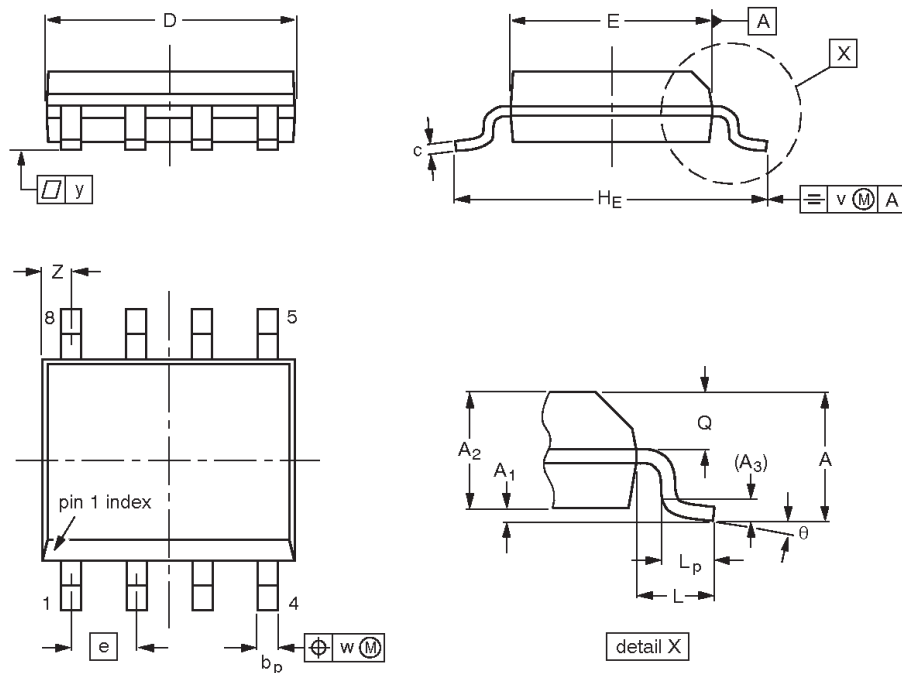
$$C_{\text{LVDS}} + \frac{1}{2} C_{\text{probe}} = 5 \text{ pF}$$

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SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 5.0 4.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.20 0.19 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

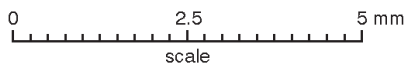
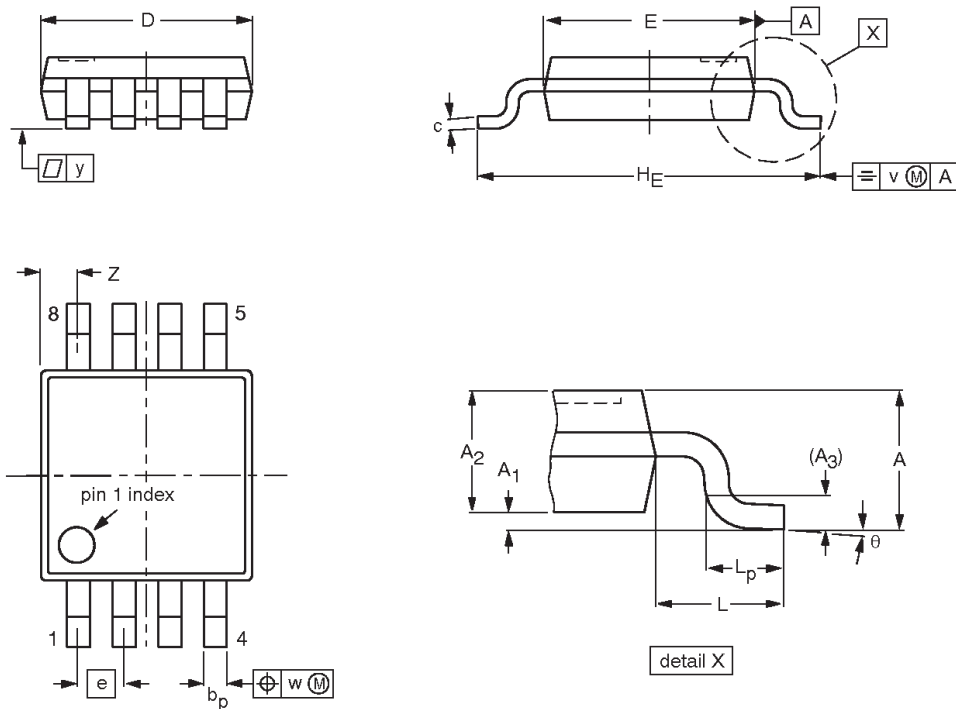
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | 99-12-27 03-02-18 |

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TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|-----|-----|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.45 0.25 | 0.28 0.15 | 3.1 2.9 | 3.1 2.9 | 0.65 | 5.1 4.7 | 0.94 | 0.7 0.4 | 0.1 | 0.1 | 0.1 | 0.70 0.35 | 6° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|---------------------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | 99-04-09 03-02-18 |

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REVISION HISTORY

| Rev | Date | Description |
|-----|----------|--|
| _3 | 20040224 | Product data (9397 750 12943). Supersedes data of 2002 Oct 24 (9397 750 10628). Modifications: <ul style="list-style-type: none">• Corrected package outline version from SOT505-2 to SOT505-1 in Ordering information table and Package outline sections. |
| _2 | 20021024 | Product data (9397 750 10628). ECN 853-2362 28701 dated 06 August 2002. Supersedes data of 2001 Jun 19 (9397 750 08511). |
| _1 | 20010619 | Product data (9397 750 08511). |

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sales.addresses@www.semiconductors.philips.com

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