SC2677B
Dual Synchronous Voltage Mode Controller with Current Sharing Circuitry

POWER MANAGEMENT

Description

The SC2677B is a versatile 2 phase, synchronous, voltage mode PWM controller that can be used in two distinct ways. First, the SC2677B is ideal for applications where point of use output power exceeds any single input power budget. Alternatively, the SC2677B can be configured as a dual switcher. The SC2677B features a precise temperature compensated voltage reference, cycle-by-cycle peak current limit, under voltage lockout over current protection, and internal level-shifted high-side gate drive circuitry.

In current sharing configuration, the SC2677B can produce a single output voltage from two separate input voltage sources (which can be different in voltage levels) while maintaining current sharing between the two channels. Current sharing is programmable to allow each input supply to be loaded differently per application requirements.

In dual switcher configuration, two feedback paths are provided for independent control of the separate outputs. The device will provide a regulated output from flexibly configured inputs, such as 3.3V, 5V, 12V etc. The phasing between the two switchers is adjustable to minimize the input and output ripple.

Features

- 300kHz to 1MHz externally programmable frequency operation
- Soft Start and Enable function
- Power Good output provided
- Cycle-by-cycle peak current limit
- Latch off for over current protection
- Phase-shifted switchers minimize ripple
- High efficiency operation, >90%
- Programmable output(s) as low as 0.5V
- Industrial temperature range
- TSSOP-24 package
- TSSOP-24 EDP package
- Bias voltage as low as 4.5V
- Adjustable phase shift between channels

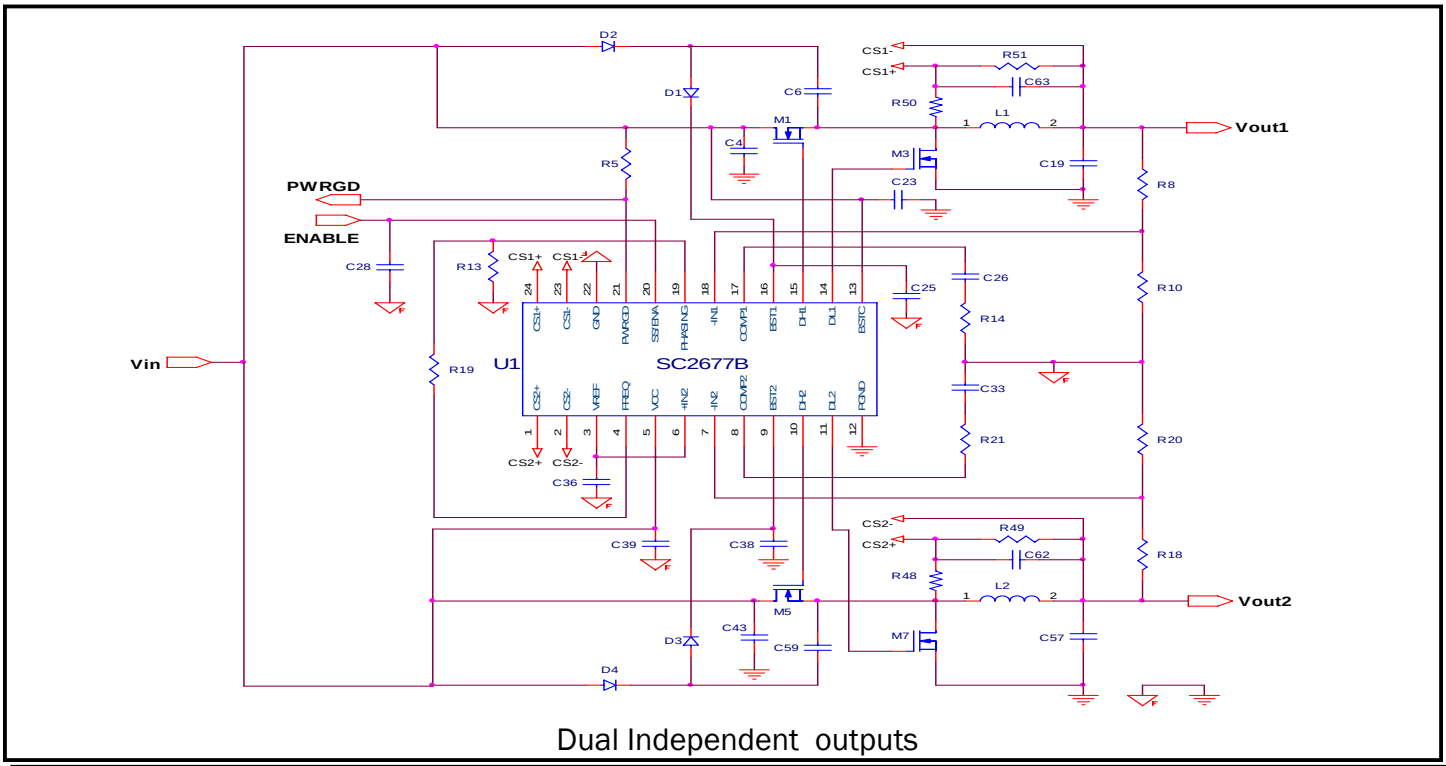
Two Phase, Current Sharing Controller

- Flexible, same or separate V_{IN}
- Programmable current sharing
- Thermal distribution via multi-phase output

Applications

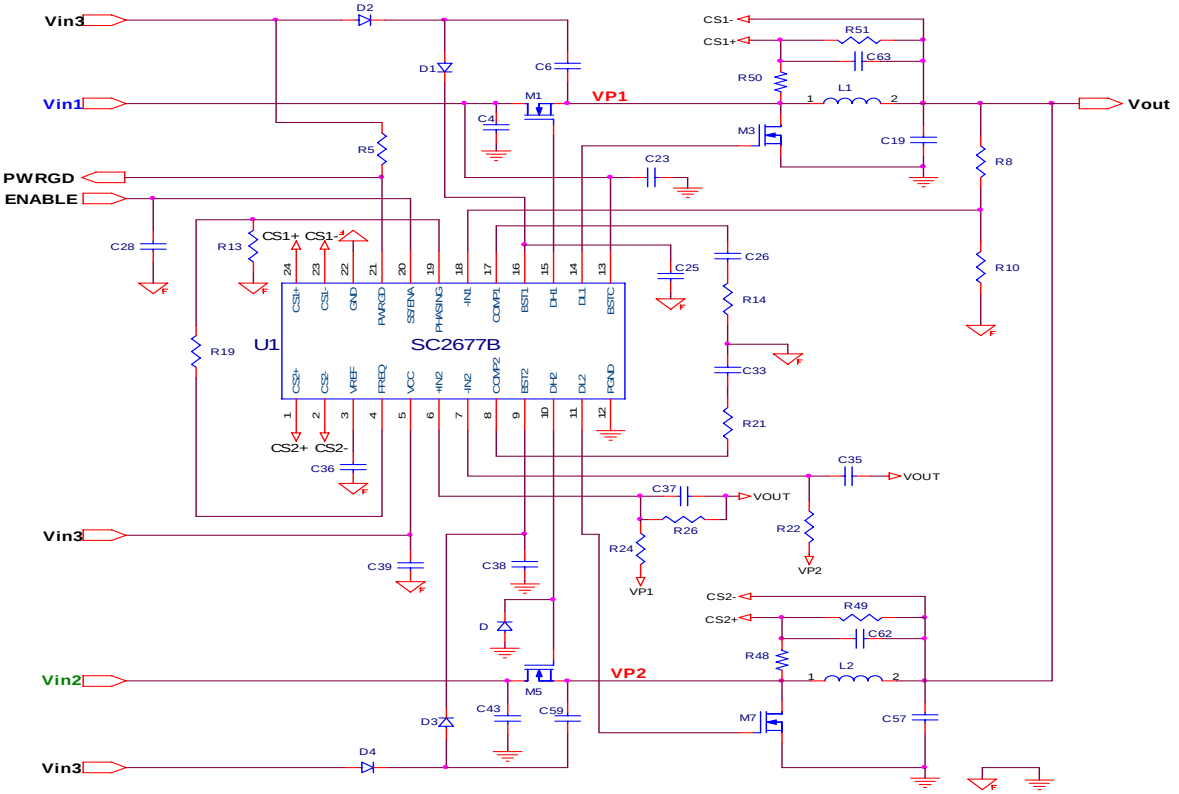
- Graphics cards
- Peripheral add-in card
- Dual-Phase power supply
- Power supplies requiring two outputs

Typical Application Schematic

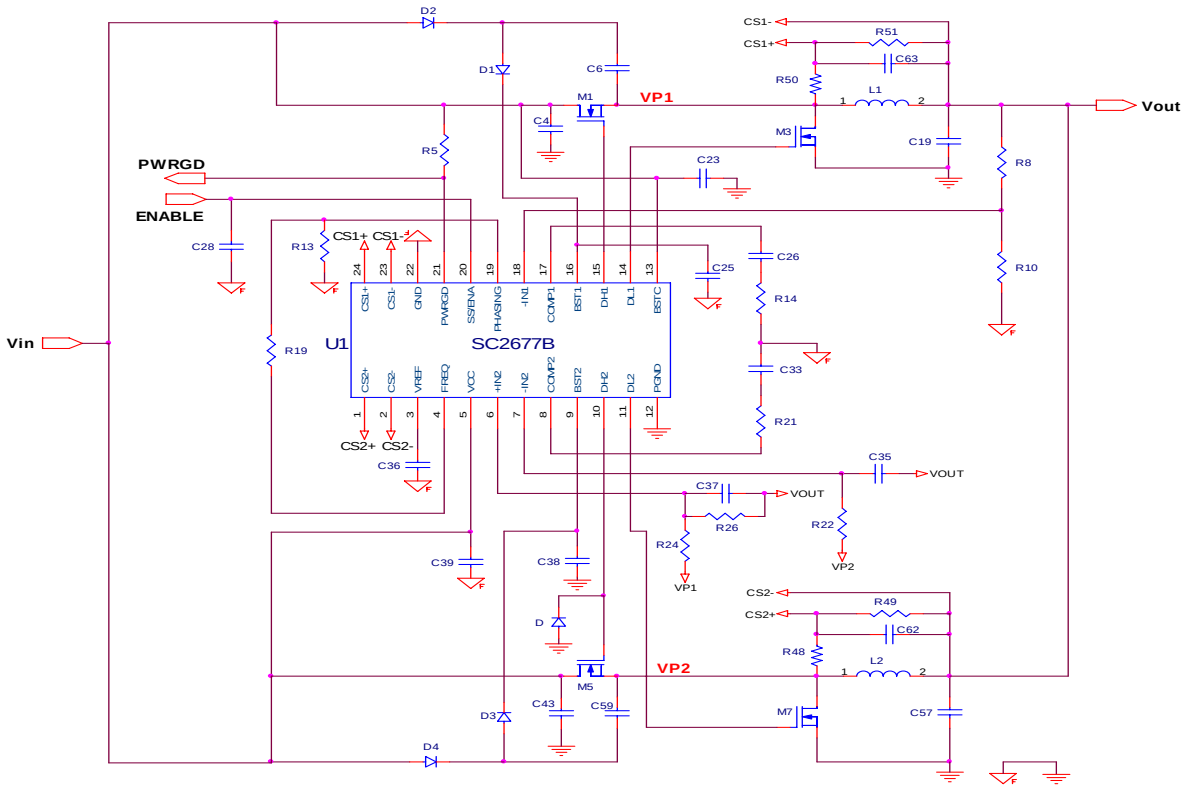


Dual Independent outputs

Typical Application Schematic



Dual Input, Single output, Current share Mode



Single Input/output, Current share Mode

Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Limits	Units
V_{CC} to GND	V_{IN}	-0.3 to 15	V
PGND to GND		± 1	V
BST1, BST2 to GND		-0.3 to 30	V
BSTC to GND		-0.3 to 20	V
-IN1, +/-IN2 to GND		7	V
COMP1, COMP2 to GND		7	V
DH1, DH2 to GND(6)		-0.3 to 30	V
DL1, DL2 to GND		-0.3 to BSTC + 0.3	V
		-3 peak (50nS) (1)	V
CS1+, CS1-, CS2+, CS2-		7	V
PWRGD to GND		V_{CC} + 0.3	V
PHASING		7	V
SS/ENA to GND		-0.3 to 7	V
Thermal Resistance Junction to Case TSSOP-24 TSSOP-24 EDP	θ_{JC}	 17 5.5	°C/W
Thermal Resistance Junction to Ambient TSSOP-24 TSSOP-24 EDP	θ_{JA}	 90 32	°C/W
Operating Ambient Temperature Range	T_A	-40 to 85	°C
Operating Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, T_J = 25°C, V_{BSTC} = V_{BST} = 12V

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	V_{OUT} = V_{FB}	0.495	0.500	0.505	V
	V_{OUT} = V_{FB}, -40 to 125 °C	0.492	0.500	0.508	V
Supply Voltage	V_{CC}	4.5		15	V
Supply Current	V_{CC} = 5.0		10		mA
UVLO	V_{CC} Ramp up Threshold		2.84		V
UVLO Hysteresis	V_{CC}		100		mV
Reference			0.5		V
Reference Load Regulation	V_{REF} source 10uA ~ 100uA			0.2	%
Reference Line Regulation	5V < V_{CC} < 15V			0.7	%
Output Line Regulation	5V < V_{IN} < 15V			0.7	%
Gain (Gm) (Error Amplifier)	COMP pin source 100uA	4	5	6.5	mA/V
Input Offset Voltage (Slave Error Amplifier)		-3	-1	0	mV
Max Current (Error Amplifier)	Source, Sink	400	460		µA
Input Bias Current	-IN1, +IN2, -IN2			2	µA

Electrical Characteristics (Cont.)

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, T_J = 25°C, V_{BSTC} = V_{BST} = 12V

Parameter	Conditions	Min	Typ	Max	Units
Under Voltage Latching off Threshold		60	70	80	%
Oscillator Frequency Range		300		1000	kHz
Oscillator Frequency	R_{SET} = 5kohm	450	500	550	kHz
Oscillator Max Duty Cycle	F_{OSC} = 500kHz	86	90		%
Phasing of DH2 and DH1	$V_{PHASING}$ = 0.585V		180		°
DH Sink Current	DH - PGND = 3.5V	1.7			A
DH Sink Current	DH - PGND = 2.5V	0.85			A
DH Source Current	BSTH - DH = 3.75V	1.7			A
DH Source Current	BSTH - DH = 3V	0.85			A
DL Sink Current	DL - PGNG = 3.5V	1.7			A
DL Sink Current	DL - PGND = 2.5V	0.85			A
DL Source Current	BSTL - DL = 3.75V	1.7			A
DL Source Current	BSTL - DL = 3V	0.85			A
DH Minimum on Time	-40 to 0 °C		300		ns
Dead Time	Note 5	50	85	120	ns
Soft Start Charge Current (2)			50		µA
Soft Start Enable	0% duty cycle		400		mV
Soft Start End	100% duty cycle		825		mV
Soft Start Transition Threshold(2)	Synchronous mode		1.22		V
OCP Trip Threshold		28	33	37	mV
OCP Delay Time	From OCP detection to DH low			200	nS
Input Offset (Current Sense Amplifier)			+/-3		mV
Input Bias Current	CS1+, CS1-, CS2+, CS2-			100	nA
Power Good Threshold	V_{OUT} ramping up	83%	88%	93%	V_{OUT}
Power Good Pull Down	Sink Current = 2mA			0.4	V

Notes:

(1) Measured from 50% to 50% pulse amplitude.

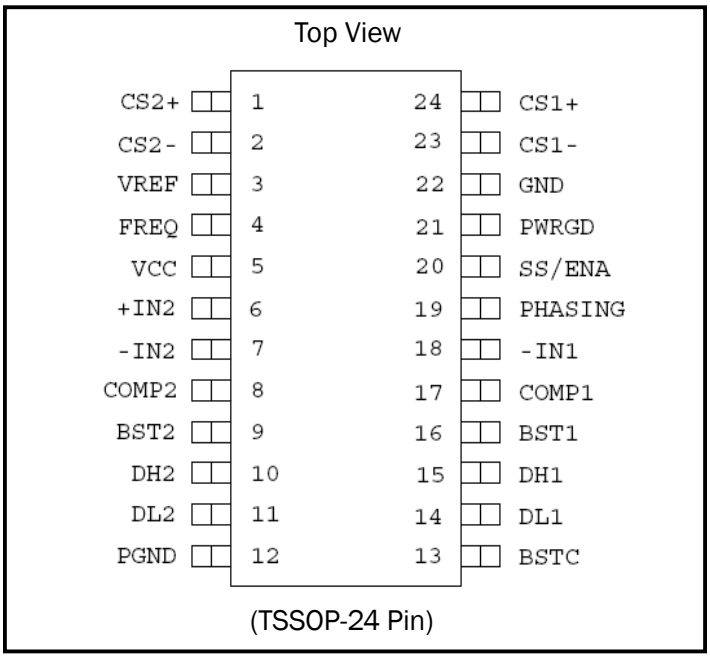
(2) The soft start pin sources 50µA to an external capacitor. The converter operates in synchronous mode above the soft start transition threshold and in asynchronous mode below it.

(4) This device is ESD sensitive. Use of standard ESD handling precautions is required.

(5) 120ns maximum at 70°C.

(6) Under pulsing condition, the negative voltage can be -5V for no more than 40ns measured from 50% falling to 50% rising.

Pin Configuration



(TSSOP-24 Pin)

Ordering Information

Device[1]	Package
SC2677BITSTRT[2]	TSSOP-24
SC2677BTETRT[2]	TSSOP-24 EDP
SC2677BEVB-1	Current Share Evaluation Board
SC2677BEVB-2	Dual Channel Evaluation Board

Notes:

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) Lead free package. Device is fully WEEE and RoHS compliant.

Pin Descriptions

EXPANDED PIN DESCRIPTION

Pin 1, 24: (CS2+, CS1+)
Current sense amplifier (for OCP protection) non-inverting inputs.

Pin 2, 23: (CS2-, CS1-)
Current sense amplifier (for OCP protection) inverting inputs.

Pin 3: (VREF)
Internal 0.5V reference. Connected to the + input of the master channel error amplifier.

Pin 4: (FREQ)
External frequency adjustment. Connect a resistor to AGND to set the switching frequency. Please see more information in Application section.

Pin 5: (VCC)
Bias pin for the controller. Connect a ceramic decoupling capacitor from this pin to AGND with minimum trace length.

Pin 6: (+IN2)
"+" input of the slave error amplifier.

Pin 7, 18: (-IN2, -IN1)
"-" inputs of the error amplifiers.

Pin 8, 17: (COMP2, COMP1)
Compensation pins of the error amplifiers.

Pin 9, 16: (BST2, BST1)
Supply pins for the high side drivers. Usually connected to bootstrap circuit.

Pin 10, 15: (DH2, DH1)
Gate drive pins for the top MOSFETs. Requires a small series resistor.

Pin 11, 14: (DL2, DL1)
Gate drive pins for the bottom MOSFETs. Requires a small series resistor.

Pin 12: (PGND)
Power GND. Return of the high side and low side gate drivers.

Pin 13: (BSTC)
Supply pin for bottom MOSFET gate drivers.

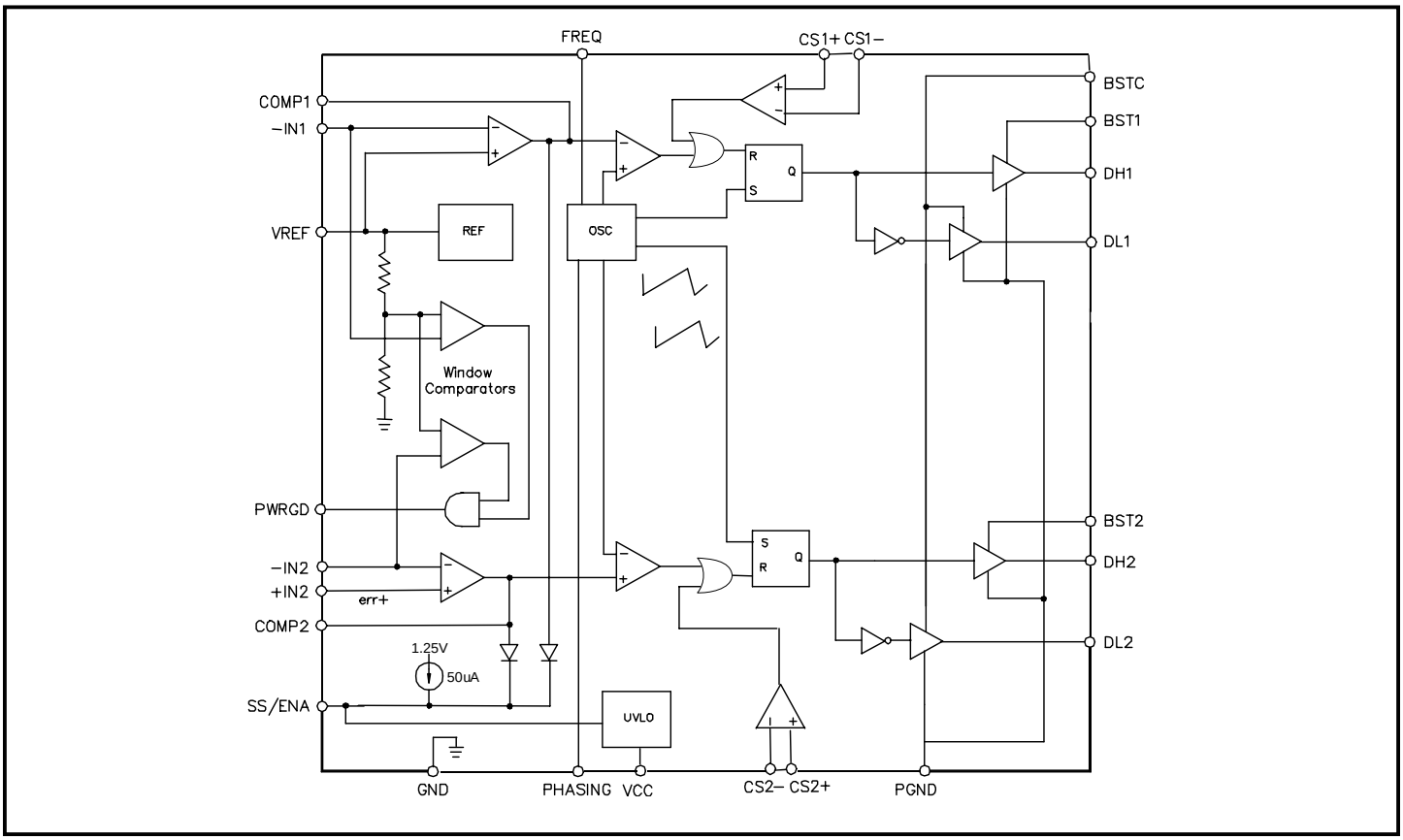
Pin 19: (PHASING)
This pin controls the phase shift between master and slave for optimum noise immunity. Use a resistive divider from the FREQ pin (pin 2) to AGND, and connect the tap of the resistive divider to pin 17. Please see more information in Application section.

Pin 20: (SS/ENA)
Soft start pin. Connect a ceramic capacitor from this pin to AGND, and there is an internal current source charging up this capacitor during soft start. The PWM operation can be disabled if this pin is pulled low.

Pin 21: (PWRGD)
Power good signal. This is an open collector output. It is pulled low internally if output voltage is outside the power good window.

Pin 22: (GND)
Analog GND. Return of the analog signals and bias of the chip.

Block Diagram



Notes:

(1) Channel 1 is the Master and Channel 2 is the Slave in current sharing configuration.

(2) For dual output operation, tie +IN2 to VREF and the two PWM channels are independent.

Main Loop(s)

The SC2677B is a dual, voltage mode synchronous Buck controller. The two separate channels are identical and share only IC supply pins (Vcc and GND), output driver ground (PGND) and pre-driver supply voltage (BSTC). They also share a common oscillator generating a sawtooth waveform for channel 1 and an dephased sawtooth for channel 2. Channel 2 has both inputs of the error amplifier uncommitted and available externally. This allows the SC2677B to operate in two distinct modes.

a) Two independent channels with either common or different input voltages and different output voltages. The two channels each have their own voltage feedback path from their own output. In this mode, positive input of the error amplifier 2 is connected externally to Vref. If the application uses a common input voltage, the sawtooth phase shift between the channels provides some measure of input ripple current cancellation.

b) Two channels operating in current sharing mode with common output voltage and either common input voltage or different input voltages. In this mode, channel 1 operates as a voltage mode Buck controller, as before, but error amplifier 2 monitors and amplifies the difference in voltage across the output current sense resistors of channel 1 and channel 2 (Master and Slave) and adjusts the Slave duty cycle to match output currents. To controller also works well for using the output choke winding resistance as current sensing element (please refer the application schematic for details). The amount of the current of the slave channel vs the master channel can be programmed according to the application. This feature is especially useful when two input sources are used and each source has its power budget.

The offset of the current sharing error amplifier is trimmed whthin the range of -2mV to 0mV. The polarity being such that the slave is OFF if the master has no current.

Power Good

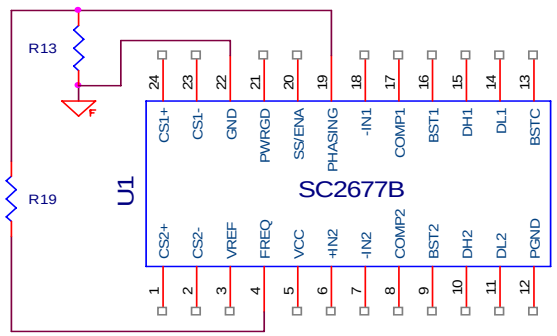
The controller provides a power good signal. This is an open collector output, which is pulled low if the output voltage is outside of the power good window.

Soft Start/Enable

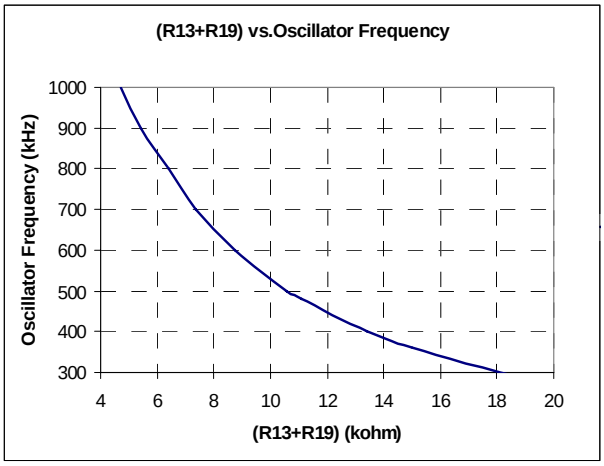
The Soft Start/Enable (SS/ENA) pin serves several functions. If held below the Enable threshold, both channels are inhibited. DH1 and DH2 will be low, turning off the top FETs. Between the Soft Start Enable threshold and the Soft Start End threshold, the duty cycle is allowed to increase. At the Soft Start End threshold, maximum duty cycle is reached. In practical applications the error amplifier will be controlling the duty cycle before the Soft Start End threshold is reached. To avoid boost problems during start-up in current share mode, both channels start up in asynchronous mode, and the bottom FET body diode is used for circulating current during the top FET off time. When the SS/ENA pin reaches the Soft Start Transition threshold, the channels begin operating in synchronous mode for improved efficiency. The soft start pin sources approximately 50uA and soft start timing can be set by selection of an appropriate soft start capacitor value.

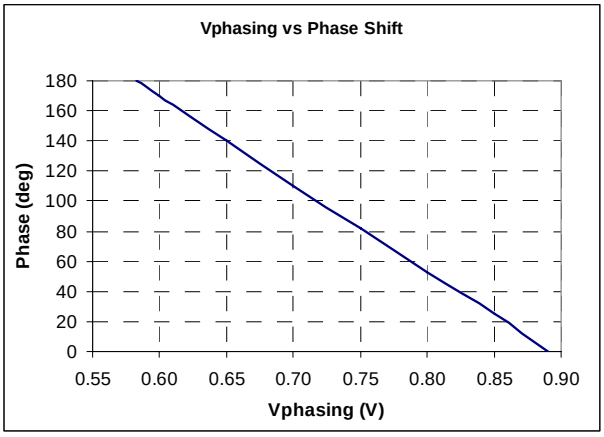
Frequency Set and Phasing

The switching frequency can be programmed by connecting a resistor from the FREQ pin to AGND. The PHASING pin controls the phase shift between the master sawtooth and slave sawtooth which allows the adjustment of the phase shift for maximum noise immunity by controlling the timing between master and slave transition. A resistive divider is used from the FREQ pin to AGND and the divided voltage is fed to the PHASING pin as depicted.



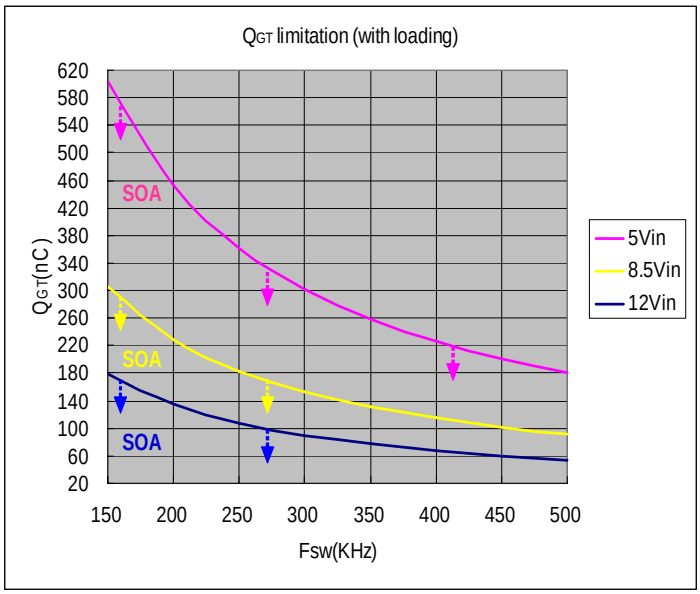
Application Information(Cont.)





I_{CC} : Supply current for controller.
Q_{GT} : Total gate charge of all selected MOSFETs.
Q_G : Total gate charge of per selected MOSFETs.
F_{SW} : Switching frequency.
N : Number of MOSFET.

It's recommended that the below figure be performed to ensure SC2677B under safe operation area.



Over Current Protection

Current sense amplifiers sense the inductor DCR, and compare with an internal OCP reference. As over current being detected, the current sense amplifier will trip the peak current limit on cycle-by-cycle basis. If the over current condition sustains, and the output voltage drops below 75% of its nominal voltage level, the PWM will be disabled and the power supply be latched off with short amount of delay. The latch can be reset by power cycling.

Controller Power Dissipation

Controller power dissipation is generated by following parameter; switching frequency, total gate charge of all selected MOSFETs and supply voltage.

$$P = Vin * (I_{CC} + Q_{GT} * F_{SW})$$
$$Q_{GT} = Q_G * N$$

Where

Vin : Supply voltage for controller and driving MOSFET.

An example is shown below to demonstrate the procedure introduced above.

Vin =12V
Fsw =250KHz
N =4(number of MOSFET)

Then

Q_{GT} = 108nC
Q_G = 27nC (per MOSFET)

Layout Guidelines

Power and signal traces must be kept separated for noise considerations. Feedback, current sense traces and analog ground should not cross any traces or planes carrying high switching currents, such as in the input loop or the phase node.

The input loop, consisting of the input capacitors and both MOSFETs must be kept as small as possible. Since all of the high switching currents occur in the input loop, the enclosed loop area must be kept small to minimize inductance and radiated and conducted noise emissions.

Application Information(Cont.)

Designing for minimum trace length is not the only factor for best design, often a optimum layout can be achieved by keeping the wide trace and using proper layer stacking to minimize the stray inductance.

It is important to keep the gate traces short, the IC must be close to the power switches. It is recommended to use at least 25 mil width or wider trace when. A good placement can help if the controller is placed in the middle of the two PWM channels.

Grounding requirements are always important in a buck converter layout, especially at high power. Power ground (PGND) should be returned to the bottom MOSFET source to provide the best gate current return path. Analog ground (AGND) should be used for the anaglog returns such as chip decoupling, frequency setiing, reference voltage (or soft starting cap), and the compensation.

This AGND shape should be single point connected to the PGND shape near the ground side of the output capacitors. This will provide noise free analog ground for operation stablity, and also provide best possible remote sensing for the feedback voltage.

In case two output rails need to be regulated, the AGND shape should single point connected to the geometric center of the PGND for the two point of loads. The single ponit tie is a must to prevent the power current from flowing on the AGND shape, so that the analog circuitry in the controller has an electrically quiet reference and to provide the greatest noise free operation. Keep in mind that the AGND pin is never allowed to have bigger than 1V voltage difference vs the PGND pin. This usually achievable by using a ground plane for PGND in PCB layout.

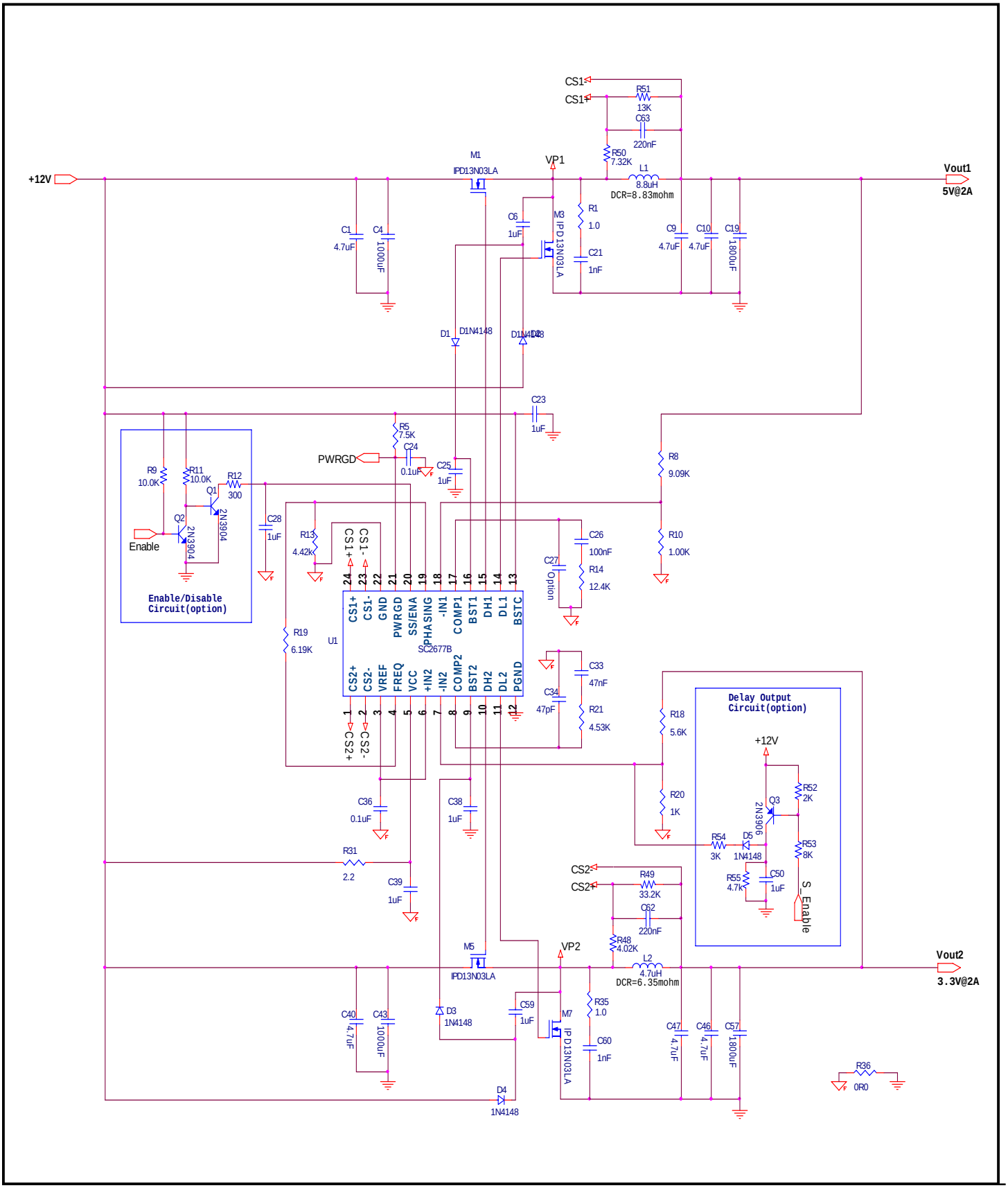
Using ground plane for PGND can reduce the physical separation between the two grounds, such that even the fast current transitions in the PGND plane can not generate voltage spikes exceeding the 1V level, therefore preventing unstable and erratic behavior from happening.

The feedback divider must be close to the IC and be returned to analog ground. Current sense traces must be run parallel and close to each other and to analog ground.

The IC must have a ceramic decoupling capacitor across its supply pins, mounted as close to the device as possible. The small ceramic, noise-filtering capacitors on the current sense lines should also be placed as close to the IC as possible.

Evaluation Schematic

Dual Independent outputs



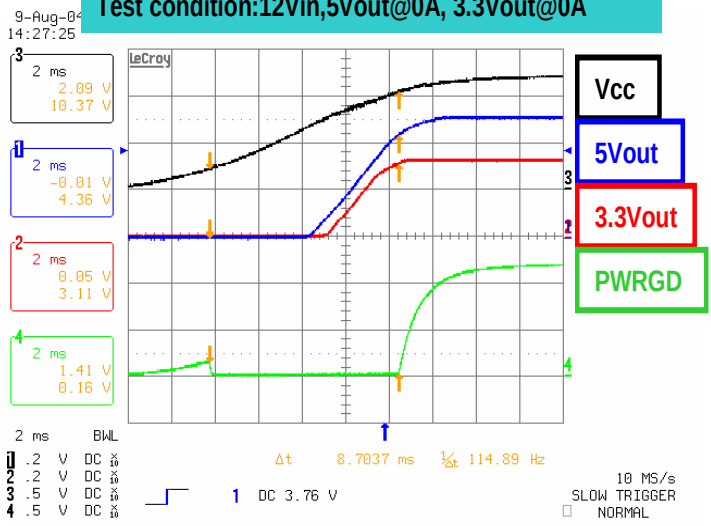
Evaluation Board - Bill of materials

Dual Independent outputs

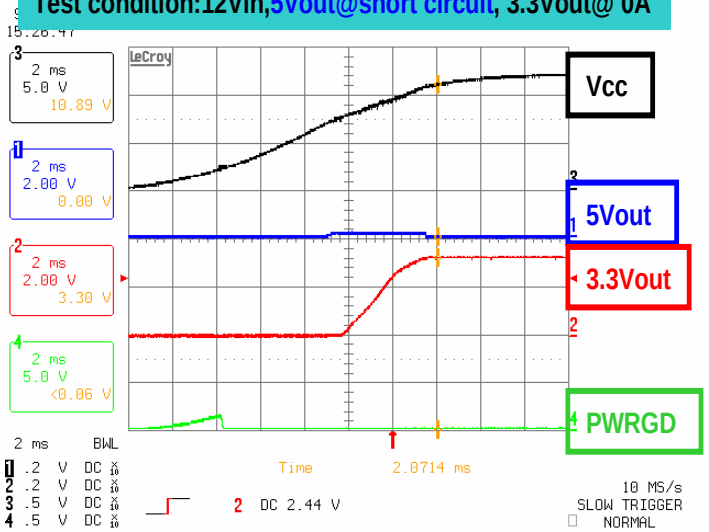
Item	Reference	Quantity	Description	Part
1	C1,C9,C10,C40,C46,C47	6	16V Ceramic Cap, X7R	4.7uF
2	C4,C43	2	16V Aluminum Electrolytic Cap.	1000uF/16V
3	C19,C57	2	16V Aluminum Electrolytic Cap.	1800uF/16V
4	C6,C23,C25,C28,C38,C39,C59,C50	8	16V Ceramic Cap, X7R	1uF
5	C21,C60	2	16V Ceramic Cap, X7R	1nF
6	C24,C36	2	16V Ceramic Cap, X7R	0.1uF
7	C26	1	16V Ceramic Cap, X7R	100nF
8	C33	1	16V Ceramic Cap, X7R	47nF
9	C34	1	16V Ceramic Cap, X7R	47pF
10	C62,C63	2	16V Ceramic Cap, X7R	220nF
11	L1	1	Inductor	8.8uH/4m ohm
12	L2	1	Inductor	4.7uH/4m ohm
13	M1,M3,M5,M7	4	30V N-Channel MOSFET	IPD13N03LA
14	D1,D2,D3,D4,D5	5	Small Signal Diode	1N4148
15	Q1,Q2	2	NPN General Purpose Amplifier	2N3904
16	Q3	1	PNP General Purpose Amplifier	2N3906
17	R1,R35	2	SM 5%	1ohm
18	R5	1	SM 5%	7.5K
19	R8	1	SM 5%	9.09K
20	R9,R11	2	SM 5%	10K
21	R10	1	SM 5%	1K
22	R12	1	SM 5%	300ohm
23	R13	1	SM 5%	4.42K
24	R14	1	SM 5%	12.4K
25	R18	1	SM 5%	5.6K
26	R19	1	SM 5%	6.19K
27	R20	1	SM 5%	1K
28	R21	1	SM 5%	4.53K
29	R31	1	SM 5%	2.2ohm
30	R36	1	SM 5%	0ohm
31	R48	1	SM 5%	4.02K
32	R49	1	SM 5%	33.2K
33	R50	1	SM 5%	7.32K
34	R51	1	SM 5%	13K
35	R52	1	SM 5%	2K
36	R53	1	SM 5%	8K
37	R54	1	SM 5%	3K
38	R55	1	SM 5%	4.7K
39	U1	1	PWM controller	SC2677B

Performance (Dual output)

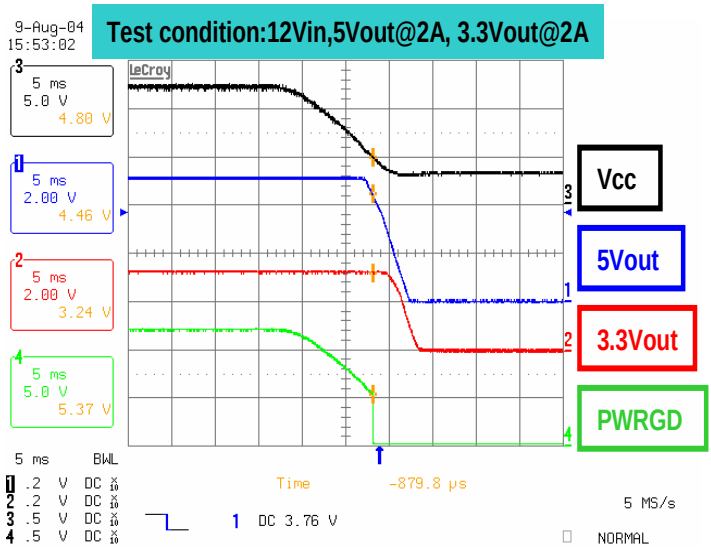
Test condition:12Vin,5Vout@0A, 3.3Vout@0A



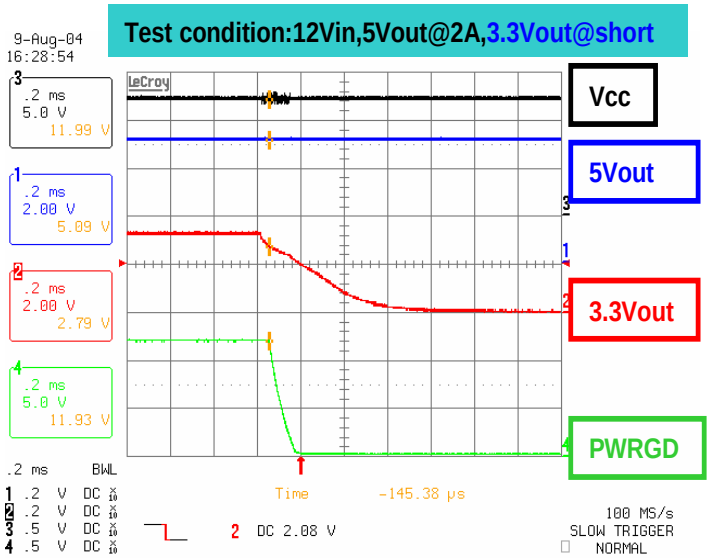
Test condition:12Vin,5Vout@short circuit, 3.3Vout@ 0A



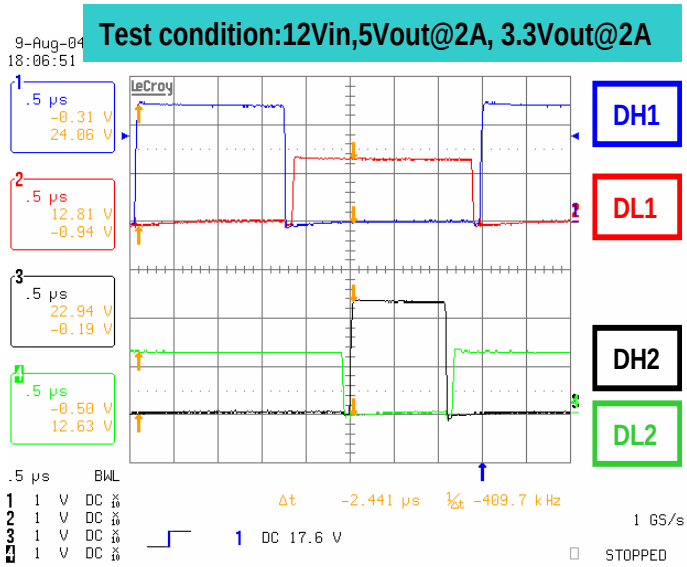
Test condition:12Vin,5Vout@2A, 3.3Vout@2A



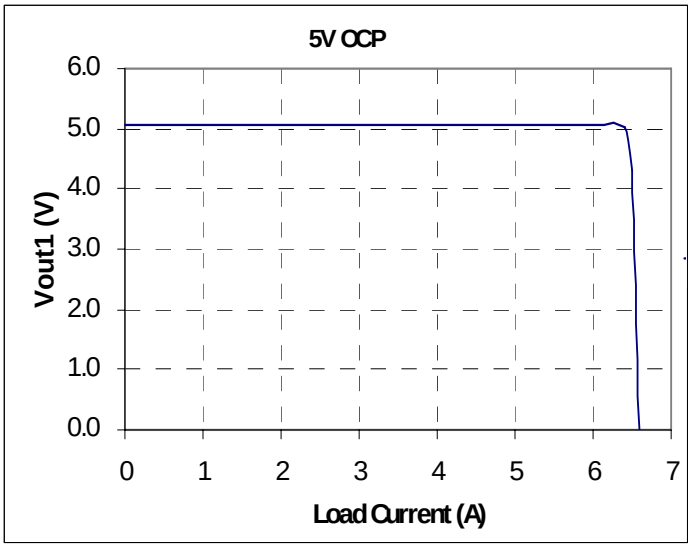
Test condition:12Vin,5Vout@2A,3.3Vout@short

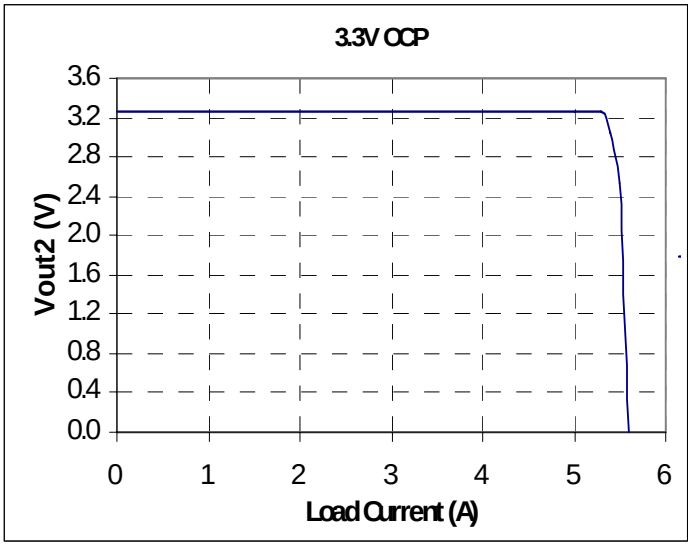


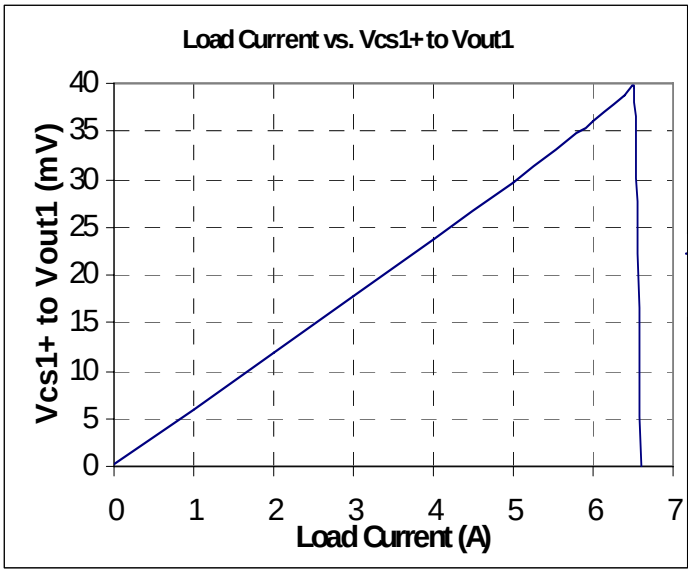
Test condition:12Vin,5Vout@2A, 3.3Vout@2A

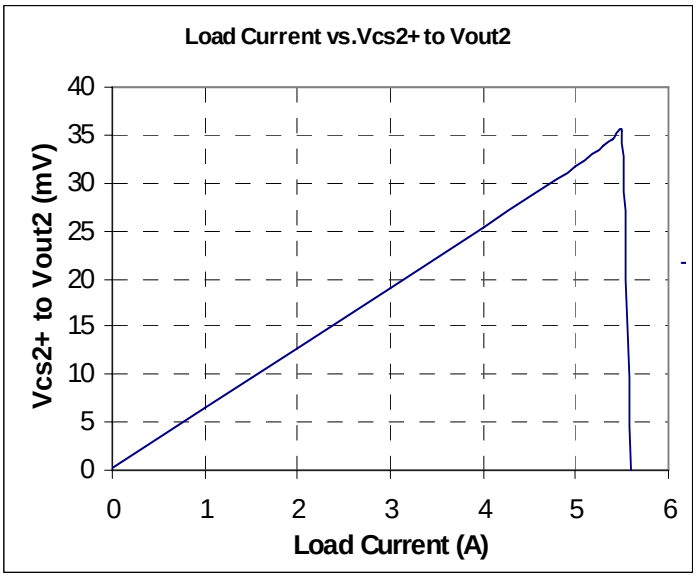


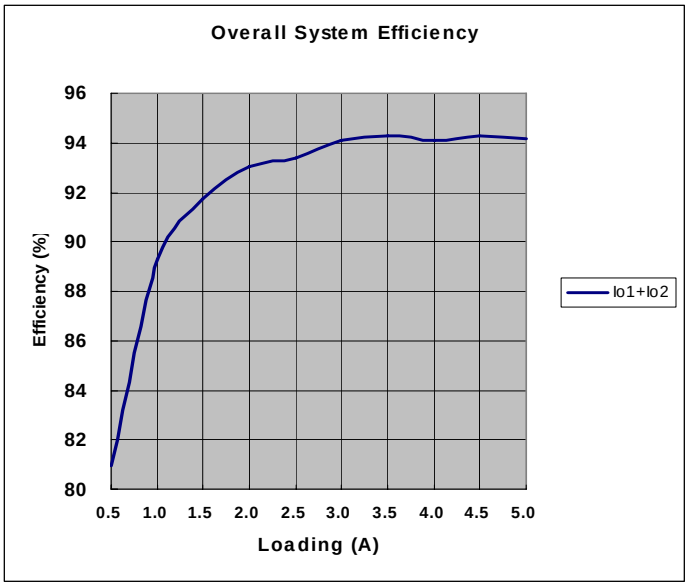
Performance (Dual output)





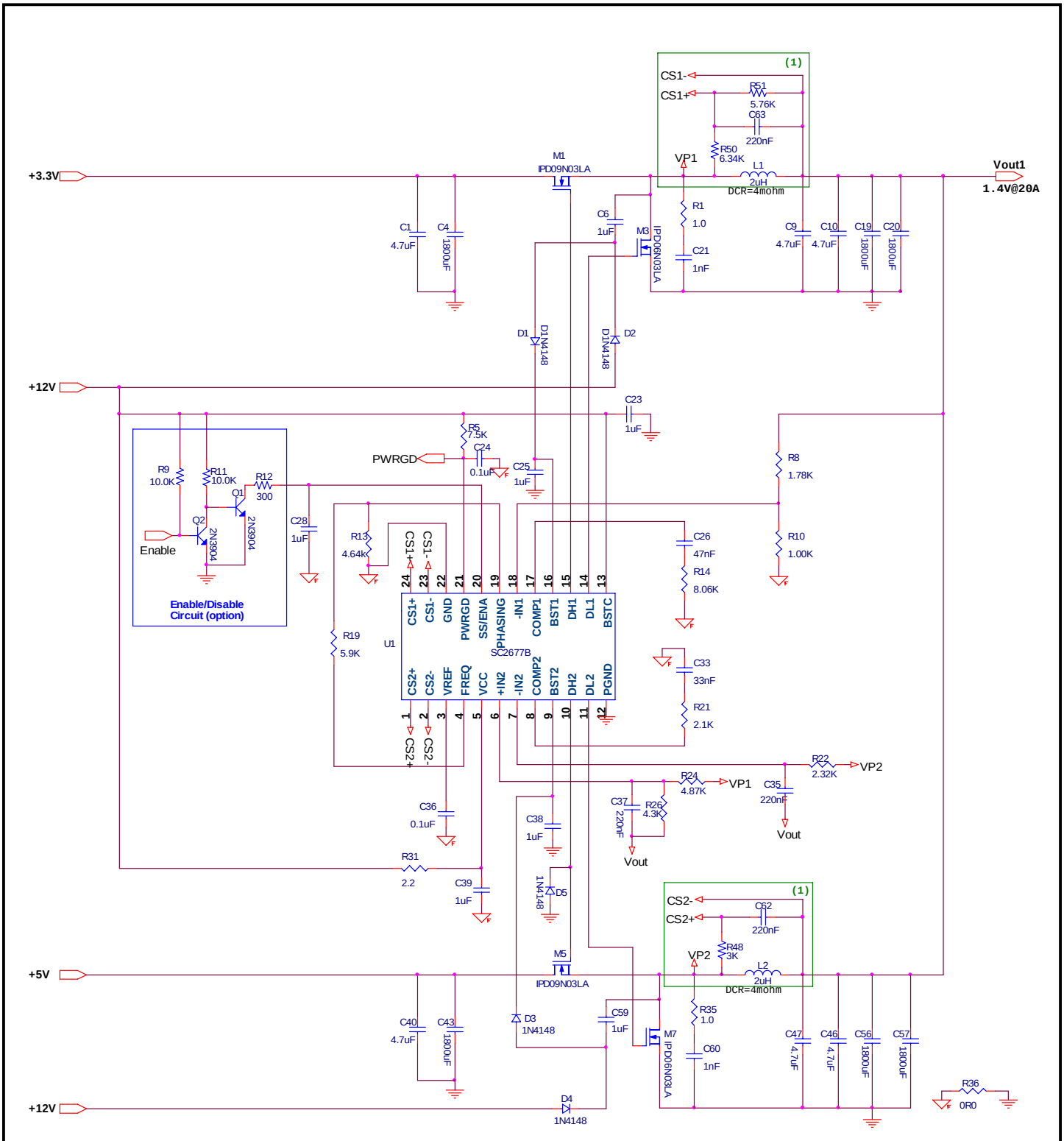






Evaluation Schematic (Cont.)

Single output, Current share Mode



Note (1) : Current Scale. Master channel current weighting factor is around 0.68 * Io, Slaver is around 0.32 * Io

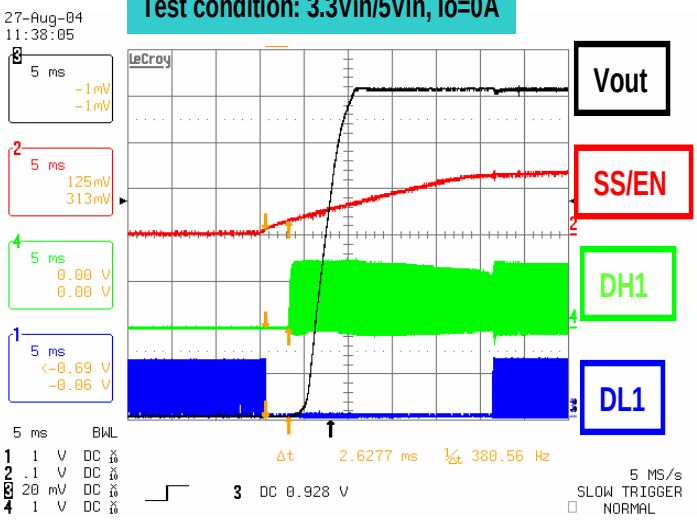
Evaluation Board - Bill of materials

Single output, Current share Mode

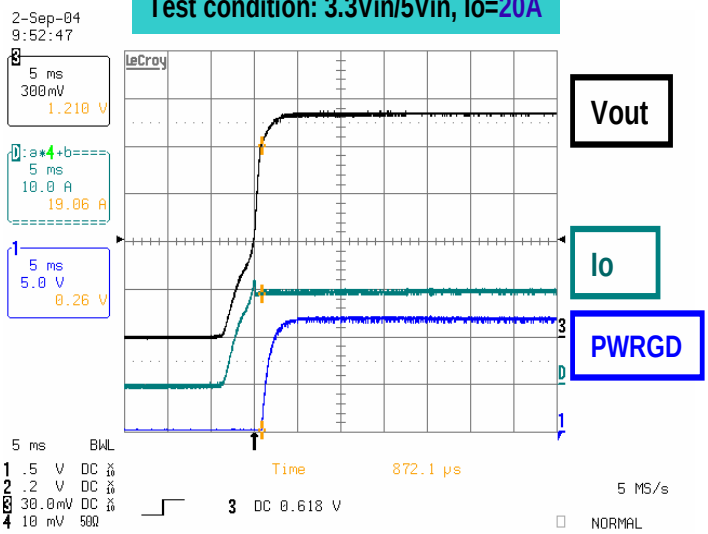
Item	Reference	Quantity	Description	Part
1	C1,C9,C10,C40,C46,C47	6	16V Ceramic Cap, X7R	4.7uF
2	C4,C19,C20,C43,C56,C57	6	16V Aluminum Electrolytic Cap.	1800uF/16V
3	C6,C23,C25,C28,C38,C39,C59	7	16V Ceramic Cap, X7R	1uF
4	C24,C36	2	16V Ceramic Cap, X7R	0.1uF
5	C26	1	16V Ceramic Cap, X7R	47nF
6	C33	1	16V Ceramic Cap, X7R	33nF
7	C35,C37,C62,C63	4	16V Ceramic Cap, X7R	220nF
8	L1,L2	2	Inductor	2uH/4m ohm
9	M1,M5	2	25V N-Channel MOSFET	IPD09N03LA
10	M3,M7	2	25V N-Channel MOSFET	IPD06N03LA
11	D1,D2,D3,D4,D5	5	Small Signal Diode	1N4148
12	Q1,Q2	2	NPN General Purpose Amplifier	2N3904
13	R1,R35	2	SM 5%	1ohm
14	R5	1	SM 5%	7.5K
15	R8	1	SM 5%	1.78K
16	R9,R11	2	SM 5%	10K
17	R10	1	SM 5%	1K
18	R12	1	SM 5%	300ohm
19	R13	1	SM 5%	4.64K
20	R14	1	SM 5%	8.06K
21	R19	1	SM 5%	5.9K
22	R21	1	SM 5%	2.1K
23	R22	1	SM 5%	2.32K
24	R24	1	SM 5%	4.87K
25	R26	1	SM 5%	4.3K
26	R31	1	SM 5%	2.2ohm
27	R36	1	SM 5%	0ohm
28	R48	1	SM 5%	3K
29	R50	1	SM 5%	6.34K
30	R51	1	SM 5%	5.76K
31	U1	1	PWM controller	SC2677B

Performance (Single output)

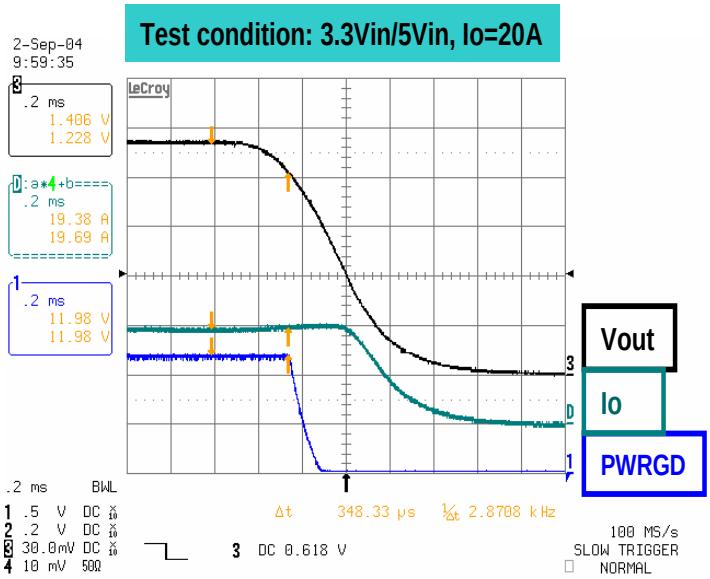
Test condition: 3.3Vin/5Vin, Io=0A



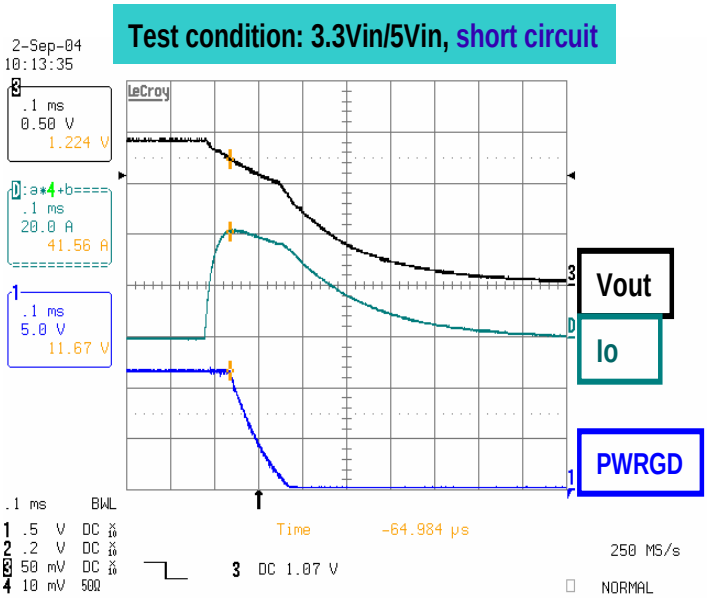
Test condition: 3.3Vin/5Vin, Io=20A



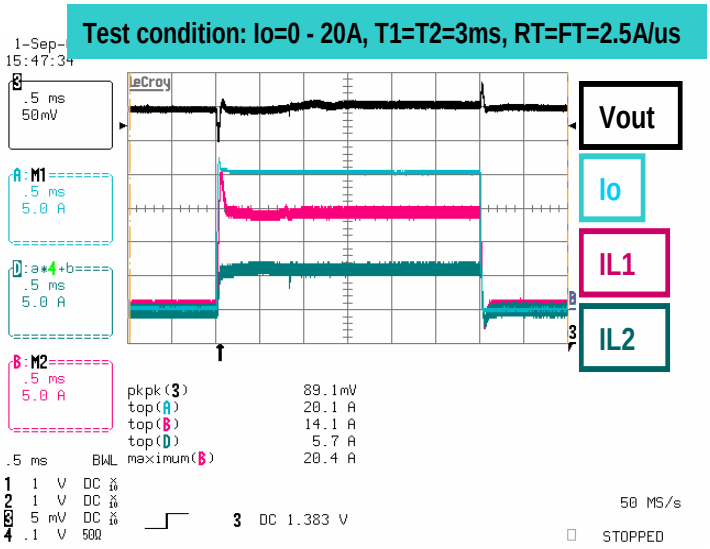
Test condition: 3.3Vin/5Vin, Io=20A



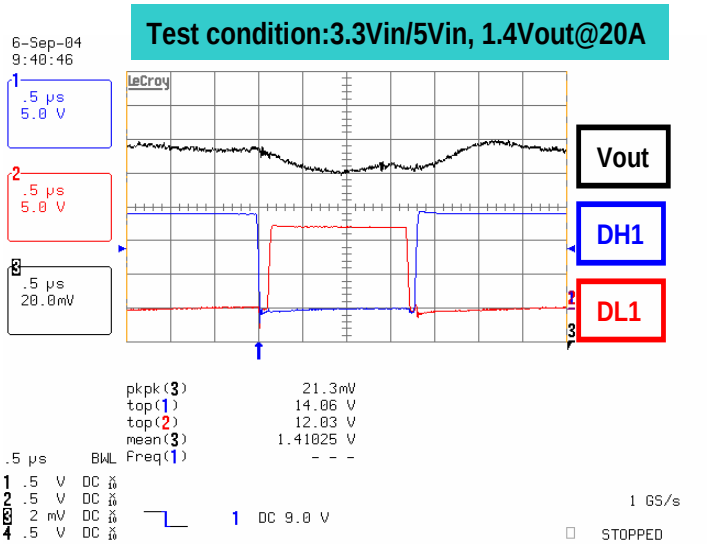
Test condition: 3.3Vin/5Vin, short circuit



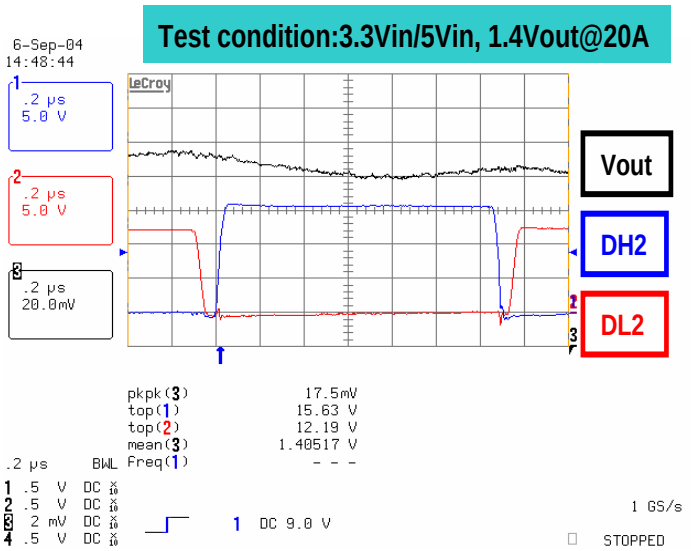
Test condition: Io=0 - 20A, T1=T2=3ms, RT=FT=2.5A/us

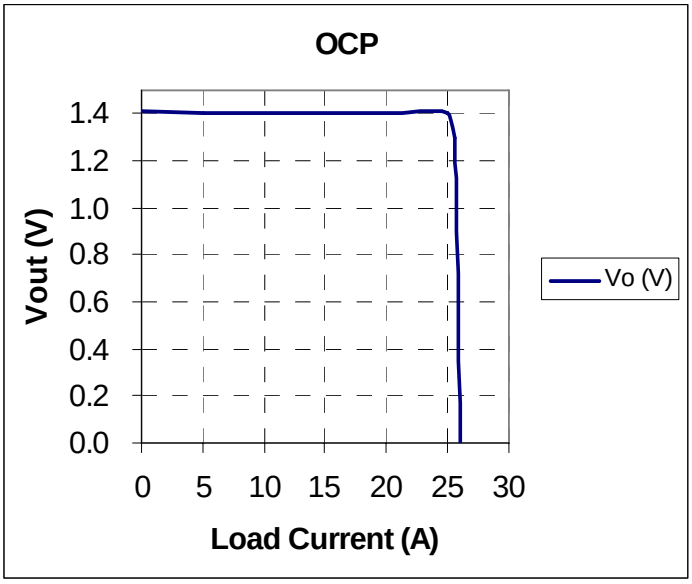


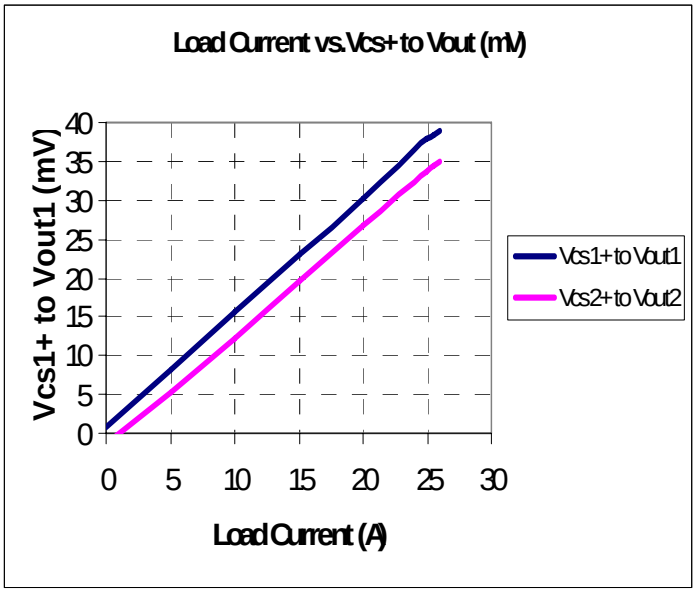
Test condition:3.3Vin/5Vin, 1.4Vout@20A

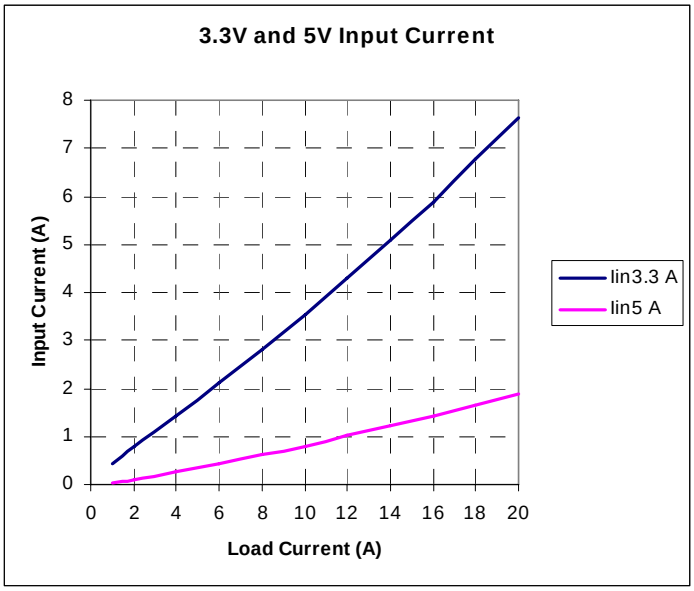


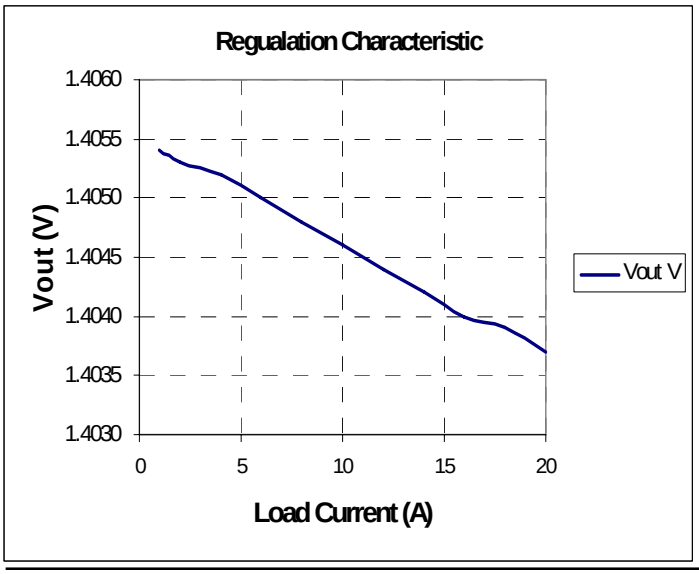
Performance (Single output)

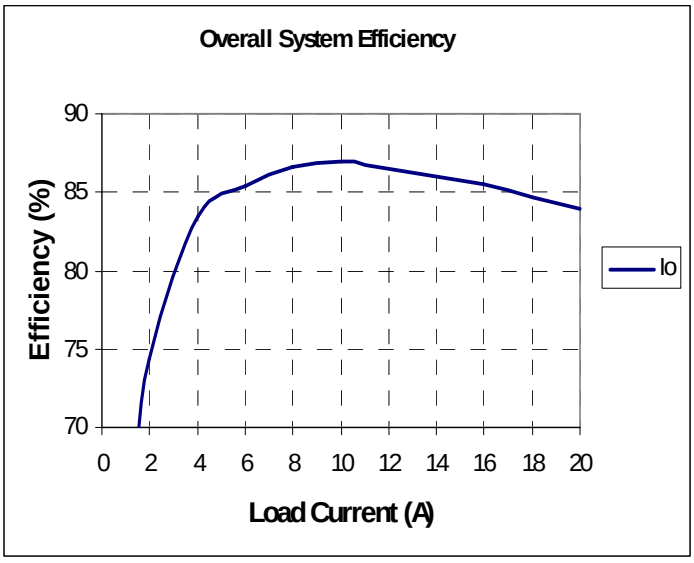




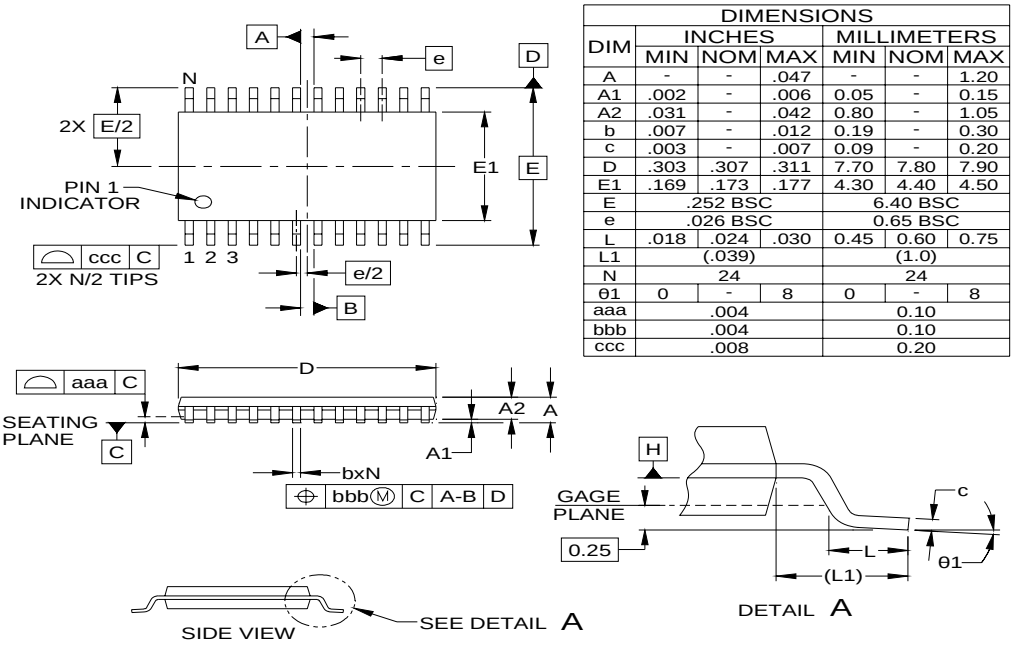








Outline Drawing - TSSOP-24

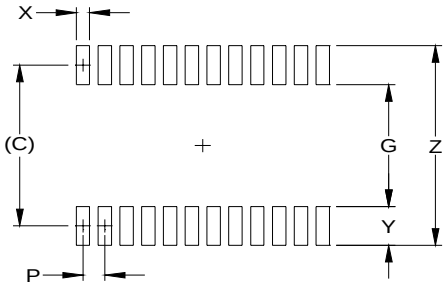


DIM	INCHES MIN	INCHES NOM	INCHES MAX	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.303	.307	.311	7.70	7.80	7.90
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	24			24		
θ1	0	-	8	0	-	8
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AD.

Land Pattern - TSSOP-24



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

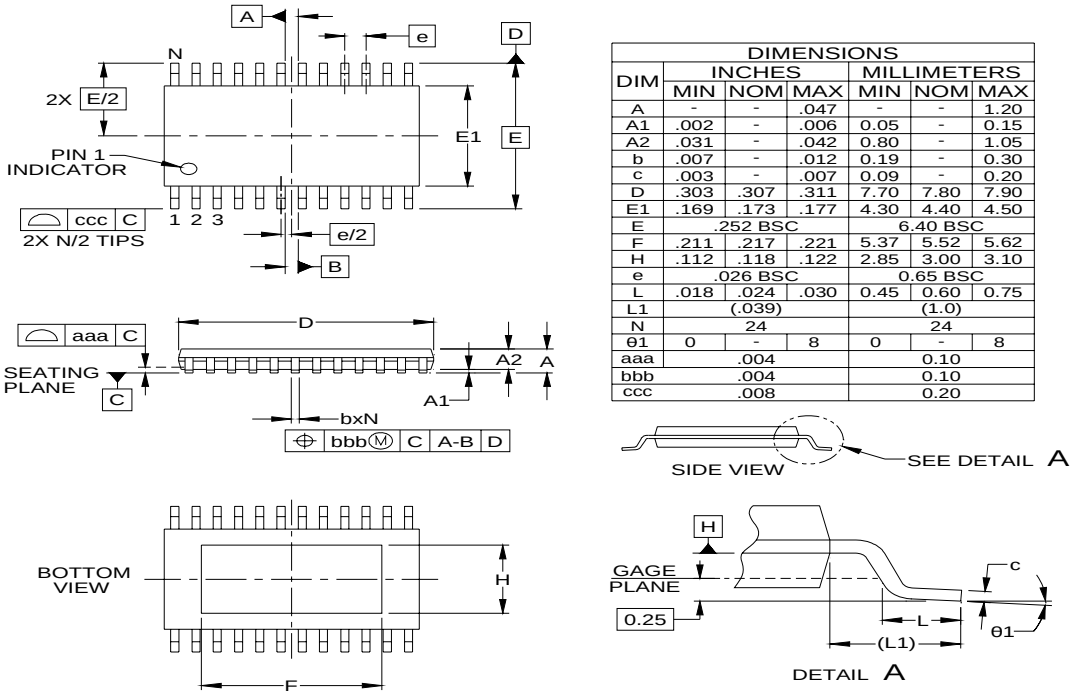
NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

Outline Drawing - TSSOP-24 EDP



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.303	.307	.311	7.70	7.80	7.90
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
F	.211	.217	.221	5.37	5.52	5.62
H	.112	.118	.122	2.85	3.00	3.10
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	24			24		
θ1	0	-	8	0	-	8
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

OTES:

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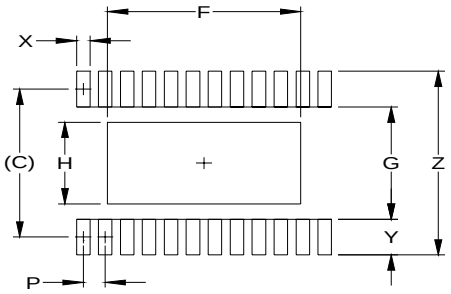
Land Pattern - TSSOP-24 EDP



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.222)	(5.65)
F	.225	5.72
G	.161	4.10
H	.126	3.20
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

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