

TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

SSM6N37CTD

○ Power Management Switch Applications

- 1.5V drive
- Low ON-resistance
 - $R_{on} = 5.60 \Omega$ (max) (@ $V_{GS} = 1.5 V$)
 - $R_{on} = 4.05 \Omega$ (max) (@ $V_{GS} = 1.8 V$)
 - $R_{on} = 3.02 \Omega$ (max) (@ $V_{GS} = 2.5 V$)
 - $R_{on} = 2.20 \Omega$ (max) (@ $V_{GS} = 4.5 V$)

Unit: mm

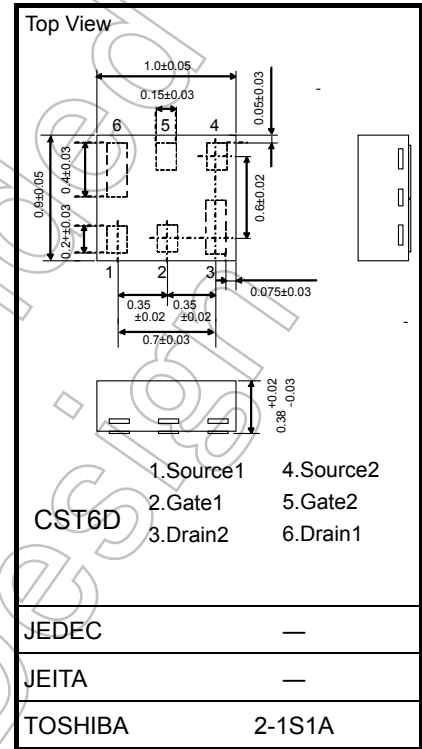
Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

| Characteristic | Symbol | Rating | Unit |
|-------------------------|----------------|------------|------|
| Drain-source voltage | V_{DSS} | 20 | V |
| Gate-source voltage | V_{GSS} | ± 10 | V |
| Drain current | DC | I_D | 250 |
| | Pulse | I_{DP} | 500 |
| Drain power dissipation | P_D (Note 1) | 140 | mW |
| Channel temperature | T_{ch} | 150 | °C |
| Storage temperature | T_{stg} | -55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

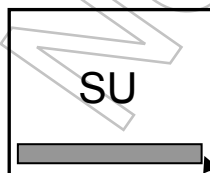
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating
 Mounted on an FR4 board
 (10 mm × 10 mm × 1.0 mm, Cu Pad: 100 mm²)



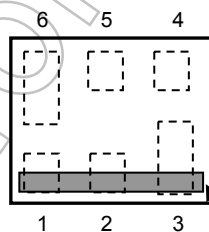
Weight : 1.0 mg (typ.)

Marking



Polarity mark

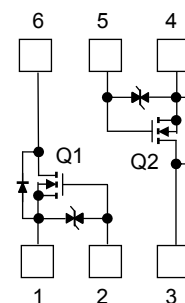
Pin Condition (top view)



Polarity mark (on the top)

*Electrodes: on the bottom

Equivalent Circuit (top view)



Start of commercial production
 2009-12

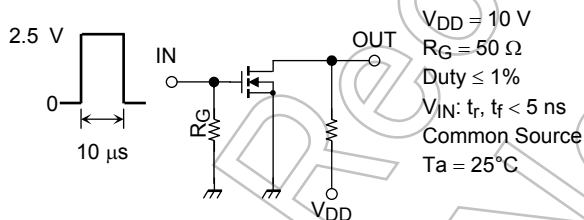
Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

| Characteristic | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------|---------------|--|--|------|---------|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$ | 20 | — | — | V |
| | $V_{(BR)DSX}$ | $I_D = 1 \text{ mA}, V_{GS} = -10 \text{ V}$ | 12 | — | — | |
| Drain cutoff current | I_{DSS} | $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ | — | — | 1 | μA |
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$ | — | — | ± 1 | μA |
| Gate threshold voltage | V_{th} | $V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$ | 0.35 | — | 1.0 | V |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = 3 \text{ V}, I_D = 100 \text{ mA}$ (Note 2) | 0.14 | 0.28 | — | S |
| Drain-source ON-resistance | $R_{DS(ON)}$ | $I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$ (Note 2) | — | 1.65 | 2.20 | Ω |
| | | $I_D = 50 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note 2) | — | 2.16 | 3.02 | |
| | | $I_D = 20 \text{ mA}, V_{GS} = 1.8 \text{ V}$ (Note 2) | — | 2.66 | 4.05 | |
| | | $I_D = 10 \text{ mA}, V_{GS} = 1.5 \text{ V}$ (Note 2) | — | 3.07 | 5.60 | |
| Input capacitance | C_{iss} | $V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | — | 12 | — | pF |
| Output capacitance | C_{oss} | | — | 5.5 | — | |
| Reverse transfer capacitance | C_{rss} | | — | 4.1 | — | |
| Switching time | Turn-on time | t_{on} | $V_{DD} = 10 \text{ V}, I_D = 100 \text{ mA}$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}, R_G = 50 \Omega$ | — | 18 | ns |
| | Turn-off time | t_{off} | | — | 36 | |
| Drain-source forward voltage | V_{DSF} | $I_D = -250 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 2) | — | -0.9 | -1.2 | V |

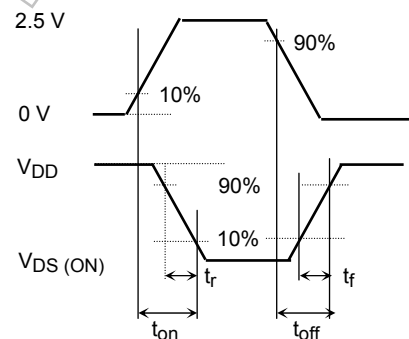
Note 2: Pulse test

Switching Time Test Circuit (Q1, Q2 Common)

(a) Test Circuit



(b) V_{IN}



Precaution

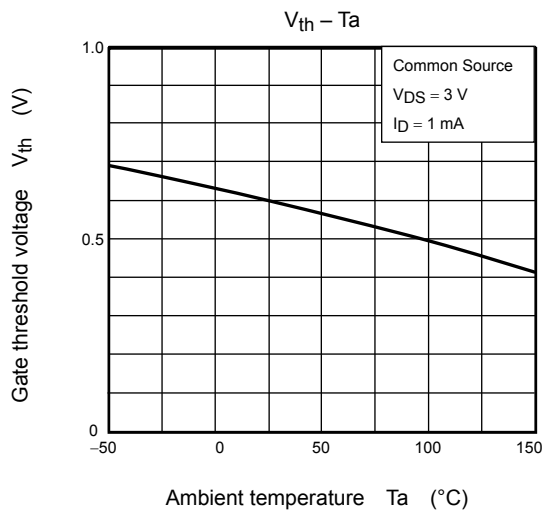
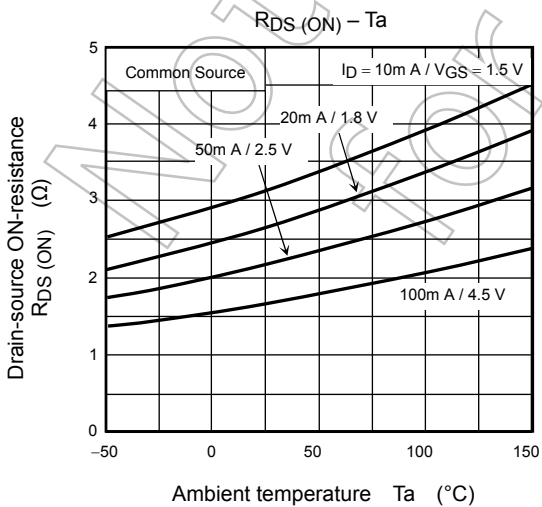
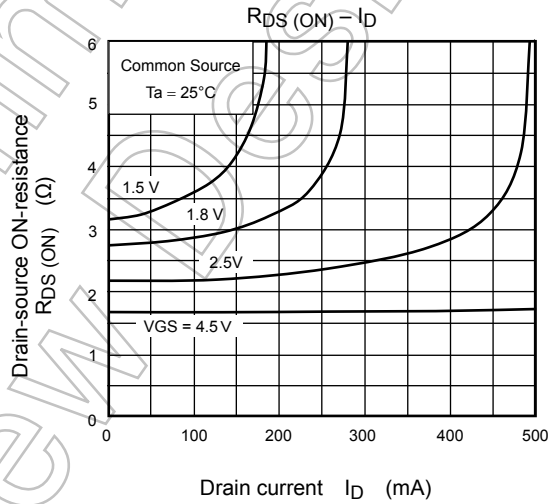
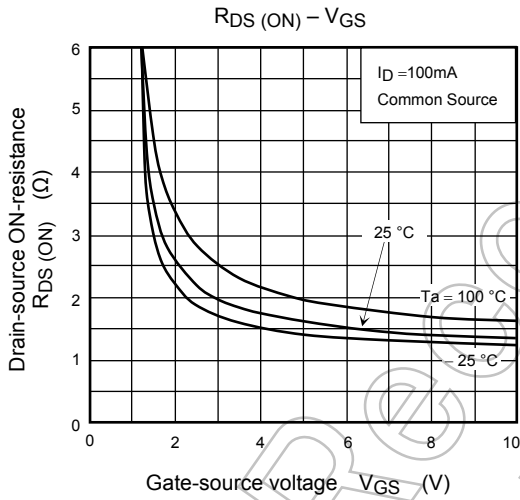
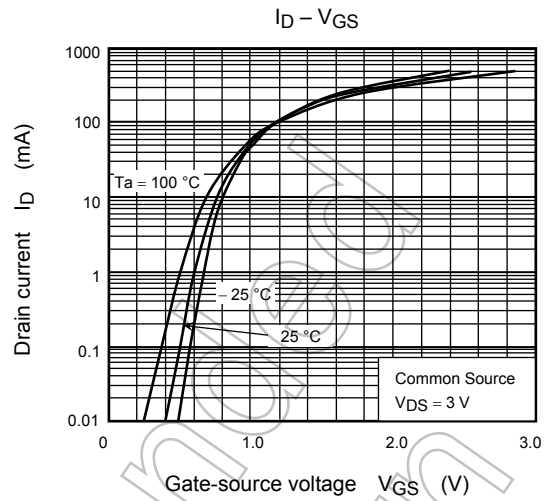
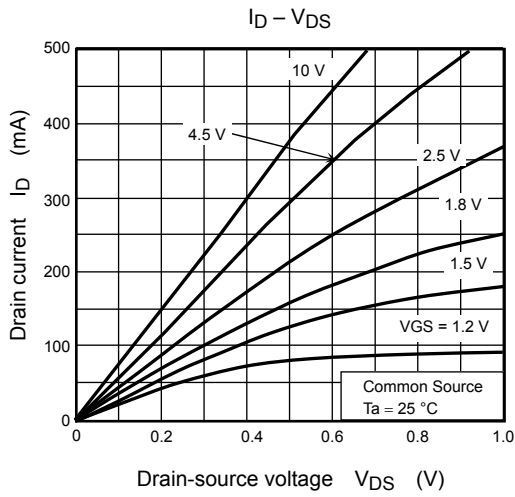
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (1mA for the SSM6N37CTD). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

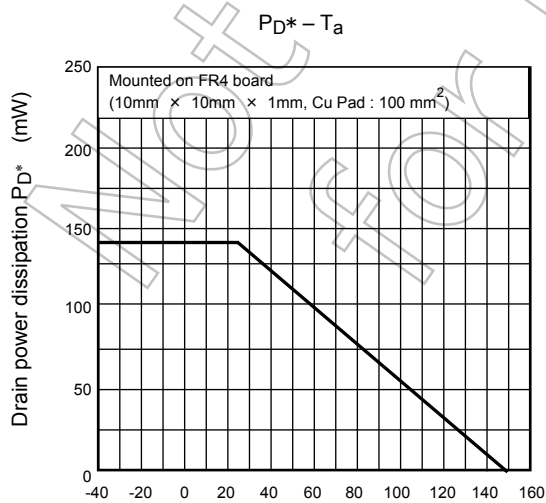
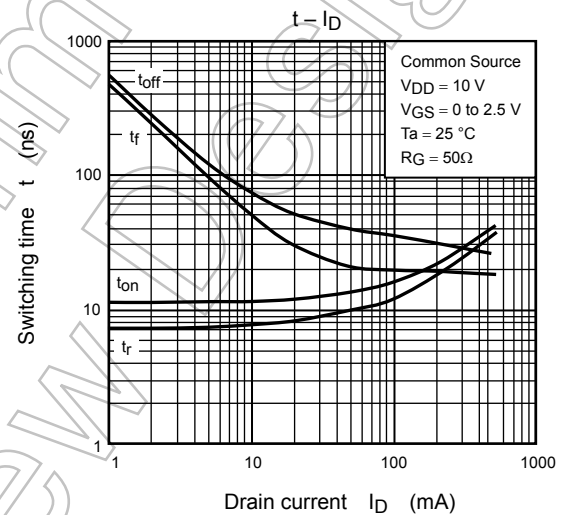
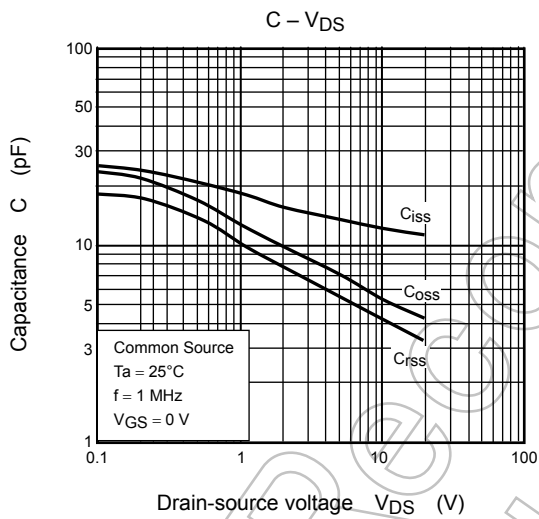
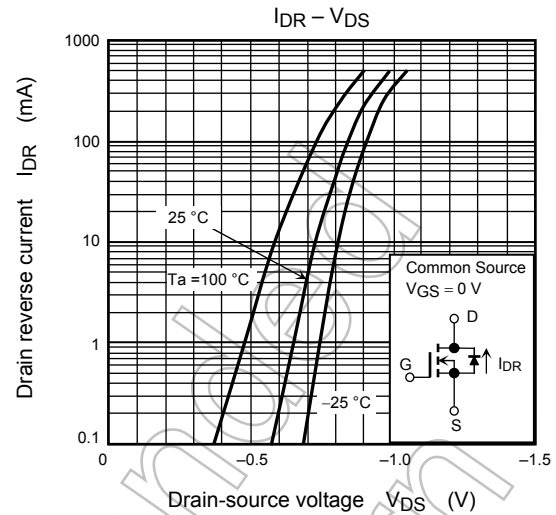
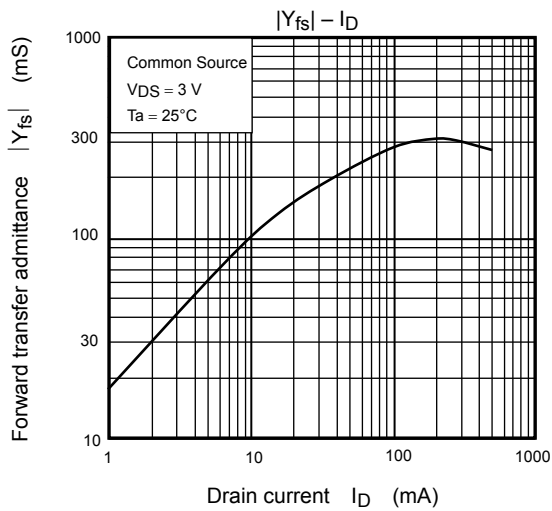
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

(Q1, Q2 Common)



(Q1, Q2 Common)



*:Total Rating Ambient temperature T_a (°C)

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