UM2185
User manual

Getting started with the STEVAL-ISB041V1 Li-Ion/Li-Po battery power management evaluation board based on STBC02

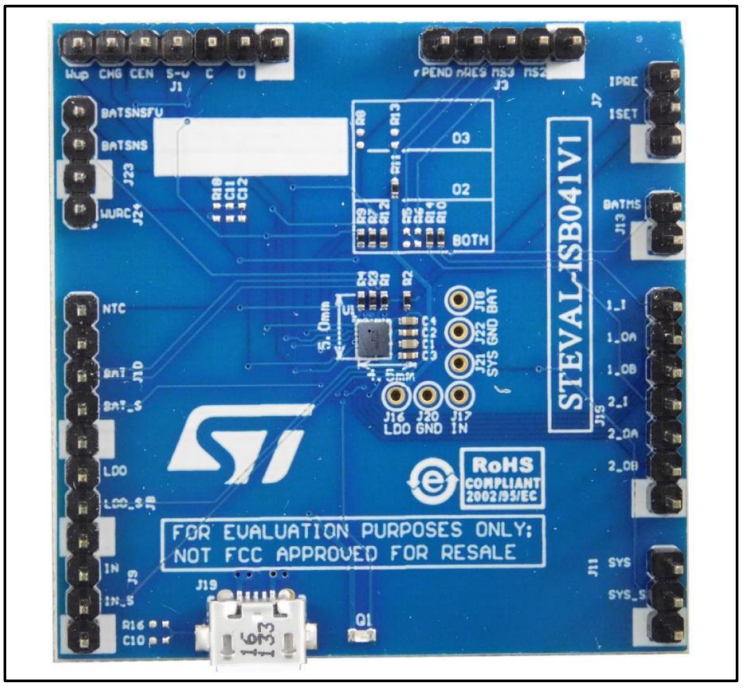
Introduction

The STEVAL-ISB041V1 evaluation board is based on STBC02 Li-Ion and Li-Po linear battery management device, integrating a CC-CV charger algorithm, an always-on LDO, smart-reset Watchdog, a protection circuit module (PCM) and a dual SPDT switch matrix.

The device is able to charge batteries at a 450 mA continuous maximum current with few external passive components, so the whole application can be reduced down to as little as 4.5 mm x 5 mm.

The module can deliver 60 mA charging current and supply the system up to 300 mA while powered by a standard 5 V output DC power supply. It is suitable for battery operated equipment, wearable devices, fitness portable devices, MP3 players, healthcare and medical instrumentation, body worn equipment, etc.

Figure 1: STEVAL-ISB041V1 evaluation board



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1 Getting started

1.1 Board overview

The STEVAL-ISB041V1 evaluation board size is 50 mm x 50 mm.

The PCB is made by using FR4 glass epoxy support with 4 copper layers.

The device features:

- Charges single-cell Li-Ion/Li-Po batteries with CC-CV algorithm and charge termination
- Fast charge current programmable from 1 mA to 450 mA
- Pre-charge current programmable from 1 mA to 450 mA
- Adjustable floating voltage up to 4.45 V
- Integrated always-on low quiescent LDO regulator
- Battery over-charge and over-discharge protections
- Overcurrent protection
- Shipping mode exit input
- Integrated dual 3 Ω SPDT load switches
- Integrated smart reset / watchdog logic
- Single wire control interface
- RoHS compliant

1.2 Input/output connectors

The input/output connectors (J1-J23) provide the necessary probing signals:

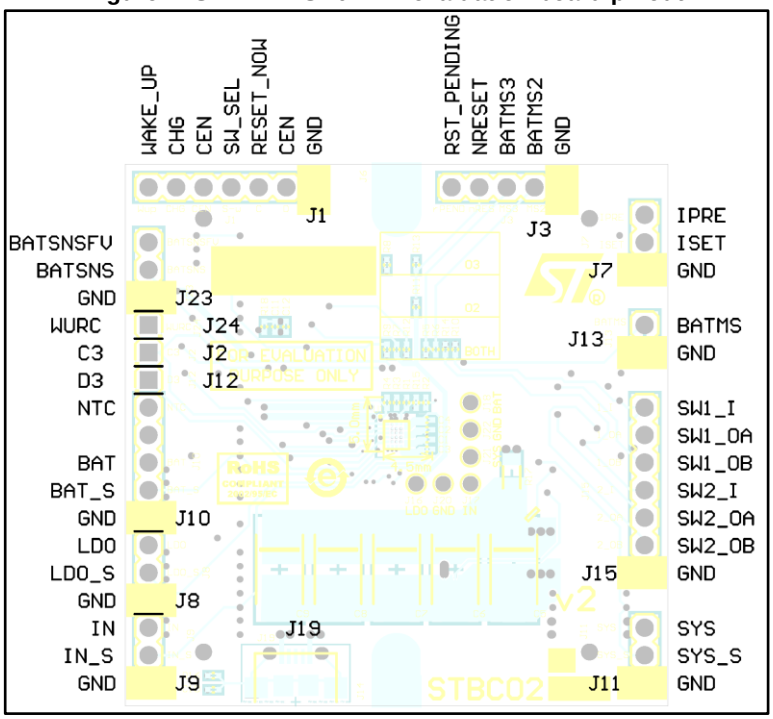
- Kelvin connection points for input and output voltage;
- enable signal input;
- multiple GND connection;
- s-wire input

Table 1: Input/output connector: pin description

Connector	Pin number	Symbol	Signal name	Pin description
J1	2	D	CEN	Charger enable pin
	3	C	RESET_NOW	Smart reset input signal
	4	S-w	SW_SEL	Serial s-wire input
	5	CEN	CEN	Charger enable pin
	6	CHG	CHG	Charging/fault flag
	7	Wup	Wake-Up	Shipping mode exit input pin
J3	2	MS2		Reserved
	3	MS3		Reserved
	4	nRES		Smart reset output signal
	5	rPEND		Smart reset output signal
J7	2	ISET	ISET	Fast-charge current programming resistor

Connector	Pin number	Symbol	Signal name	Pin description
	3	IPRE	IPRE	Pre-charge current programming resistor
J8	2	LDO	LDO	LDO output
	3	LDO_S	LDO	LDO output sensing
J9	2	IN	IN	Input supply voltage
	3	IN_S	IN	Input supply voltage sensing
J10	2	BAT_S	BAT	Battery sensing
	3	BAT	BAT	Battery - positive terminal
	4	----	----	Reserved
	5	NTC	NTC	Battery temperature monitor pin
J11	2	SYS	SYS	System output
	3	SYS_S	SYS	System output sensing
J13	2	BATMS	BATMS	Battery voltage measurement pin
J15	2	1_I	SW1_I	
	3	1_OA	SW1_OA	
	4	1_OB	SW1_OB	
	5	2_I	SW2_I	
	6	2_OA	SW2_OA	
	7	2_OB	SW2_OB	
J19	VBUS	----	IN	Input supply voltage
J23	2	BATSNS	BAT	Battery voltage sensing
	3	BATSNSFV	BATSNSFV	Floating voltage sensing
J1, J3, J7, J8, J9, J10, J11, J13, J15, J23	1		GND	Ground connection

Figure 2: STEVAL-ISB041V1 evaluation board pinout



1.3 Test procedure and technical recommendations

STBC02 linear battery management IC is designed to manage the whole battery charging procedure, powering the system through the power path node output (SYS unregulated voltage rail) via a low quiescent linear regulator output.

Being a linear device, the charger is most efficient when the input voltage is only slightly above the battery voltage (V_{IN} = 4.55 to 5.4 V).

A low input voltage (inferior to the sum of the OUT voltage plus the dropout voltage) results in degraded performance. Excessive input voltage (>5.4 V) results in power dissipation and reduced performance (it halves the charge current if thermal warning is reached) due to the IC thermal management protection circuit.

The IC is set to 16 V and is not damaged with a lower V_{IN} voltage, but it is disabled by any V_{IN} voltage over the overvoltage protection threshold (5.9 V).

Section 1.3.2: "Procedure to test a typical full charging cycle" describes the procedure to test and observe a typical full charging cycle. The CC-CV algorithm is linked to the battery voltage level. If a battery having V_{BAT}>3 V is plugged, the pre-charge phase is skipped and the device directly enters in fast charge mode.

1.3.1 Recommended equipment

- Bench power supply (+5 V_{DC}) with current limit set to ~1-2 A or USB wall adaptor with micro USB plug;
- oscilloscope with one current and three high impedance voltage probes;
- programmable digital waveform generator (or standard MCU to implement digital sequence).

1.3.2 Procedure to test a typical full charging cycle

The three most important STBC02 functional modes are:

- battery mode: V_{BAT} valid range, system up and running, V_{IN} invalid range;
- shutdown mode: device supplied by battery but in shutdown mode;
- V_{IN} mode: V_{IN} valid range present.

The charger is designed to be used with Li-Ion batteries (Li-Ion nominal battery voltage is 3.7-3.8V). V_{BAT} range is 0 (dead battery) to 4.5 V (overcharged battery). The device input operating supply voltage is 4.5 to 5.5 V_{DC}.

The procedure to demonstrate this power path charger is:

1. Connect one high impedance probe to J1/pin6 (CHG) vs GND.
2. Connect one high impedance probe to J10/pin2 (BAT_S) vs. GND.
3. Place the current probe on the positive battery terminal wire.
4. Connect (fully discharged) battery (e.g. 2.5 V) to J10/pin3 (VBAT) vs. GND.
5. Connect power supply ~5.0 V to J9/pin3 (IN) vs GND.
6. Battery starts charging by IPRE charging current. Verify that IBAT is ~6 mA (10% of IFAST).
7. Connect a 33 Ω, ½-W resistor to J8/pin3 (LDO) vs. GND.
8. With a high impedance probe, verify that LDO (node LDO_S - J8/pin2) output is 3.1 V.

   CHG toggles (6 Hz).

   When battery voltage level exceeds VPRE (3 V), the charging current changes from IPRE to IFAST and increases to ~ 60 mA (IFAST setup). During this phase, CHG is still toggling at the same frequency if no warning/alarm is detected. In this condition, LDO and system are powered by the power supply.
9. Verify with high impedance probe that SYS voltage (J11/pin2) is approximately 5 V (IN node level minus internal MOS drop).

   You can stop the charging cycle by a jumper to short CEN to GND (short J1/pin2 to J1/pin1) just to verify CEN pin is functional.
10. Verify that the charger stops.

    CHG changes state and its level goes low.
11. Remove short CEN to GND to continue charging.
12. Charge the battery fully

    At a certain battery level (typical 4.2 V), charging current starts falling and battery voltage level remains constant at V_{FLOAT} level.
13. Battery charging is automatically stopped when battery charging current drops under 5 % of I_{FAST}.
14. Disconnect charger to observe device behavior in battery mode.

    Battery starts discharging to supply the load connected to LDO output; the current probe measures a negative value (~VLDO/resistive load).
15. Verify through high impedance probe that SYS_S voltage (J11/pin2) is V_{BAT} voltage minus V_{BAT} equal to VSYS MOSFET RDSON multiplied by load current.
16. Remove resistive load from the LDO output.

17 Disconnect and reconnect battery.

SYS and LOD node are not supplied now, as the device is in shutdown mode. To enter battery mode, you have to pull WakeUp pin to VBAT level (to be precise, the WakeUp pin has to exceed 3.0 V level).

2 GND pins

All GND pins are connected by a dedicated metallic layer: the evaluation board GND routing strategy does not feature separated GND branches. The only exception is the battery negative terminal connection.

Table 2: STEVAL-ISB041V1 evaluation board pin functions

Name	Function
IN_S	Sensing: to measure input voltage directly on C1 capacitor
IN	Forcing: input dedicated to charger positive terminal
LDO_S	Sensing: to measure input voltage directly on C3 capacitor
LDO	Forcing: output pin dedicated to linear voltage regulator loading
BAT_S	Sensing: to measure battery voltage directly on C4 capacitor
BAT	Forcing: pin dedicated to battery positive terminal
NTC	NTC pin can be used to measure NTC pin voltage, to force NTC pin voltage by external voltage, or to connect dedicated NTC resistor when R4 is disassembled
BATSNS	This pin is dedicated to measure the BATSNS ball voltage. If R15 is removed, this pin can be used to sense the battery voltage closer to the battery positive terminal
BATSNSFV	This pin is dedicated to measure BATSNSFV ball voltage. R3 can be used to increase V_{FLOAT}
WAKE_UP	WakeUp – Shipping Mode exit: input dedicated to wakeup device by connecting Wakeup to BAT Pin internally pulled-down.
CHG	Charger indication pin: indicates valid input voltage by state (high or low) or charging status and fault conditions by toggling at different frequency.
CEN	Charger enable pin 0 = disabled floating = 1 = enabled. The pin is pulled up internally. CEN<0.4 V is taken as 0, CEN>1.6 V is taken as 1 Range 0.4 to 1.6 V as well as exceeding LDO nominal value is no allowed.
SW_SEL	Swire digital input
RESET_NOW	Digital input to reset logic
NRESET	Digital reset output signal
RST_PENDING	Digital input t reset logic
IPRE	Pre-charge current programming resistor node: pin dedicated to measure I_{PRE} resistor voltage.
ISET	Fast-charge current programming resistor node: pin dedicated to measure I_{SET} resistor voltage
BATMS	Battery voltage measurement pin. When enabled by swire, BAT voltage is connected to this pin through an internal switch with equivalent RON-BATMS.
SW1_I	Load switch SPDT1 input
SW1_OA	Load switch SPDT1 output A
SW1_OB	Load switch SPDT1 output B
SW2_I	Load switch SPDT2 input

Name	Function
SW2_OA	Load switch SPDT2 output A
SW2_OB	Load switch SPDT2 output B
SYS	Forcing: output pin dedicated to SYS loading
SYS_S	Sensing: to measure system voltage directly on C2 capacitor

NTC

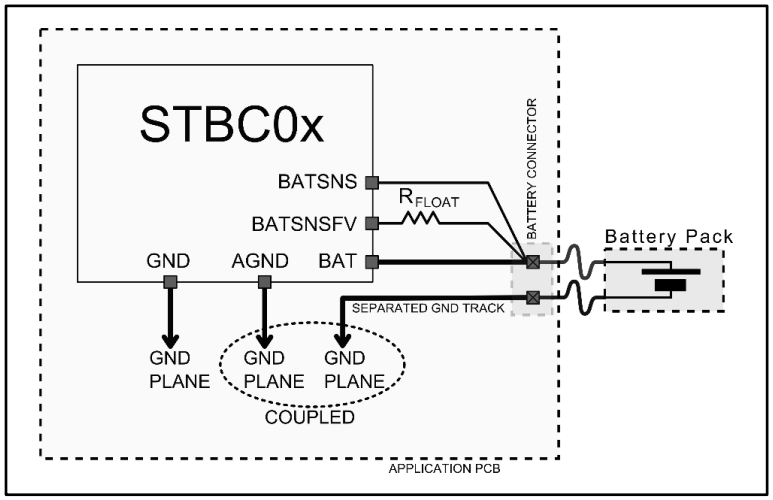
NTC is assembled on board (fixed value 10 kΩ, resistor R4). If real NTC use is requested, remove R4 and connect the real element between NTC node and GND. Couple this NTC element to the battery body properly.

BAT node

BAT node is reserved for battery positive terminal only. It is highly recommended to not connect any other circuits (e.g., workarounds, bias for any circuit) to this node.

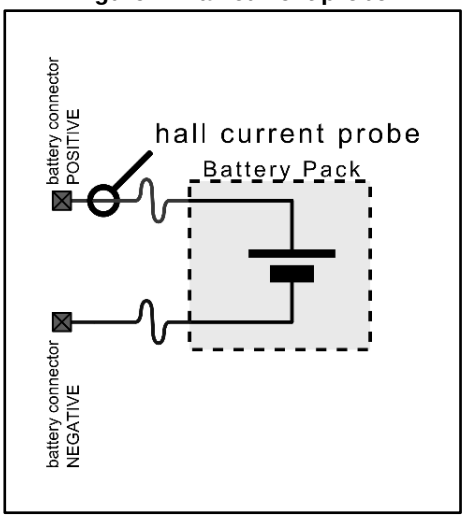
The figure below shows the correct BATSNS and BATSNSFV resistor routing to battery positive connector terminal for measurement accuracy.

Figure 3: STBC02 battery proper connection and routing



To avoid fault state conditions or other problems during device evaluation phase, it is recommended to use Hall effect oscilloscope current probes.

Figure 4: Hall current probe



Avoid connecting serial resistors between battery pack and device to measure current voltage drop.

Battery protection

STBC02 works well when the charger is plugged; battery protection is activated in case of fully discharged battery.

Safety timers do not support abnormally long delay between BAT node rise (protection stimulation) and protection deactivation.

SW_SEL

- input only
- internal pull-down: 500 k
- recommended operation voltage range: 0 V to LDO voltage level
- Idle in LOW (pull down recommended when not in use)
- single-wire peripheral communication pin
- via bitstream, the device can be controlled: charging current can be halved, switches can be switched on or off, and device can be (when in battery mode) suspended (shut down mode to avoid battery consumption).

CEN

- input
- internal pull-up: 500 k to LDO
- low = disabled charger
- high = enabled charger
- charger restart function

CHG

- output
- open drain
- external pull-up: ~10 k

WakeUp

- input
- internal pull-down: 500 k to GND
- tactile switch to battery (low to high transition) wakes up the device

RESET circuit

STBC02 is equipped with a multipurpose reset circuit. The mode can be selected by s-wire bus:

- smart reset generator in Smart reset mode (default after POR)
- watchdog in Watchdog mode

Smart reset mode application example

- Battery operated waterproof solutions or minimalistic devices (wearable sport wrap, single ear headset) may not have any buttons. When the software crashes, the only way to reset the device (processor) is by USB plug.
- After each USB connection, RST_PENDING triggers the processor to save all data 4000 miliseconds before the nRESET pulse triggers reset. The signal RESET_NOW can reset the processor earlier when all data has been saved and the processor is ready.

Watchdog mode application example

The processor code contains a routine to periodically maintain the RESET_CLEAR signal. When software crashes, the RESET_CLEAR pin is not toggled, the STBC02 timer overflows and the generated nRESET pulse resets the processor. RST_PENDING follows nRESET signal (RST_SIGNAL is not used in Watchdog mode).

nRESET pin

- output signal
- open drain output
- 50 µs in battery mode / 25 µs in V_{IN} mode pulse duration.
- Active low
- No internal resistor integrated: external pull-down requested.

RST_PENDING pin

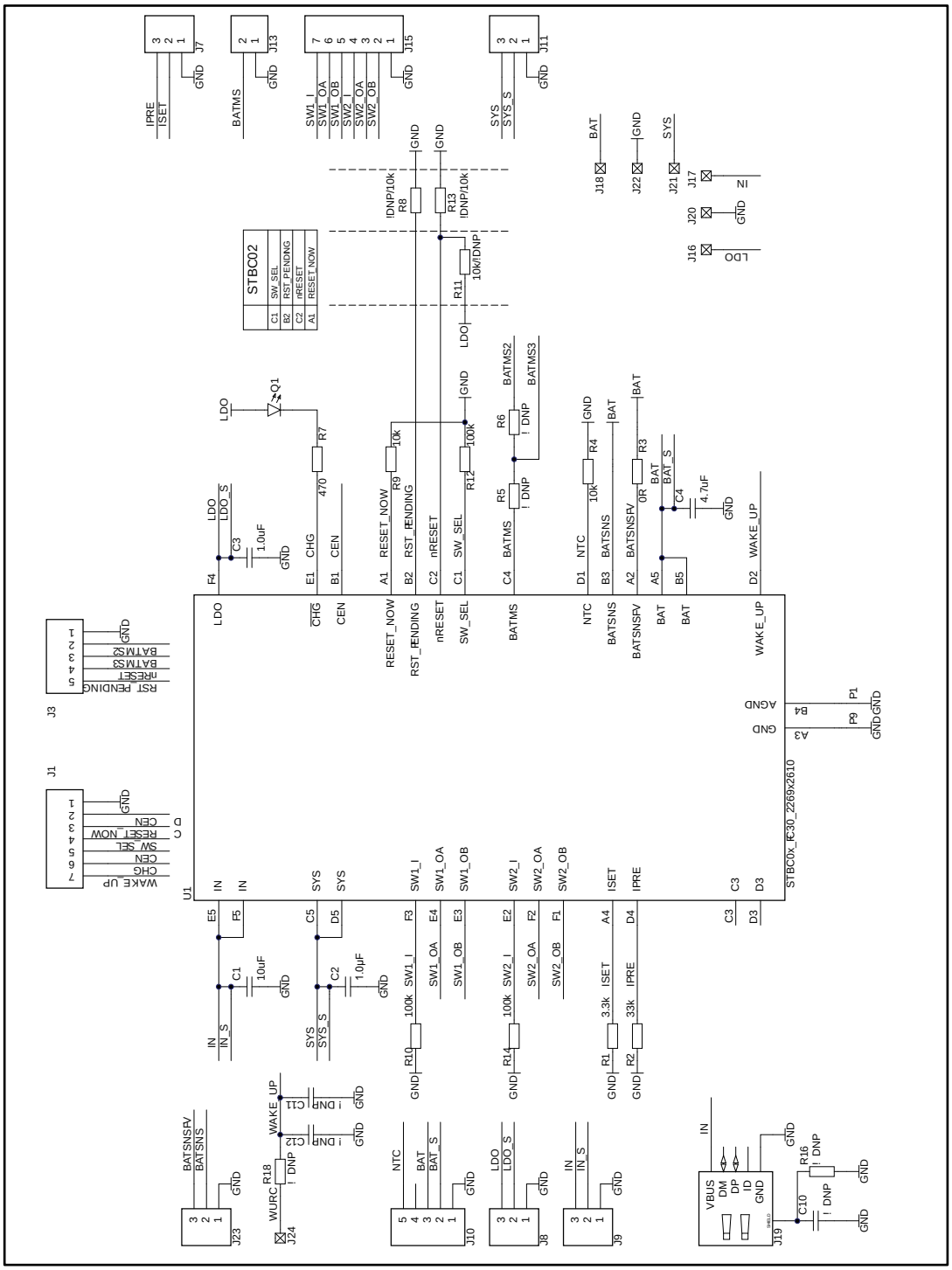
- output signal
- totem pole output: no external resistor requested

RESET_NOW pin (called also RESET_CLEAR in watchdog mode)

- input signal
- external pull-down highly recommended
- referred to LDO level
- smart reset mode: low to high transition forces immediate nRESET
- watchdog mode: high level at RESET_NOW pin clears Watchdog timer (RESET_NOW high to low transition enables counter, timer starts counting from zero, nRESET is generated after watchdog period if RESET_NOW is kept low).

3 Schematic diagram

Figure 5: STEVAL-ISB041V1 circuit schematic



4 PCB layout

Figure 6: STEVAL-ISB041V1 PCB layout: top side

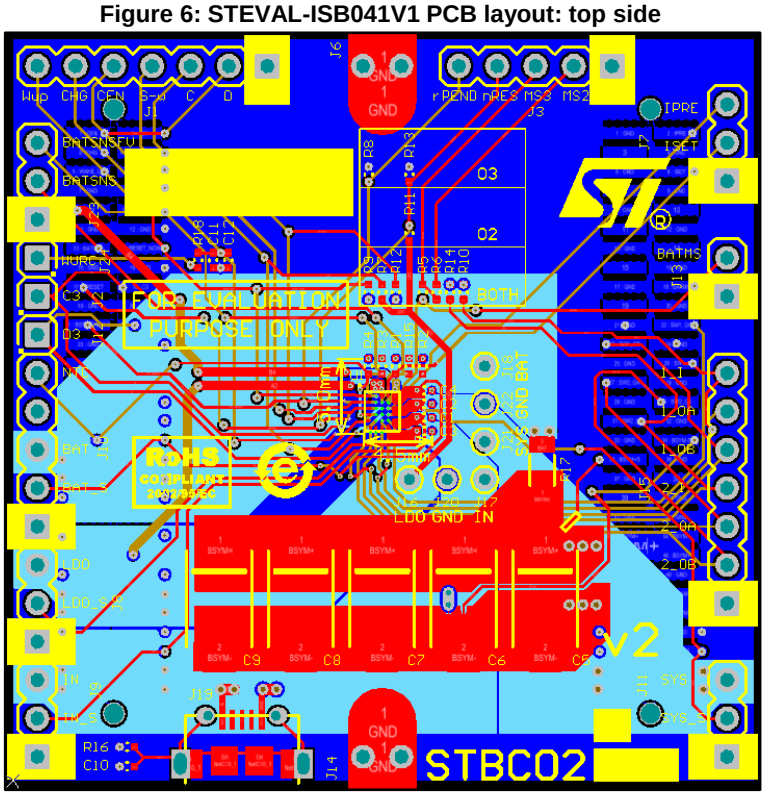
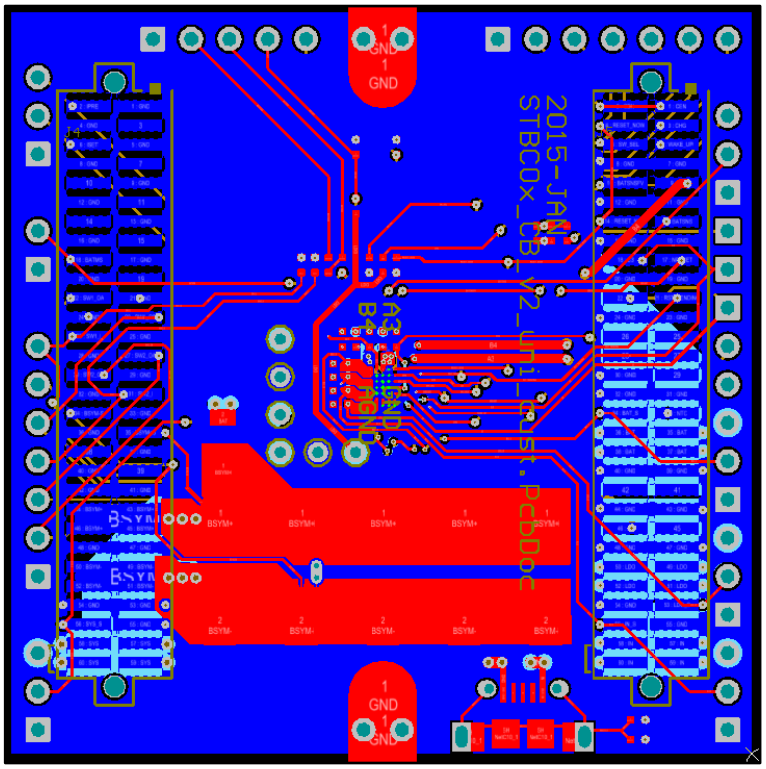


Figure 7: STEVAL-ISB041V1 PCB layout: bottom side



5 STBC02: block diagram and ballout

Figure 8: STBC02 block diagram

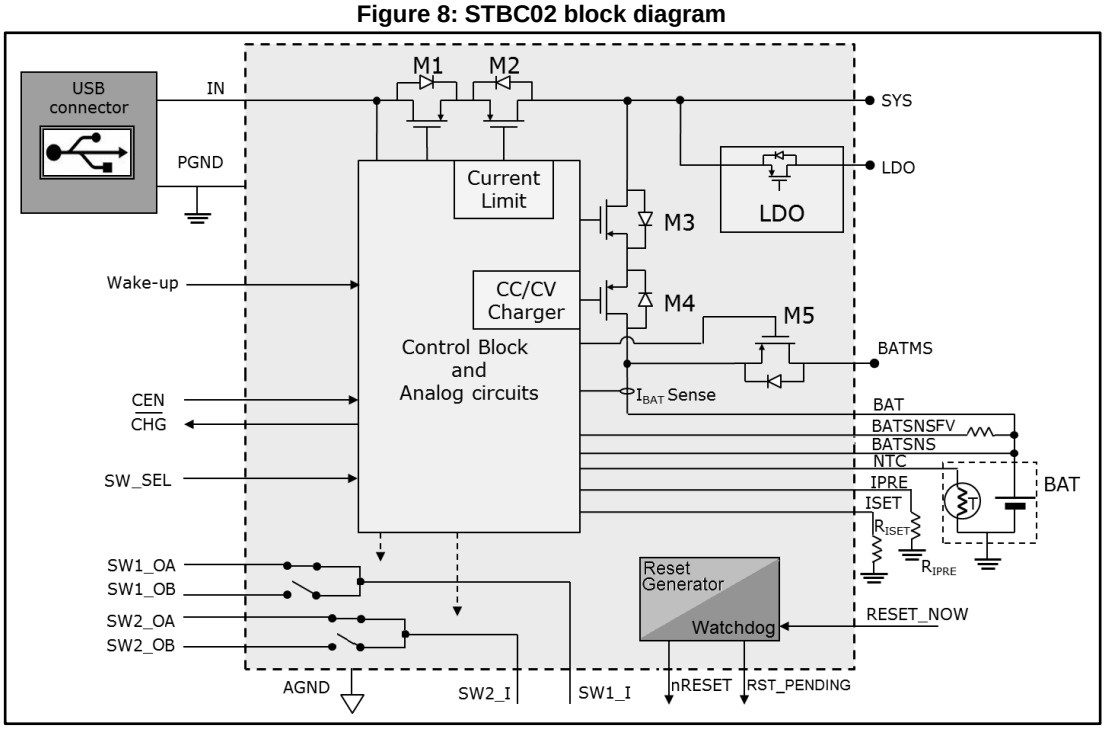


Figure 9: STBC02 (flipchip30, 2.25 mm x 2.59 mm package): ballout, top view

	1	2	3	4	5
A	A1 RESET_NOW	A2 BATSNSFV	A3 GND	A4 ISET	A5 BAT
B	B1 CEN	B2 RST_PENDING	B3 BATSNS	B4 AGND	B5 BAT
C	C1 SW_SEL	C2 NRESET	C3 C3	C4 BATMS	C5 SYS
D	D1 NTC	D2 WAKE_UP	D3 D3	D4 IPRE	D5 SYS
E	E1 CHG	E2 SW2_I	E3 SW1_OB	E4 SW1_OA	E5 IN
F	F1 SW2_OB	F2 SW2_OA	F3 SW1_I	F4 LDO	F5 IN

Table 3: Ball description

Bump name		Alternative bump name	Description	
Power	IN	E5-F5	Input supply voltage. Bypass this pin to ground with a 2.2 µF capacitor	
	BAT	A5-B5	Battery positive terminal. Bypass this pin to GND with a 4.7 µF ceramic capacitor	
	SYS	C5-D5	System output. Bypass this pin to ground with a 2.2 µF ceramic capacitor	
	LDO	F4	3.1 V LDO output. Bypass this pin to ground with a 1 µF ceramic capacitor	
	NTC	D1	Battery temperature monitor pin	
	AGND	B4	Analog Ground	Connect together with the same ground layer
	GND	A3	GROUND	
Prog	ISET	A4	Fast-charge current programming resistor	
	IPRE	D4	Pre-charge current programming resistor	
Sensing	BATMS	C4	Battery voltage measurement pin	
	BATSNS	B3	Battery voltage sensing. Connect as close as possible to the battery positive terminal	
	BATSNSFV	A2	Floating voltage sensing. Connect as close as possible to the battery positive terminal	
Digital I/Os	CEN	B1	Charger enable pin. Active high. 500 kΩ internal pull-up (to LDO)	
	CHG	E1	Charging/fault Flag. Active low (open drain output)	
	WAKE-UP	D2	Shipping mode exit input pin. Active high. 500 kΩ internal pull-down	
	SW_SEL	C1	Load switch selection input	
	nRESET	C2	Smart reset output signal (open drain output)	
	RST_PENDING	B2	Reset output signal (Totem pole output)	
	RESET_NOW	A1	Smart reset input signal (referred to LDO level); RESET_CLEAR when watchdog is enabled	
Switch Matrix	SW1_I	F3	Load switch SPDT1 input (connect to 1.8 to 5 V range)	Decoupling capacitors are recommended on input and output pins for noise minimization. These switches are not voltage regulated.
	SW1_OA	E4	Load switch SPDT1 output A (enabled/disabled PMOS)	
	SW1_OB	E3	Load switch SPDT1 output B (enabled/disabled PMOS)	
	SW2_I	E2	Load switch SPDT2 input (connect to 1.8 to 5 V range)	

Bump name		Alternative bump name	Description	
	SW2_OA	F2	Load switch SPDT2 output A (enabled/disabled PMOS)	
	SW2_OB	F1	Load switch SPDT2 output B (enabled/disabled PMOS)	
	NC	C3-D3	Not connected	

6 Revision history

Table 4: Document revision history

Date	Version	Changes
28-Mar-2017	1	Initial release.

Appendix A General handling precautions

- Do not modify or manipulate the board and the device when the board is powered and/or connected to the load;
- Do not supply the board with a DC source higher than the device maximum voltage;
- Any equipment or tool used for any manipulation of the semiconductor devices or board modification should be connected to ground to avoid ESD;
- The connectors and cables must be plugged and removed when the board is not supplied;
- Antistatic tools are recommended.

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